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Atmel
AT73C204-EK

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Features

- 300 mA/1.9V/2.5V DC to DC for Co-processor Core
- 80 mA/2.8V Dual-mode LDO for Memories (LDO1)
- 130 mA/2.7V/2.8V LDO for Camera Module (LDO2)
- 130 mA/2.8V LDO for Analog Section Supply of Audio Stereo Codec (LDO6)
- 10 mA/1.8V/2.8V LDO for Digital Section Supply of Audio Stereo Codec (LDO7)
- 130 mA/2.8V LDO for Analog Section Supply of Bluetooth® Module (LDO4)
- 130 mA/2.8V LDO for Digital Section Supply of Bluetooth® Module (LDO5)
- 2 mA/2.4V/2.7V LDO for Low-power Device Control (LDO3)
- Open Drain Switch
- Three-channel Level Shifters
- LED Driver
- 0.5 mA/1.5V Bufferized Voltage Reference
- Power Management Start-up Controller and Reset Generation
- Over- and Under-voltage Protections
- Over-temperature Protection
- Shutdown, Sleep and Enable Modes
- Straightforward and Easy Interfacing to any Baseband Controller
- Small 5 mm x 5 mm, 49-ball BGA Package

Description

The AT73C204 device provides an integrated power management solution for the add-on multimedia features in new-generation mobile phones. These features include a camera module, sound system for polyphonic ringing tones, memory module for downloaded MP3 files, Bluetooth module for cordless headset, etc. The most common approach to the IC architecture of these new-generation mobile phones is a baseband processor for the basic telephony functions and a separate co-processor for the multimedia features. Atmel proposes the AT73C202 for power management of the baseband processor and RF elements, and the AT73C204 for power management of the multimedia features.

The AT73C204 is suitable for any telecommunications standard: GSM/GPRS, PDS, CDMA, CDMA2000, WCDMA or UMTS. It is packaged in a small form-factor 49-ball 5 mm x 5 mm BGA package.

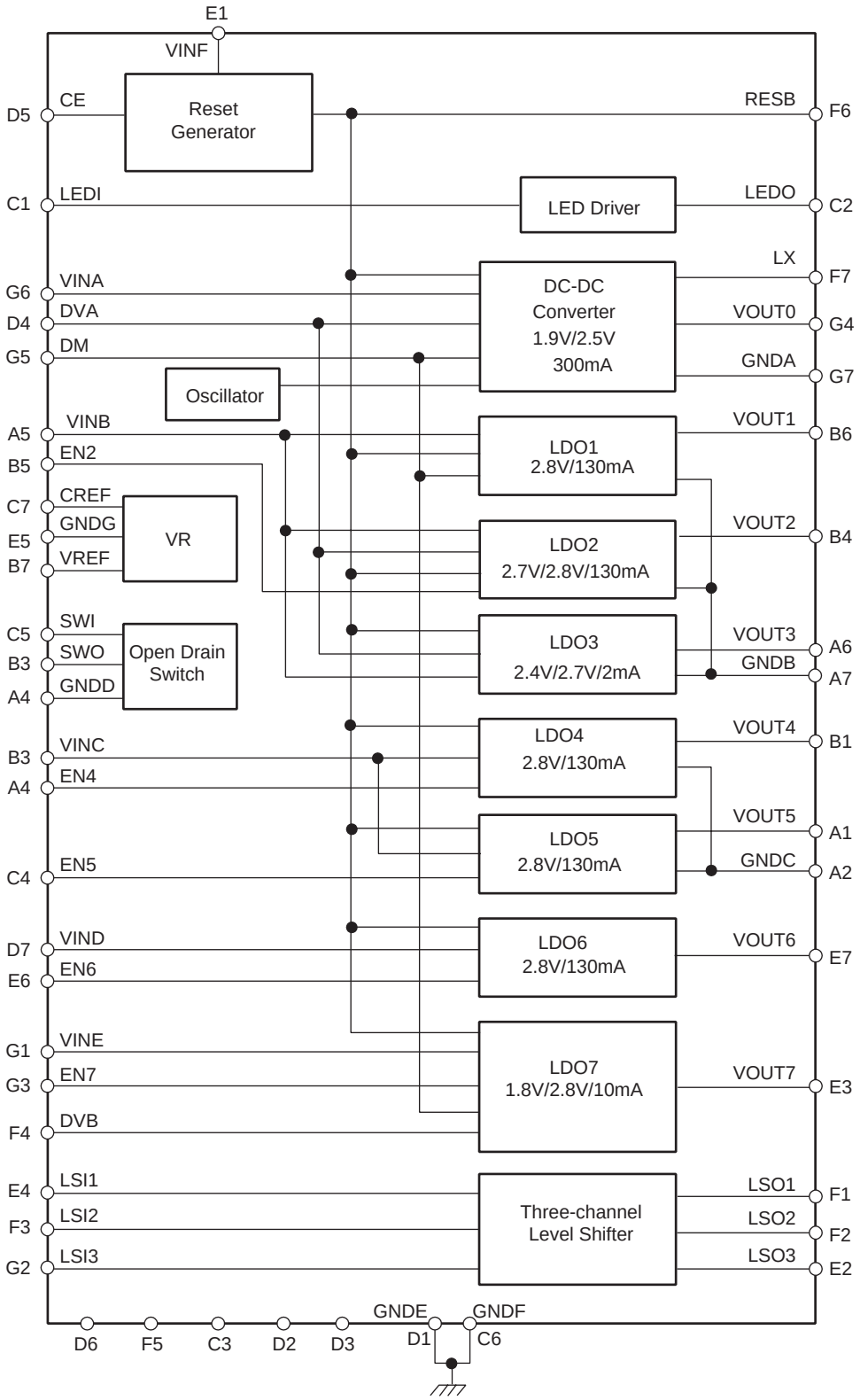
Power Management for Mobiles (PM)

AT73C204

6014A–PMGMT–10/03

Functional Block Diagram

Figure 1. AT73C204 Functional Block Diagram



Pin Description

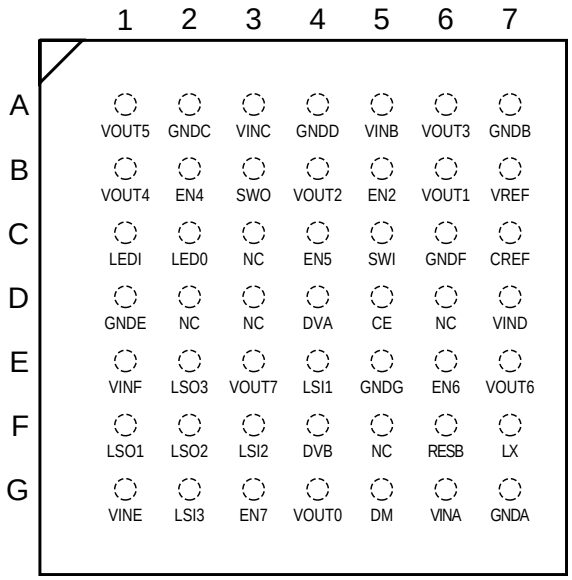
Table 1. AT73C204 Pin Description

Signal	Ball	Type	Description
LEDI	C1	I	LED driver input
LEDO	C2	O	LED driver output
VINF	E1	Power Supply	Input voltage
Power On Block			
CE	D5	I	Chip Enable
GNDF	C6	Ground	Ground
RES-B	F6	O	Reset open collector output
GNDG	E5	Ground	Ground
Baseband Supply Block			
VINA	G6	Power Supply	Input supply for DC-DC converter
LX	F7	O	DC-DC converter Output Inductor
DM	G5	I	Low-power/Full-power selector
VOUTO	G4	O	DC-DC converter output
GNDA	G7	Ground	Ground of DC-DC Converter
VINB	A5		Input supply for LDO1, LDO2, LDO3
EN2	B5	I	Enable LDO2
VOUT2	B4	O	LDO2 output voltage
GNDB	A7	Ground	Ground for LDO1, LDO2, LDO3
VOUT1	B6	O	LDO1 output voltage
VREF	B7	O	Bufferized voltage reference
VOUT3	A6	O	LDO3 output voltage
RF Supply Block			
VINC	A3	Power Supply	Input supply for LDO4, LDO5
EN4	B2	I	Enable LDO4
EN5	C4	I	Enable LDO5
VOUT4	B1	O	LDO4 output voltage
GNDC	A2	Ground	Ground for LDO4, LDO5
VOUT5	A1	O	LDO5 output voltage
Vibrator and Buzzer Driver Block			
VIND	D7	Power Supply	LDO6 input supply
EN6	E6	I	Enable LDO6
VOUT6	E7	O	LDO6 output voltage
SWI	C5	I	Open drain enable
SWO	B3	O	Open drain output

Table 1. AT73C204 Pin Description (Continued)

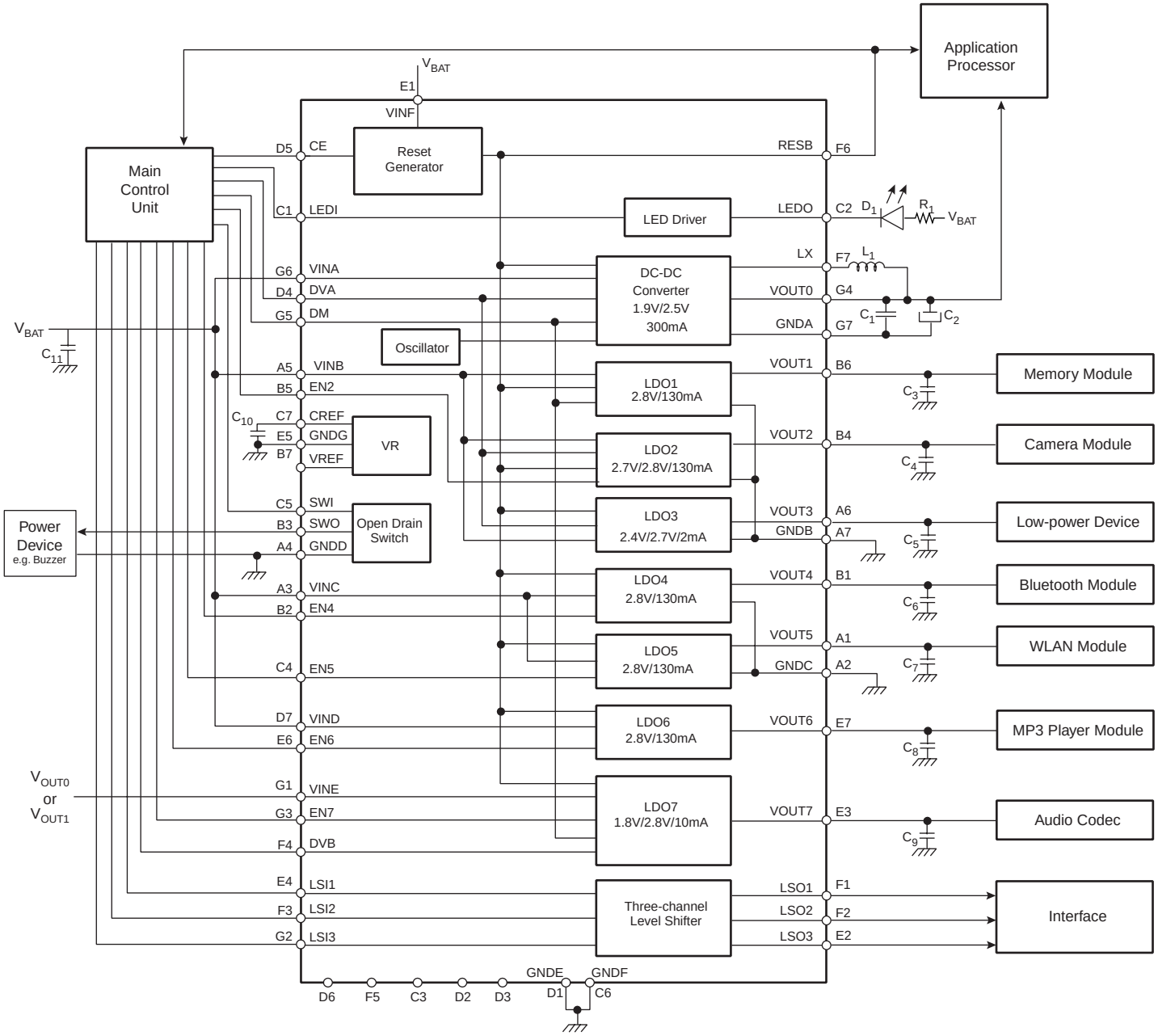
Signal	Ball	Type	Description
GNDD	A4	Ground	Open drain ground
SIM Interface Block			
VINE	G1	Power Supply	LDO7 input supply
EN7	G3	I	Enable LDO7
DVB	F4	I	Dual-voltage setting on LDO7
LSI1	E4	I	Channel 1 level shifter input
LSI2	F3	I	Channel 2 level shifter input
LSI3	G2	IO	Channel 3 level shifter input
VOUT7	E3	O	LDO7 output voltage
LSO1	F1	O	Channel 1 level shifter output
LSO2	F2	O	Channel 2 level shifter output
LSO3	E2	IO	Channel 3 level shifter output
Miscellaneous			
CREF	C7	IO	Band gap decoupling
GNDE	D1	Ground	Digital ground
DVA	D4	I	Dual-voltage setting for DC-DC, LDO2, LDO3
NC	D2		
NC	D3		
NC	C3		
NC	D6		

Figure 2. AT73C204 Pin Configuration in 49-ball BGA Package



Application Schematic

Figure 3. AT73C204 Application Schematic



External Components Specifications

Table 2. External Component Specifications

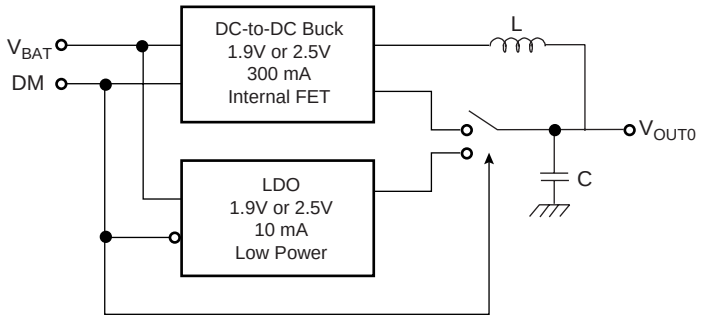
Symbol	Parameters
R1	4.7 kΩ, 1/8 W, 0603
C1, C3, C4, C5, C6, C7, C8	2.2 µF - X5R 6.3V/10%, 0603
C2	22 µF Tantale R, TYPEA
C9	220 nF - X5R 10V/10%, 0603
C10	10 nF - X5R 10V/10%, 0402
C11	10 µF - X5R 6.3V/10%
L1	10 µH
D1	HSMH - C670

Functional Description

300 mA/1.9V/2.5V DC-to-DC Converter for Co-processor Core

This DC-to-DC converter is a synchronous mode DC-to-DC “buck”-switched regulator using fixed- frequency architecture (PWM) and capable of providing 300 mA of continuous current. It has two levels of voltage programming for the co-processor core (1.9V or 2.5V). The operating supply range is from 3.1V to 4.2V, making it suitable for Li-Ion, Li-polymer or Ni-MH battery applications. This DC-to-DC converter is based on the pulse width modulation architecture to control the noise perturbation for switching noise sensitive applications (GSM). The operating frequency is set to 900 KHz using an internal clock, allowing the use of small surface inductor and moderate output voltage ripple. The controller consists of a reference ramp generator, a feedback comparator, the logic driver used to drive the internal switches, the feedback circuits used to manage the different modes of operation and the over-current protection circuits. An economic mode has been defined to reduce quiescent current. A low-dropout voltage regulator in parallel to the DC-to-DC converter minimizes standby current consumption during standby mode.

Figure 4. Dual-power DC-to-DC Converter



Low undershoot voltage is expected when going from PWM to LDO mode and vice-versa. The circuit is designed in order to avoid any spikes when transition between two modes is enabled.

Figure 5. Low-power/Full-power DC-to-DC Converter Transition

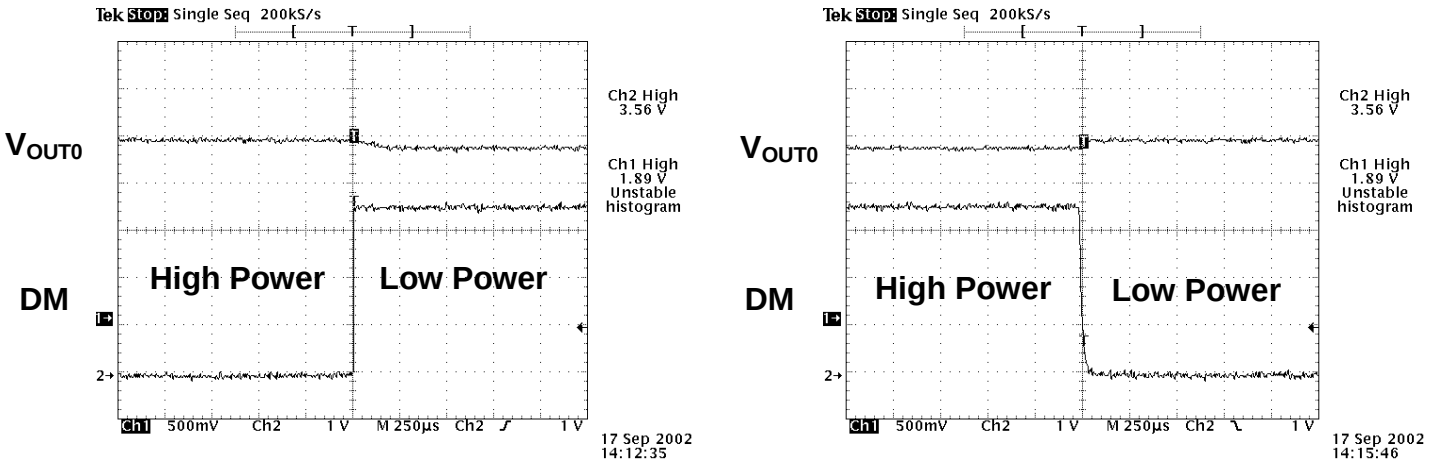
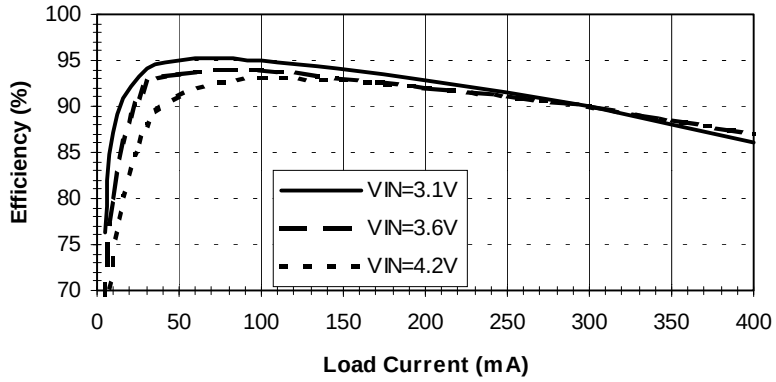


Figure 6 shows typical efficiency levels of the DC-to-DC converter for several input voltages.

Figure 6. DC-to-DC Converter with 1.9V Target Typical Case(1)



Note: 1. L = 10 µH, ESR = 0.2 Ohm, c = 22 µF, @ESR = 0.1 Ohm

LDO1, LDO3, LDO4, LDO5

The PSRR measures the degree of immunization against voltage fluctuations achieved by a regulator. An example of its importance is in the case of a GSM phone when the antenna switch activates the RF power amplifier (PA). This causes a current peak of up to 2A on the battery, with an important spike on the battery voltage. The voltage regulator must filter or attenuate this spike.

Figure 7. Functional Diagram of LDO Single Mode

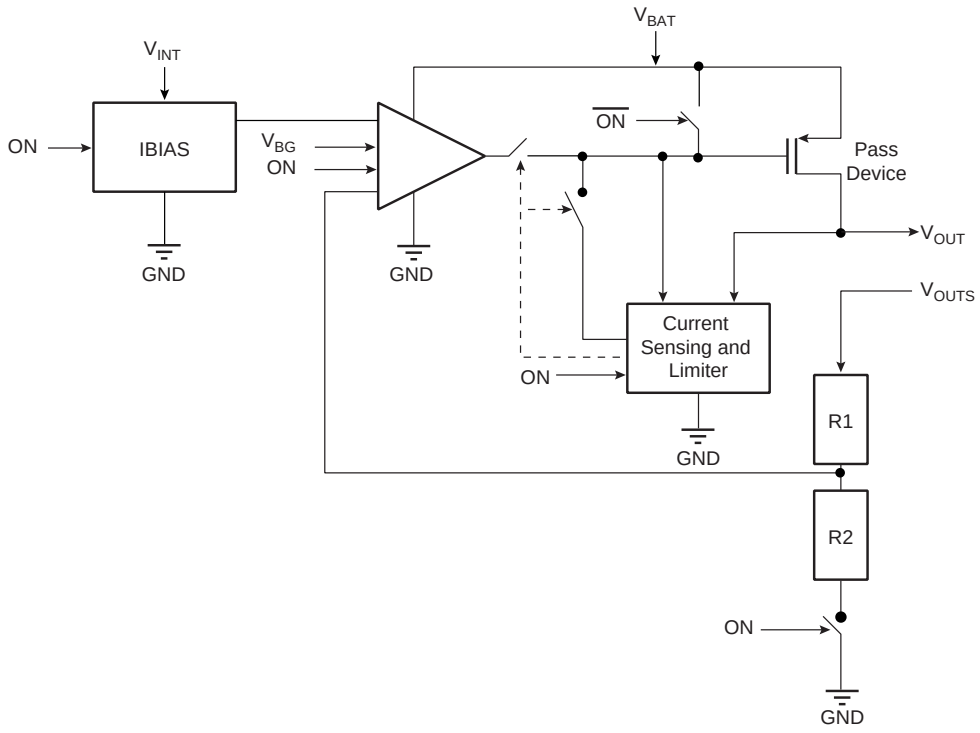
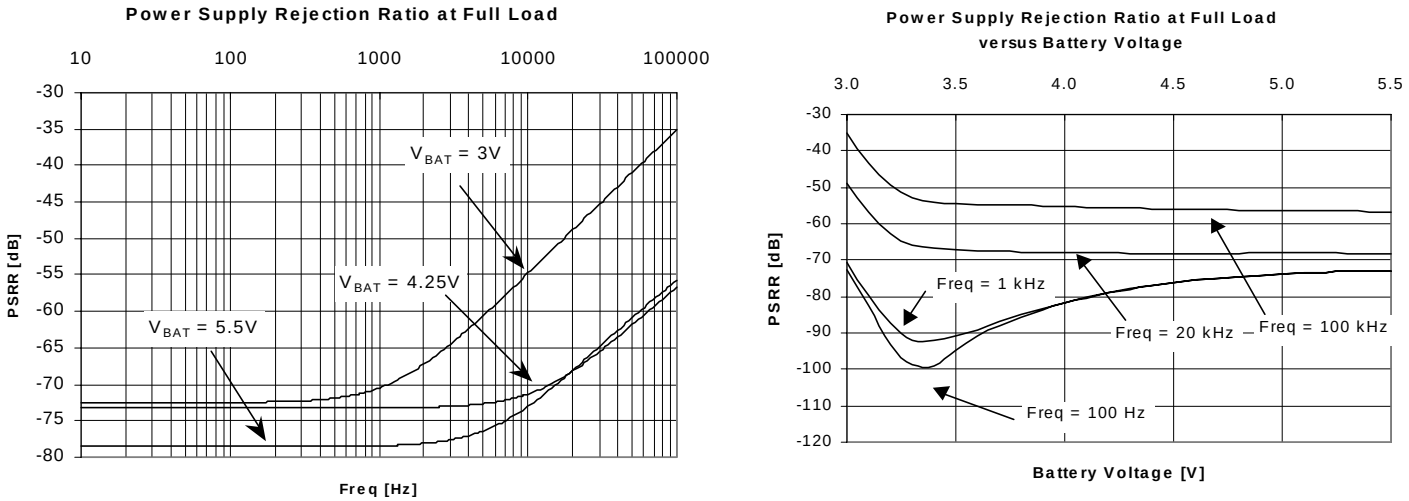


Figure 8 shows the Power Supply Rejection Ratio as functions of frequency and battery voltage. If a noise signal occurs at 1 kHz when the battery voltage is at 3V, the noise will be attenuated by 70 dB (divided by more than 3000) at the output of the regulator. Consequently, a 2V spike on the battery is attenuated to less than 1 mV, which is low enough to avoid any risk of malfunction by a device supplied by the regulator.

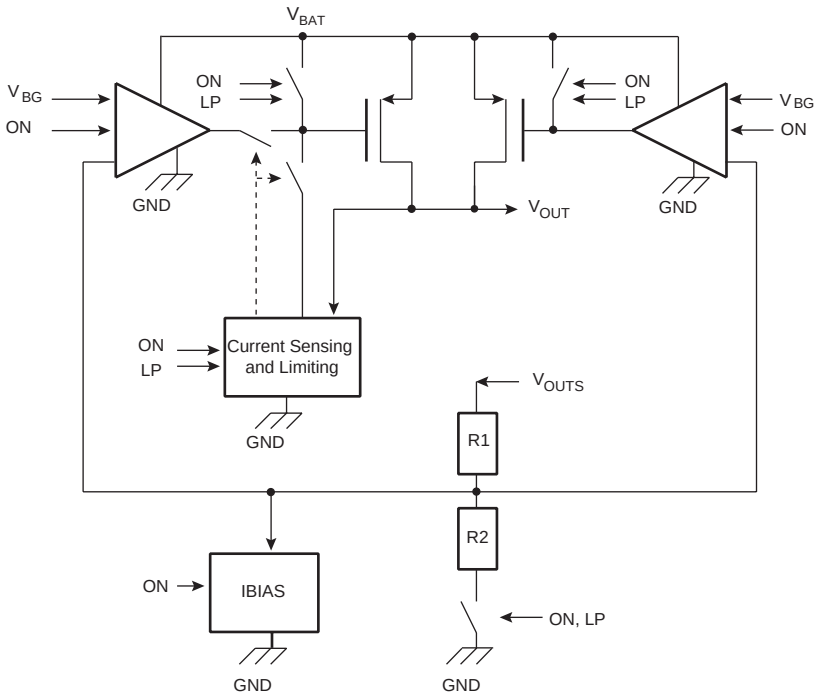
Figure 8. Power Supply Rejection Ratio in Function of Frequency and Battery Voltage



LDO2, LDO6

The first approach to reducing standby current is to decrease the standby current inside the regulators themselves. Atmel achieves this by implementing a dual mode architecture where two output transistors are used in parallel as switches in the regulation loop. Figure 9 illustrates this architecture.

Figure 9. Functional Diagram of LDO Dual Mode



In Figure 9, the left-hand output transistor is sized large enough for the required output current under full load, for example, 100 mA. In order to achieve a sufficient margin of stability, the current sensing block uses a bias cell where the current consumption is linked to the required output current. The higher the output current, the higher the bias current needed to stabilize the loop.

The right-hand output transistor delivers a very small output current, typically less than 1 mA, sufficient only to maintain the output voltage with enough current to cover the leakage current of the supplied device. This requires a much smaller bias current and, consequently, a smaller standby current inside the regulator.

LDO7

This regulator has extremely low quiescent current and is suited where power supply is enabled almost all the time. Typical use could be the supply of back-up battery.

Temperature Sensor

The temperature sensor voltage output is a linear function of temperature.

The temperature seen by the sensor is directly related to the chip activity and the power internally dissipated. To get a good indication of the ambient temperature, the software must take into account this offset.

Three-channel Level Shifters

This block provides a DC-to-DC or Memory Card level shifter and specific ESD protections. Signals are level-shifted on the LDO2 supply, allowing dual-voltage option: 1.8V or 2.8V. If the memory type is Subscriber Identity Module (SIM) Card, level shifters are compliant with ETSI GSM11.12 & 11.18.

Absolute Maximum Ratings

Operating Temperature (Industrial)..... -40°C to +85°C Storage Temperature ..... -55°C to + 150°C Power Supply Input V_{INA}, V_{INB},...,V_{INF} ..... -0.3V to +6.5V I/O Input (all except to power supply..... -0.3V to V_{MAX}+0.3	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Conditions	Min	Maw	Unit
Operating Temperature		-20	85	°C
Power Supply Input	V_{INA}, V_{INB},..., V_{INF}	3.0	4.5	V

Electrical Characteristics

V_{OUT0}

Table 4. V_{OUT0} Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INA}	Operating Supply Voltage		3		5.5	V
V_{OUT0}	Output Voltage	Full-power (DVA = 0, DM = 0)	1.80	1.90	2.0	V
V_{OUT0}	Output Voltage	Full-power (DVA = 1, DM = 0)	2.45	2.50	2.55	V
I_{OUT0}	Output Current	Full-power (DM = 0)		300	400	mA
ISD	Shutdown Current			0.1	1	µA
E_{FF}	Efficiency	I_{OUT} = 10 mA to 200 mA @1.9V		90		%
ΔV_{DCLD}	Static Load Regulation	Full-power Mode (10% to 90% of $I_{OUT(MAX)}$		50		mV
ΔV_{TRLD}	Transient Load Regulation	Full-power Mode (10% to 90% of $I_{OUT(MAX)}$, $T_R = T_F = 5µs$		50		mV
ΔV_{DCLE}	Static Line Regulation	Full-power Mode (10% to 90% of $I_{OUT(MAX)}$, 3.2V to 4.2V)		20		mV
ΔV_{TRLE}	Transient Line Regulation	Full-power Mode (10% to 90% of $I_{OUT(MAX)}$, 3.2V to 4.2V)		35		mV
V_{OUT0}	Output Voltage	Low-power Mode (DVA = 0, DM = 1)	1.75	1.85	1.95	V
V_{OUT0}	Output Voltage	Low-power Mode (DVA = 1, DM = 1)	2.35	2.40	2.45	V
I_{OUT0}	Output Current	Low-power Mode (DM = 1)			10	mA
V_{DROP}	Dropout Voltage	Low-power Mode (DM = 1)			400	mV
I_{QC}	Quiescent Current	Low-power Mode (DM = 1)		11	14	µA
ΔV_{DCLD}	Static Load Regulation	Low-power Mode (0 to 10 mA)			50	mV
ΔV_{TRLD}	Transient Load Regulation	Low-power Mode (0 to 10 mA), $T_R = T_F = 5µs$			10	mV
ΔV_{DCLE}	Static Line Regulation	Low-power Mode (3.2V to 4.2V)			8	mV
ΔV_{TRLE}	transient Line Regulation	Low-power Mode (3.2V to 4.2V)			15	mV
PSRR	Ripple Rejection	Low-power Mode up to 1 KHz	40	45		dB
ΔV_{LPFP}	Overshoot Voltage	Voltage drop from Low-power to Full-power		0	10	mV
ΔV_{FPLP}	Undershoot Voltage	Voltage drop from Low-power to Full-power	-15	0		mV

LDO2

Table 5. LDO2 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB}	Operating Supply Voltage		3		5.5	V
V_{OUT2}	Output Voltage	DVA = 0	2.65	2.70	2.75	V
V_{OUT2}	Output Voltage	DVA = 1	2.75	2.80	2.85	V
V_{INT}	Internal Supply Voltage		2.4		2.6	V
I_{OUT2}	Output Current			80	130	mA
I_{QC}	Quiescent Current			195	236	µA
DV_{OUT}	Line Regulation	V_{BAT}: 3V to 3.4V, I_{OUT} = 130 mA		3		mV
DV_{PEAK}	Line Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		4		mV
DV_{OUT}	Load Regulation	10% - 90% I_{OUT}, V_{BAT} = 3V		10		mV
		10% - 90%I_{OUT}, V_{BAT} = 5.0V		15		mV
		10% - 90% I_{OUT}, V_{BAT} = 5.5V		15		mV
DV_{PEAK}	Load Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		15		mV
PSRR	Ripple rejection	F = 217Hz – V_{BAT} = 3.6V		70		dB
V_N	Output Noise	BW: 10 Hz to 100 kHz		29		μV_{RMS}
T_R	Rise Time	100% I_{OUT}, 10% - 90% V_{OUT}			50	µs
I_{SD}	Shut Down Current				1	µA

LDO1

Table 6. LDO1 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB}	Operating Supply Voltage		3		5.5	V
V_{OUT1}	Output Voltage Full Power Mode		2.74	2.80	2.86	V
I_{OUT1}	Output Current Full Power Mode			50	80	mA
I_{OUT}	Output Current Low Power Mode				10	mA
I_{QC}	Quiescent Current FP Mode		25	30	36	µA
I_{QC}	Quiescent Current LP Mode		9.75	11.5	13.75	µA
DV_{OUT}	Line Regulation FP Mode	V_{BAT}: 3.4V to 3V, I_{OUT} = 80 mA			1	mV
DV_{PEAK}	Line Regulation Transient FP Mode	V_{BAT}: from 5V to 5.4V and from 3.4V to 3V, I_{OUT} = 80 mA, $T_R = T_F$ = 5 µs			3	mV
DV_{OUT}	Line Regulation LP Mode	V_{BAT}: 3.4V to 3V, I_{OUT} = 5 mA			3	mV
DV_{PEAK}	Line Regulation Transient LP Mode	V_{BAT}: from 5V to 5.4V and from 3.4V to 3V, I_{OUT} = 5 mA, $T_R = T_F$ = 5 µs			4	mV
DV_{OUT}	Load Regulation FP Mode	From 0 to 80mA and from 90% to 10% $I_{OUT(MAX)}$, V_{BAT} = 3.4V			3 (4 at 5.5V)	mV
DV_{PEAK}	Load Regulation Transient FP Mode	From 0 to $I_{OUT(MAX)}$ and from 90% to 10% $I_{OUT(MAX)}$, $T_R = T_F$ = 5 µs, V_{BAT} = 3.4V			23	mV
DV_{OUT}	Load Regulation LP Mode	From 0 to 80mA and from 90% to 10% $I_{OUT(MAX)}$, V_{BAT} = 3.4V			5 (10 at 5.5V)	mV
PSRR	Ripple Rejection	F = 217Hz	40	45		dB
V_N	Output Noise FP mode	BW: 10 Hz to 100 kHz			80	μV_{RMS}
V_N	Output Noise LP Mode	BW: 10 Hz to 100 kHz			300	μV_{RMS}
T_R	Rise Time FP	$I_{OUT} = I_{OUT(MAX)}$	70		130	µs
T_R	Rise Time LP	$I_{OUT} = I_{OUT(MAX)}$	50		170	µs
I_{SD}	Shut Down Current				1	µA
V_{BAT}	Operating Supply Voltage		3		5.5	V
V_{SAUV}	Internal Operating Supply Voltage		2.74	2.8	2.86	V
I_{SC}	Short Circuit Current			50	80	mA

LDO3

Table 7. LDO3 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB}	Operating Supply Voltage		3		5.5	V
V_{OUT3}	Output Voltage	BB1 = 0	2.4	2.45	2.50	V
V_{OUT3}	Output Voltage	BB1 = 1	2.65	2.70	2.75	V
I_{OUT3}	Output Current			2	5	mA
V_{DROP}	Dropout Voltage				50	mV
I_{QC}	Quiescent Current		4.8	6.6	9.7	µA
PSRR	Ripple Rejection			40		dB
T_R	Rise Time		110		320	µs

Buffered Voltage Reference

Table 8. Buffered Voltage Reference Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF}	Output Voltage		1.45	1.50	1.55	V
I_{REF}	Output Current				0.5	mA
V_{DROP}	Dropout Voltage				50	mV
I_{QC}	Quiescent Current		4.8	6.6	9.7	µA
I_{SD}	Shutdown Current			0.1	1	µA
PSRR	Ripple Rejection			40		dB
T_R	Rise time		110		320	µs

LDO4, LDO5, LDO6

Table 9. LDO4, LDO5, LDO6 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INC}	Operating Supply Voltage		3		5.5	V
V_{INT}	Operating Internal Supply Voltage		2.4	2.5	2.6	V
V_{OUT}	Output Voltage		2.74	2.8	2.86	V
I_{OUT}	Output Current			80	130	mA
I_{QC}	Quiescent Current			195	236	µA
DV_{OUT}	Line Regulation	V_{BAT}: 3V to 3.4V, I_{OUT} = 130 mA		3	2	mV
DV_{PEAK}	Line Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		4	2.85	mV
DV_{OUT}	Load Regulation	10% - 90% I_{OUT}, V_{BAT} = 3V		10	1	mV
		10% - 90% I_{OUT}, V_{BAT} = 5.0V		15	1	mV
		10% - 90% I_{OUT}, V_{BAT} = 5.5V		15	1	mV
DV_{PEAK}	Load Regulation Transient	Same as above, $T_R = T_F$ = 5 µs		1.2	2.4	mV
PSRR	Ripple Rejection	F=217Hz – V_{BAT} = 3.6V	70	73		dB
V_N	Output Noise	BW: 10 Hz to 100 kHz		29	37	μV_{RMS}
T_R	Rise Time	100% I_{OUT}, 10% - 90% V_{OUT}			50	µs
I_{SD}	Shut Down Current				1	µA

Open Drain Switch

Table 10. Open Drain Switch Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Low Output Voltage	I_{OL} = 100 mA			0.4	V
I_{OL}	Low Output Current				100	mA
T_{ON}	Turn-on Time				10	µs
T_{OFF}	Turn-off Time				10	µs

LDO7

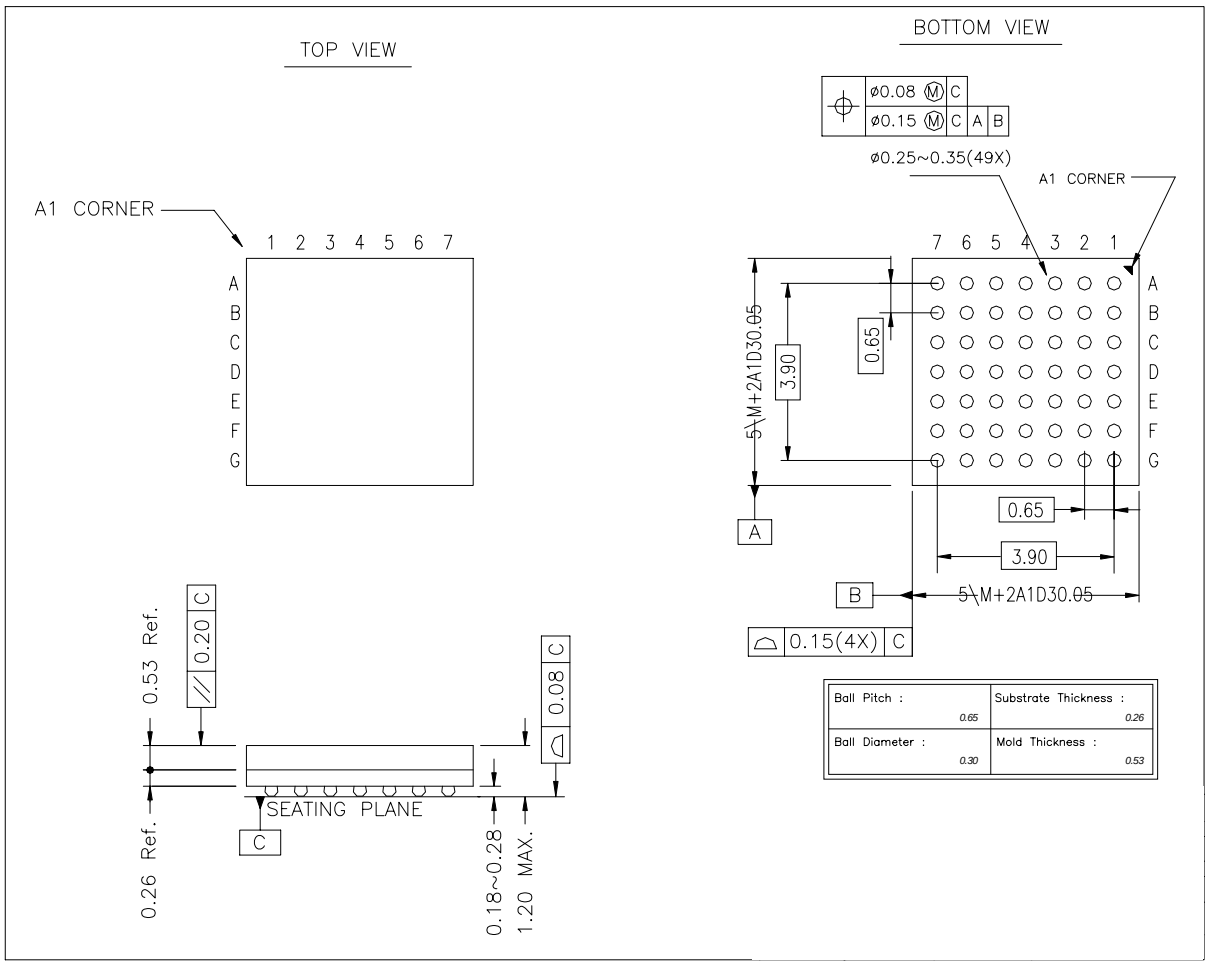
Conditions are V_{INE} = 1.8V or 2.8V, t_A = -40°C to +85°C, C_{DVCC} = 100 nF, CSIM-V_{CC} = 100 nF

Table 11. LDO7 Electrical Characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INE}	Operating Supply Voltage	V_{OUT0} or V_{OUT1}	1.65			
V_{OUT7}	Output Voltage	I_{OUT7} < 10 mA EN7 = 1 DVB = 1	1.71	1.8	1.89	V
V_{OUT7}	Output Voltage	I_{OUT7} < 10mA EN7 = 1 DVB = 0	2.74	2.8	2.86	V
I_{SD}	Total Shutdown Current	EN7 = 0		0.1	1	µA
I_{QC}	Quiescent Current	Low-power Mode		8	9.5	µA
I_{QC}	Quiescent Current	Full-power Mode			60	µA
I_{OUT7}	Output Current			10		mA
I_{SC}	Short Circuit Current				40	mA

Packaging Information

Figure 10. Mechanical Package Drawing for 49-ball Ball Grid Array



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