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STMicroelectronics
ESDALC6V1W5

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# ESDALC6V1W5

## Quad TRANSIL™ array for data protection

## Main applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems
- Cellular phones and accessories
- Wireline and wireless telephone sets
- Set top boxes

## Features

- 4 Unidirectional Transil functions
- Breakdown voltage:
  $V_{BR}$ = 6.1 V minimum
- Low leakage current: < 1 µA
- Low capacitance: 7.5 pF at 3 V
- Very small PCB area < 4.2 $mm^2$ typically

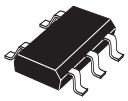
## Description

The ESDALCxxxWx are monolithic suppressors designed to protect components connected to data and transmission lines against ESD.

These devices clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

## Benefits

- High ESD protection level: up to 25 kV
- High integration

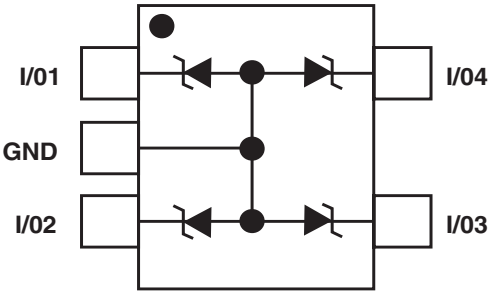


**SOT323-5L**

### Order codes

| Part Number | Marking |
|---|---|
| ESDALC6V1W5 | C61 |

### ESDALC6V1W5 Functional diagram




### Complies with the following standards

**IEC61000-4-2**

Level 4 — 15 kV (air discharge)
8 kV(contact discharge)

**MIL STD 883E - Method 3015-7 Class 3**

25 kV HBM (Human Body Model)

TM: TRANSIL is a trademark of STMicroelectronics

# 1 Characteristics

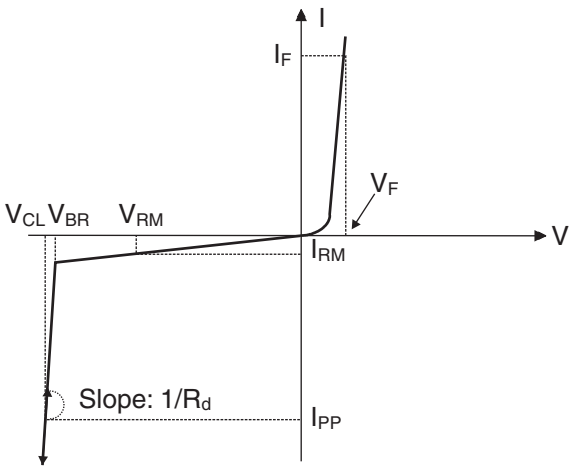
**Table 1. Absolute Ratings ($T_{amb}$ = 25°C)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $P_{PP}$ | Peak pulse power (8/20 µs) | 25 | W |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{stg}$ | Storage temperature range | -55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10s | 260 | °C |
| $T_{op}$ | Operating temperature range(1) | -40 to +150 | °C |

1. The values of the operating parameters versus temperature are given through curves and αT parameter.

## 1.1 Electrical Characteristics (Tamb = 25°C)

| Symbol | Parameter |
|---|---|
| $V_{RM}$ | Stand-off voltage |
| $V_{BR}$ | Breakdown voltage |
| $V_{CL}$ | Clamping voltage |
| $I_{RM}$ | Leakage current |
| $I_{PP}$ | Peak pulse current |
| $I_R$ | Reverse leakage current |
| $I_F$ | Forward current |
| αT | Voltage temperature coefficient |
| $V_F$ | Forward voltage drop |
| C | Capacitance |
| $R_d$ | Dynamic resistance |




| Part Numbers | $V_{BR}$@ $I_R$ | | | $I_{RM}$ @ $V_{RM}$ | | $R_d$ | αT | C |
|---|---|---|---|---|---|---|---|---|
| | min. | max. | | max. | | typ.(1) | max.(2) | typ. 3V bias |
| | V | V | mA | µA | V | Ω | $10^{-4}$/°C | pF |
| ESDALC6V1W5 | 6.1 | 7.2 | 1 | 1 | 3 | 1.1 | 6 | 7.5 |

1. Square pulse $I_{pp}$ = 15 A, $t_p$ = 2.5 µs
2. $V_{BR}$ = aT* ($T_{amb}$ - 25 °C) * $V_{BR}$ (25 °C)

**Figure 1. Peak power dissipation versus initial junction temperature**

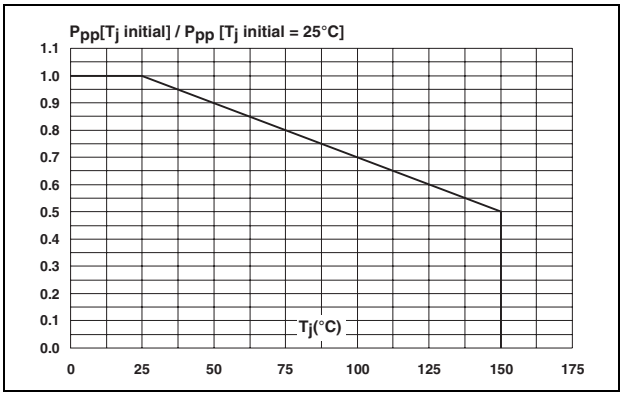



**Figure 2. Peak pulse power versus exponential pulse duration ($T_j$ initial = 25°C)**

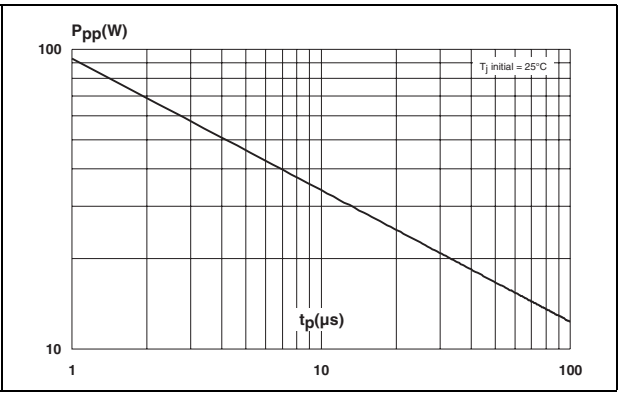



**Figure 3. Clamping voltage versus peak pulse current ($T_j$ initial = 25°C, rectangular waveform, $t_p$ = 2.5 µs)**

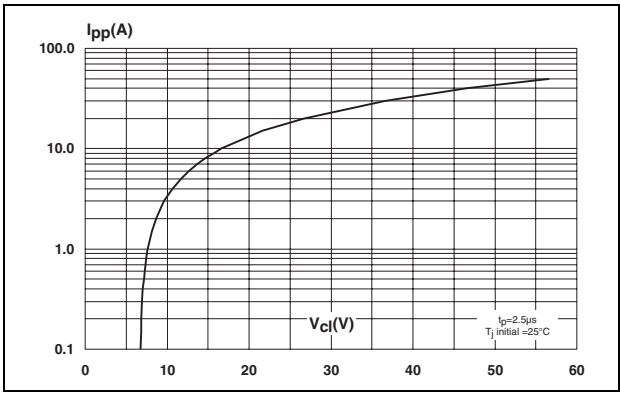



**Figure 4. Capacitance versus reverse applied voltage (typical values)**

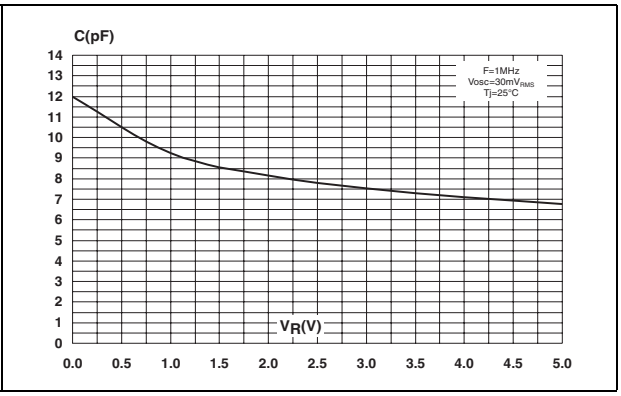



**Figure 5. Relative variation of leakage current versus junction temperature (typical values)**

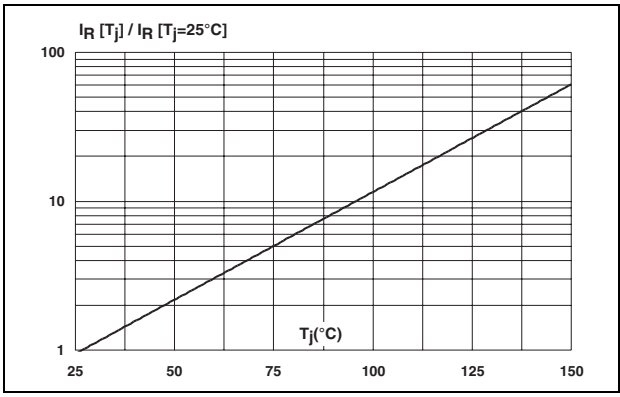



**Figure 6. Peak forward voltage drop versus peak forward current (typical values)**

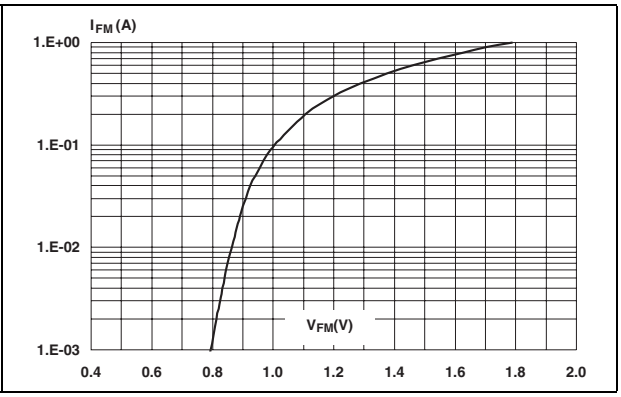
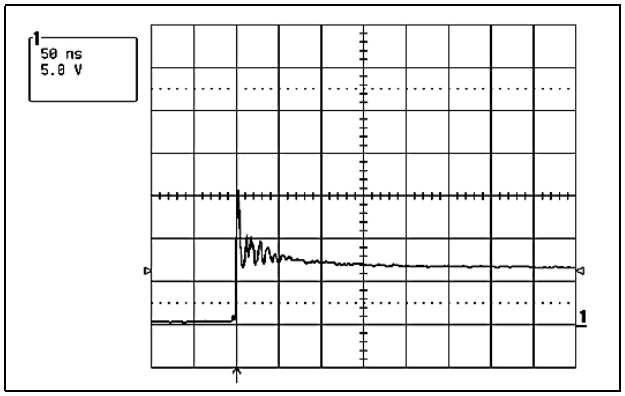


**Figure 7. ESD response to IEC61000-4-2 (air discharge 15 kV, positive surge)**




# 2 Ordering information scheme

**ESDA LC 6V1 W5**

**ESD Array**

**Low capacitance**

**Breakdown Voltage**

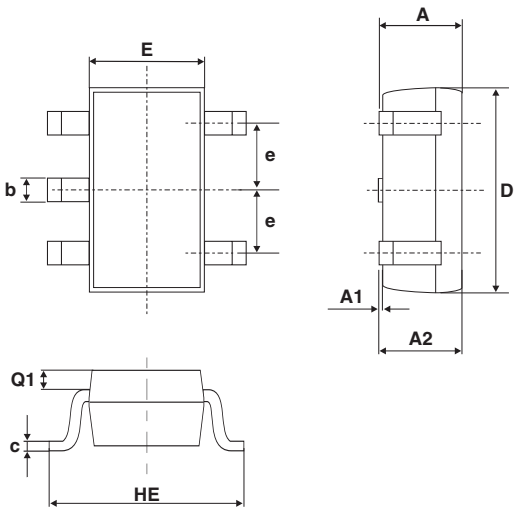
6V1 = 6.1 Volts min

**Package**

W5 = SOT323-5L

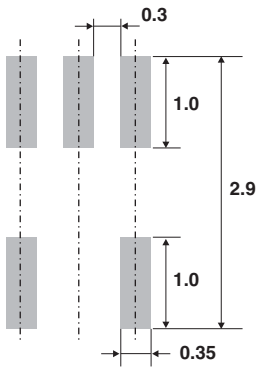
# 3 Package mechanical data

## 3.1 SOT323-5L package




| REF. | DIMENSIONS | | | |
|---|---|---|---|---|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | 0.8 | 1.1 | 0.031 | 0.043 |
| A1 | 0 | 0.1 | 0 | 0.004 |
| A2 | 0.8 | 1 | 0.031 | 0.039 |
| b | 0.15 | 0.3 | 0.006 | 0.012 |
| c | 0.1 | 0.18 | 0.004 | 0.007 |
| D | 1.8 | 2.2 | 0.071 | 0.086 |
| E | 1.15 | 1.35 | 0.045 | 0.053 |
| e | 0.65 Typ. | | 0.025 Typ. | |
| HE | 1.8 | 2.4 | 0.071 | 0.094 |
| Q1 | 0.1 | 0.4 | 0.004 | 0.016 |

**Figure 8. Footprint dimensions**




Dimensions in mm

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

# 4 Ordering information

| Part Number | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| ESDALC6V1W5 | C61 | SOT323-5L | 5.4 mg | 3000 | Tape & reel |

# 5 Revision history

| Date | Revision | Changes |
|---|---|---|
| Jun-2002 | 4A | Previous issue |
| 10-Jan-2006 | 5 | Reformatted to current template.<br>Figure 5: Range of $T_j$ extended to 150 °C.<br>Figure 6: Peak forward voltage drop versus peak forward current (typical values) added. |