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June1996

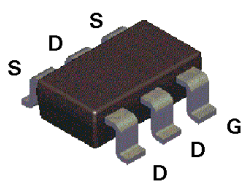
## NDC632P P-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

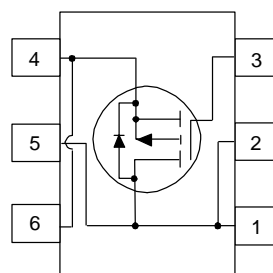
These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 2.7A, -20V.  $R_{DS(ON)} = 0.14\Omega @ V_{GS} = -4.5V$   
 $R_{DS(ON)} = 0.2\Omega @ V_{GS} = -2.7V$ .
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter		NDC632P	Units
$V_{DSS}$	Drain-Source Voltage		-20	V
$V_{GSS}$	Gate-Source Voltage - Continuous		-8	V
$I_D$	Drain Current - Continuous		-2.7	A
	- Pulsed		-10	
$P_D$	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.8	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	$^\circ\text{C/W}$

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$	
			$T_J = 55^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
<b>ON CHARACTERISTICS</b> (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$		-0.4	-0.7	-1	V
			$T_J = 125^\circ\text{C}$	-0.3	-0.5	-0.8	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$			0.1	0.14	$\Omega$
			$T_J = 125^\circ\text{C}$			0.145	0.28
			$V_{GS} = -2.7\text{ V}, I_D = -2.2\text{ A}$			0.152	0.2
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$				A	
			$V_{GS} = -2.7\text{ V}, V_{DS} = -5\text{ V}$	-10			
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -2.7\text{ A}$		6		S	
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		550		pF	
$C_{oss}$	Output Capacitance			260		pF	
$C_{rss}$	Reverse Transfer Capacitance			75		pF	
<b>SWITCHING CHARACTERISTICS</b> (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -5\text{ V}, I_D = -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns	
$t_r$	Turn - On Rise Time			40	60	ns	
$t_{D(off)}$	Turn - Off Delay Time			25	40	ns	
$t_f$	Turn - Off Fall Time			17	30	ns	
$Q_g$	Total Gate Charge	$V_{DS} = -5\text{ V}, I_D = -2.7\text{ A}, V_{GS} = -4.5\text{ V}$		8.7	15	nC	
$Q_{gs}$	Gate-Source Charge			1.7		nC	
$Q_{gd}$	Gate-Drain Charge			1.8		nC	

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$I_S$	Continuous Source Diode Current				-1.3	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.77	-1.2	V

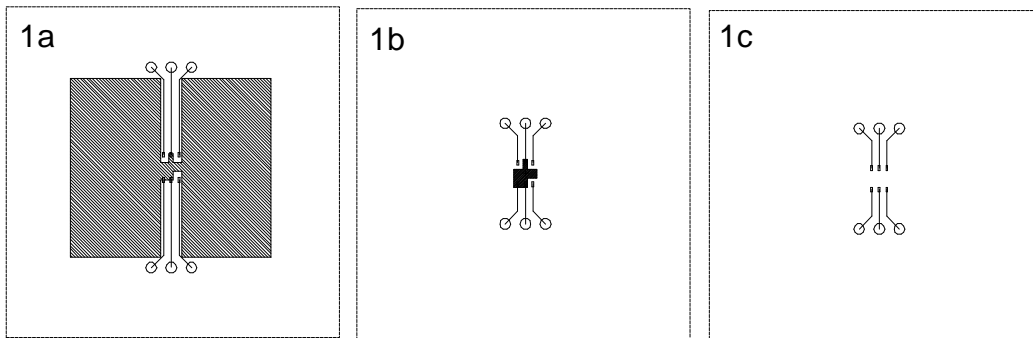
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J \theta A}(t)} = \frac{T_J - T_A}{R_{\theta J} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical  $R_{\theta JA}$  using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

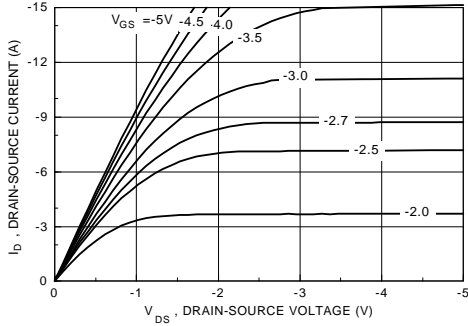
- 78°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- 125°C/W when mounted on a 0.01 in<sup>2</sup> pad of 2oz copper.
- 156°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



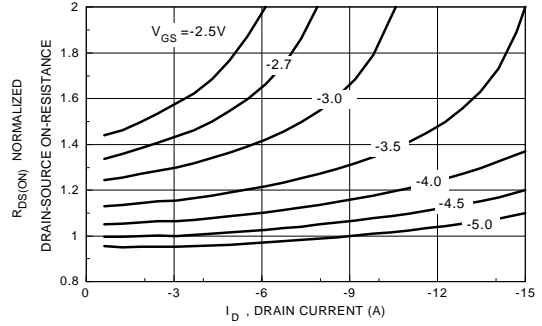
Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

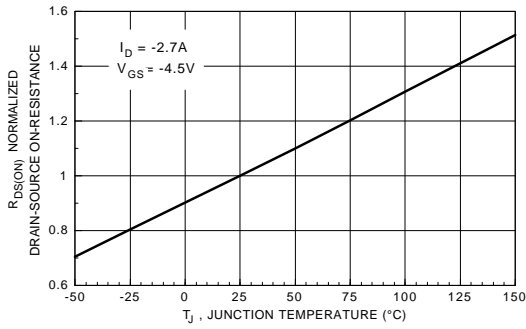
**Typical Electrical Characteristics**



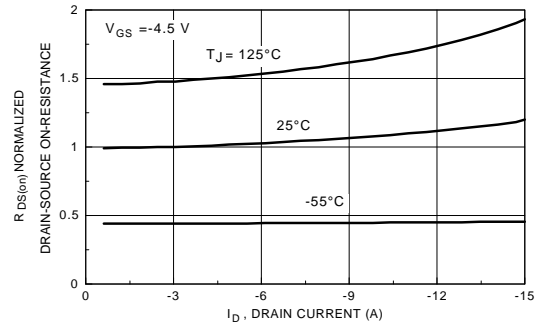
**Figure 1. On-Region Characteristics.**



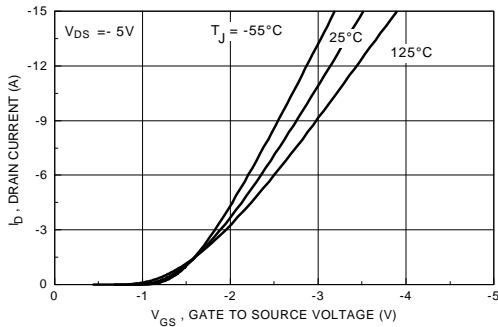
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



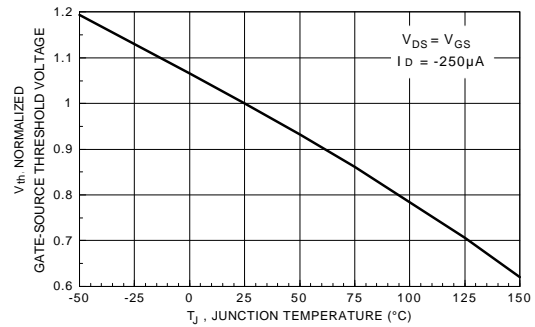
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Drain Current and Temperature.**

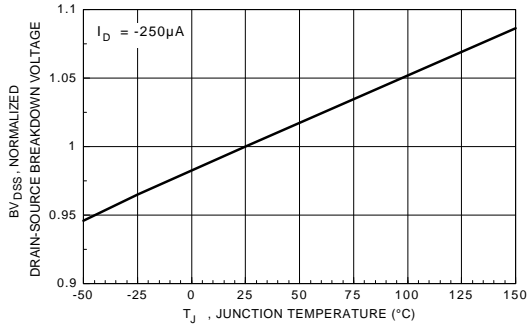


**Figure 5. Transfer Characteristics.**

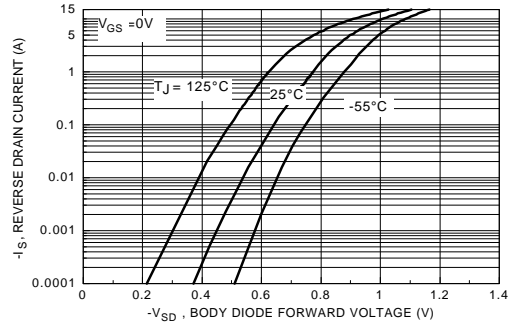


**Figure 6. Gate Threshold Variation with Temperature.**

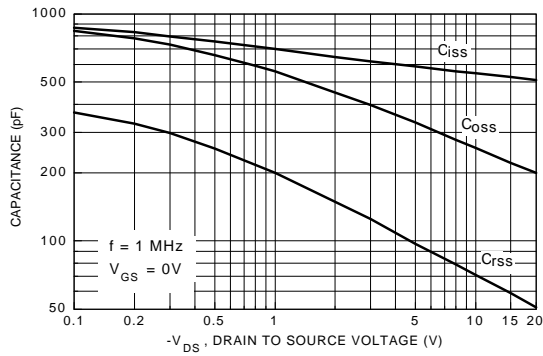
**Typical Electrical Characteristics (continued)**



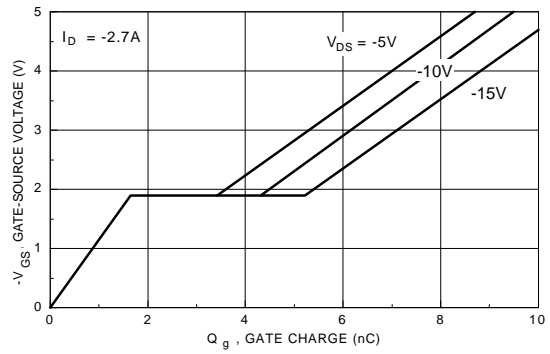
**Figure 7. Breakdown Voltage Variation with Temperature.**



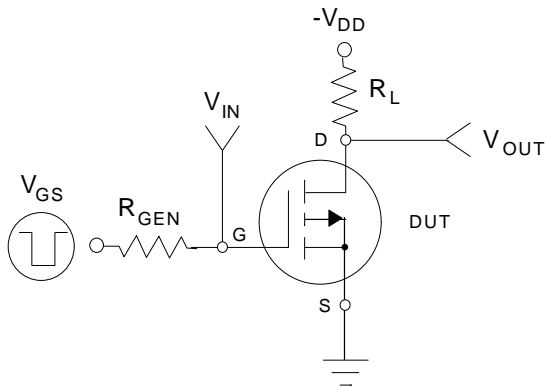
**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.**



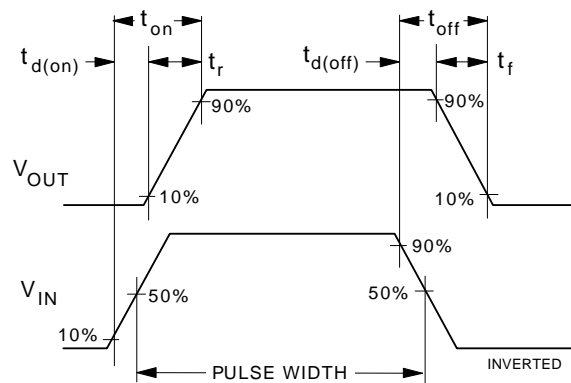
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**

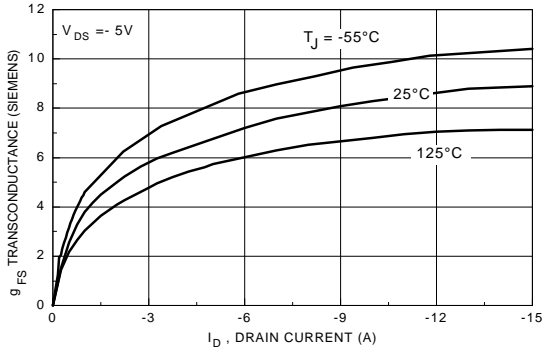


**Figure 11. Switching Test Circuit.**

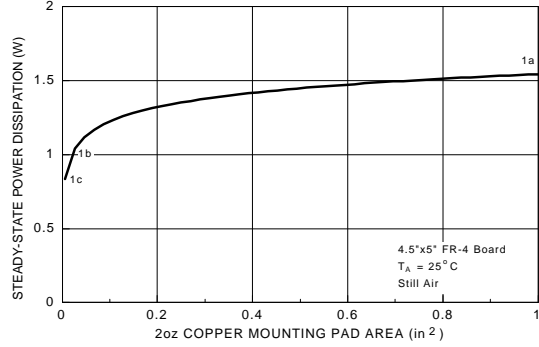


**Figure 12. Switching Waveforms.**

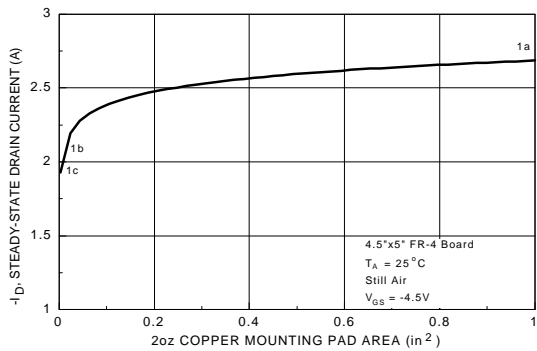
**Typical Electrical and Thermal Characteristics (continued)**



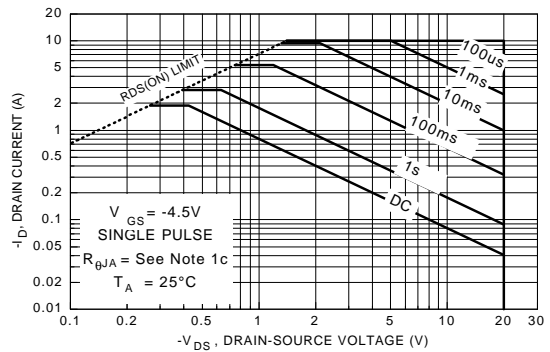
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



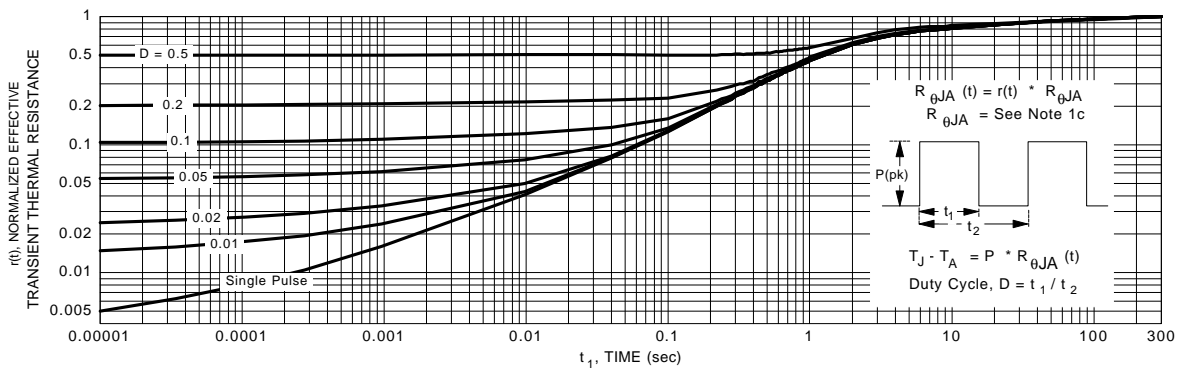
**Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 16. Maximum Safe Operating Area**



**Figure 17. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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