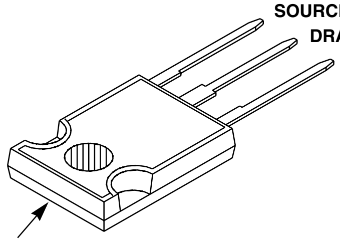
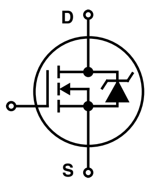
75A, 150V, 0.016 Ohm, N-Channel, UltraFET® Power MOSFET

Packaging

JEDEC TO-247



Symbol



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.016\Omega$, $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA75852G3	TO-247	75852G

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HUFA75852G3	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	150	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	150	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous ($T_C = 25^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15	
Power Dissipation	P_D	500	W
Derate Above 25^oC		3.33	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	^oC

NOTE:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
Reliability data can be found at: http://www.mtp.intersil.com/automotive.html.
All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 11)		150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 140V$, $V_{GS} = 0V$		-	-	1	μA
		$V_{DS} = 135V$, $V_{GS} = 0V$, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 75A$, $V_{GS} = 10V$ (Figure 9)		-	0.013	0.016	W
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-247		-	-	0.30	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	30	$^oC/W$
SWITCHING SPECIFICATIONS ($V_{GS} = 10V$)							
Turn-On Time	t_{ON}	$V_{DD} = 75V$, $I_D = 75A$ $V_{GS} = 10V$, $R_{GS} = 2.0\Omega$ (Figures 18, 19)		-	-	260	ns
Turn-On Delay Time	$t_{d(ON)}$			-	22	-	ns
Rise Time	t_r			-	151	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	82	-	ns
Fall Time	t_f			-	107	-	ns
Turn-Off Time	t_{OFF}			-	-	285	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 75V$, $I_D = 75A$, $I_{g(REF)} = 1.0mA$ (Figures 13, 16, 17)	-	400	480	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0V$ to $10V$		-	215	260	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $2V$		-	15	17.5	nC
Gate to Source Gate Charge	Q_{gs}			-	25	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	66	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 12)		-	7690	-	pF
Output Capacitance	C_{OSS}			-	1650	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	535	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75A$	-	-	1.25	V
		$I_{SD} = 35A$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75A$, $dI_{SD}/dt = 100A/\mu s$	-	-	260	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75A$, $dI_{SD}/dt = 100A/\mu s$	-	-	1830	nC

Typical Performance Curves

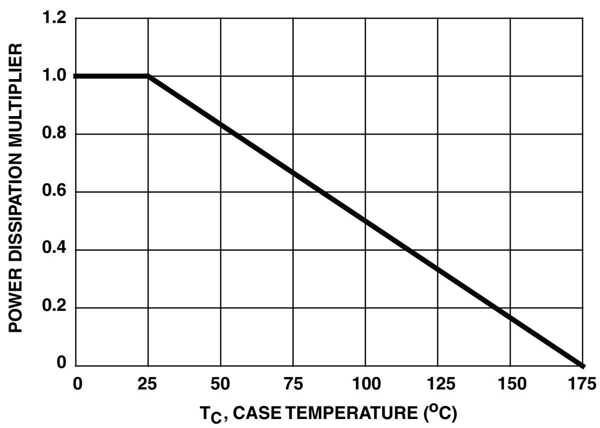


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

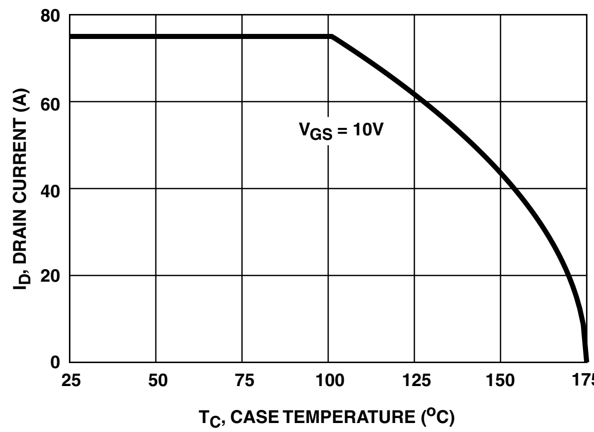


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

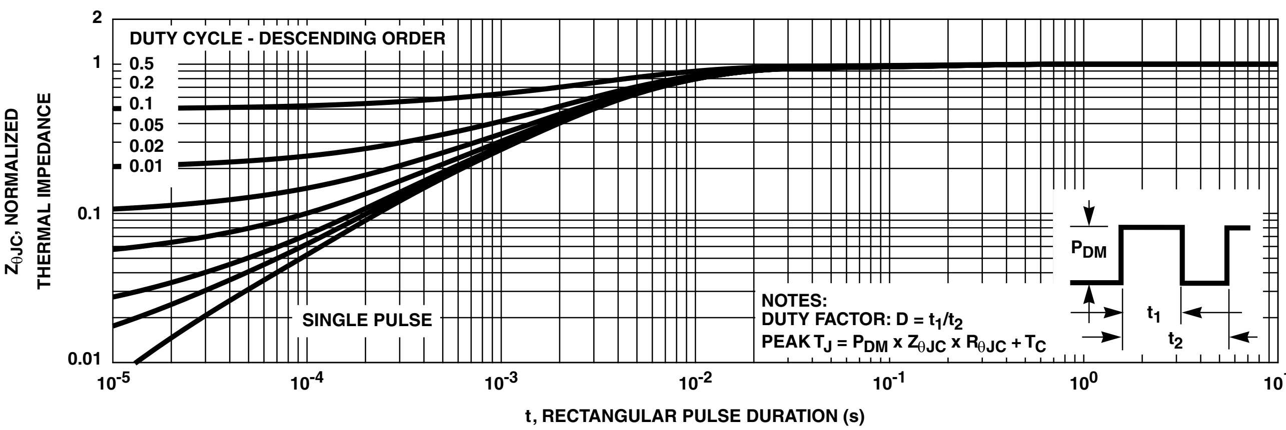


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

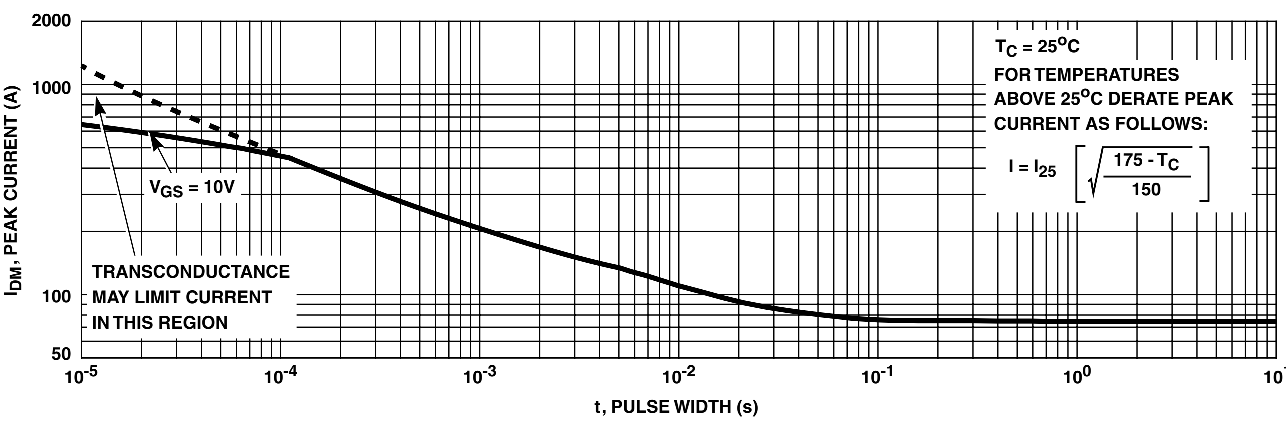


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

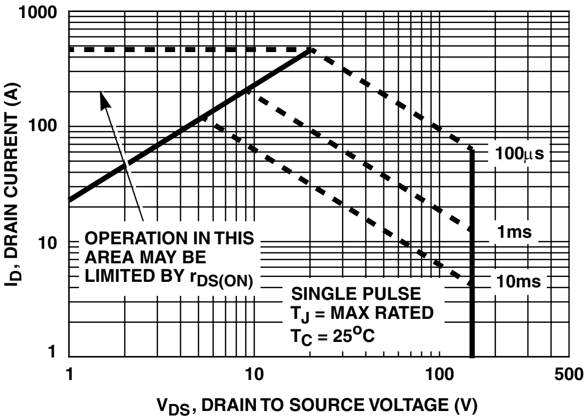
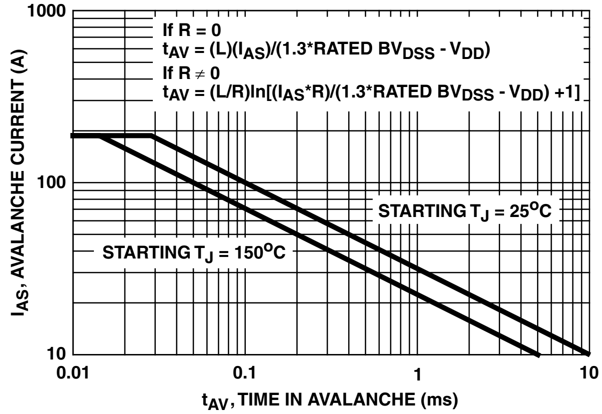


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

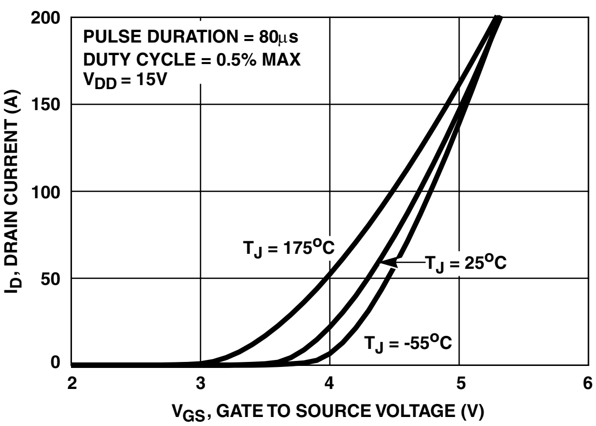


FIGURE 7. TRANSFER CHARACTERISTICS

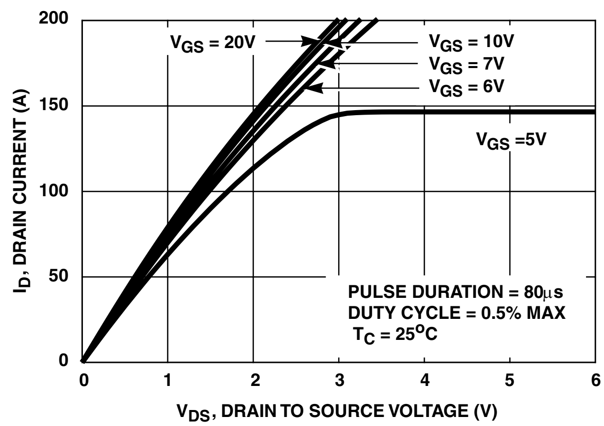


FIGURE 8. SATURATION CHARACTERISTICS

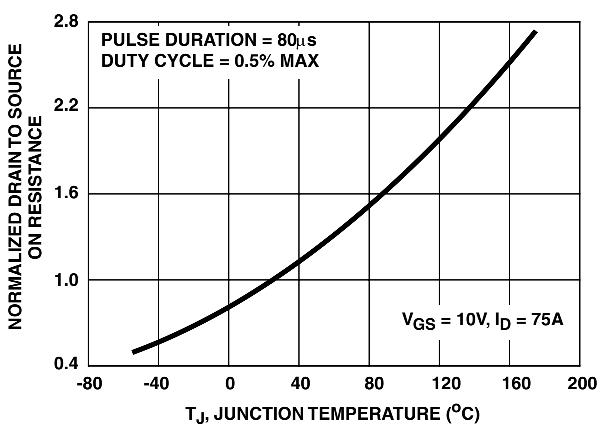


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

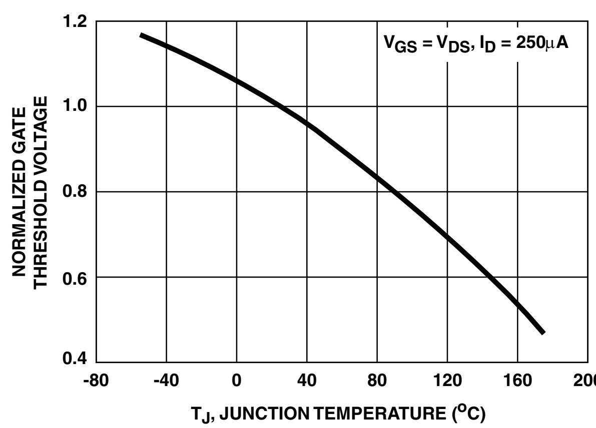


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

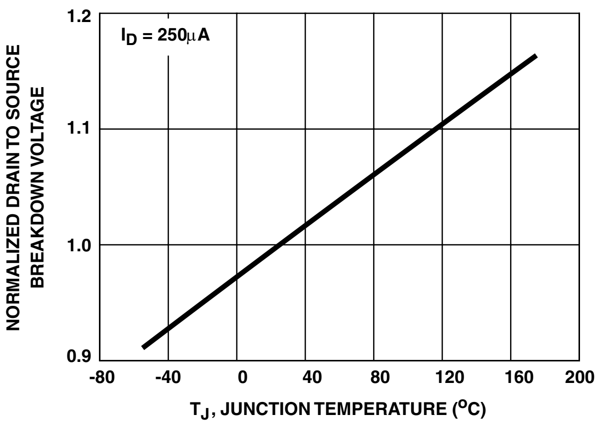


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

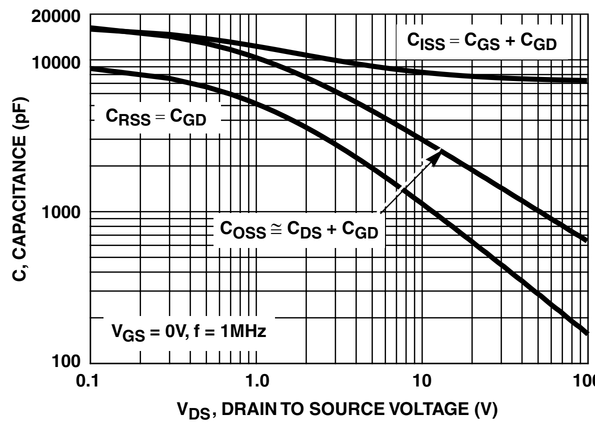
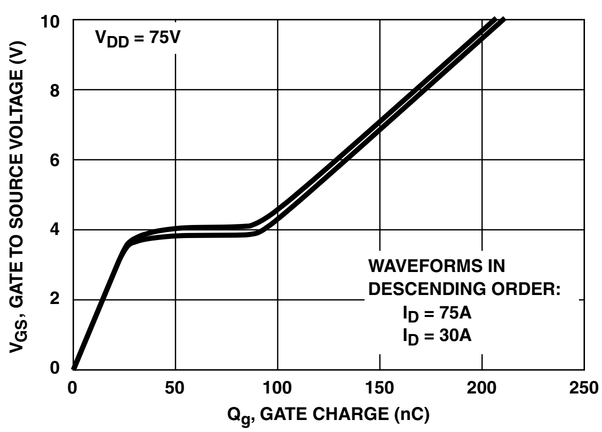


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

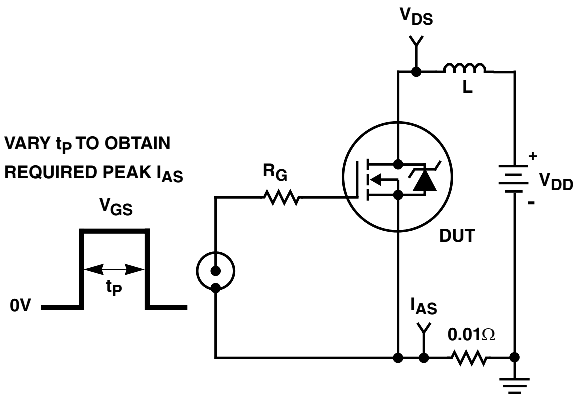


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

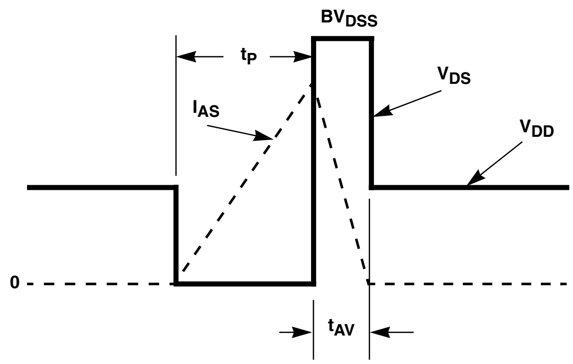


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

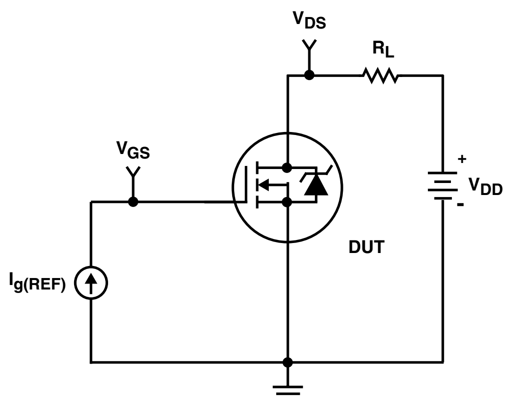


FIGURE 16. GATE CHARGE TEST CIRCUIT

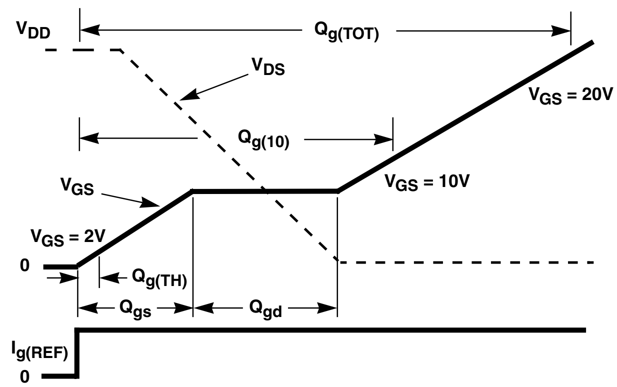


FIGURE 17. GATE CHARGE WAVEFORMS

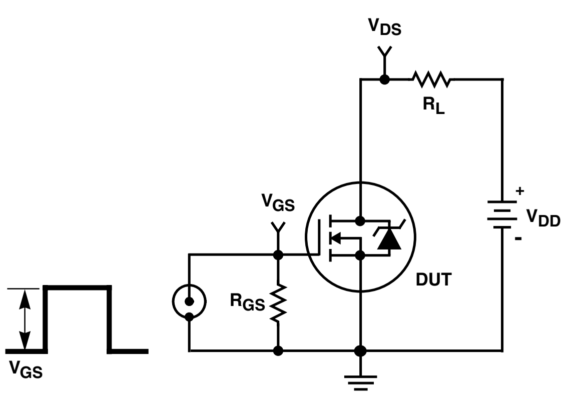


FIGURE 18. SWITCHING TIME TEST CIRCUIT

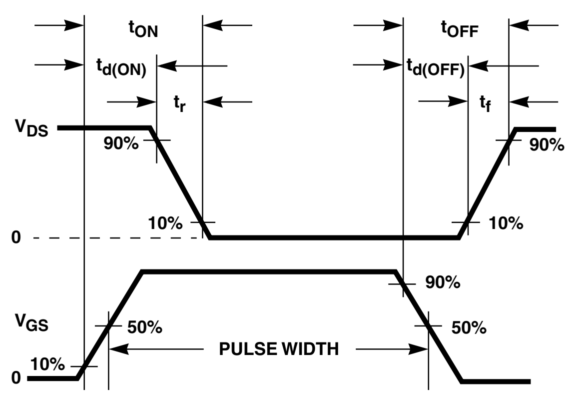
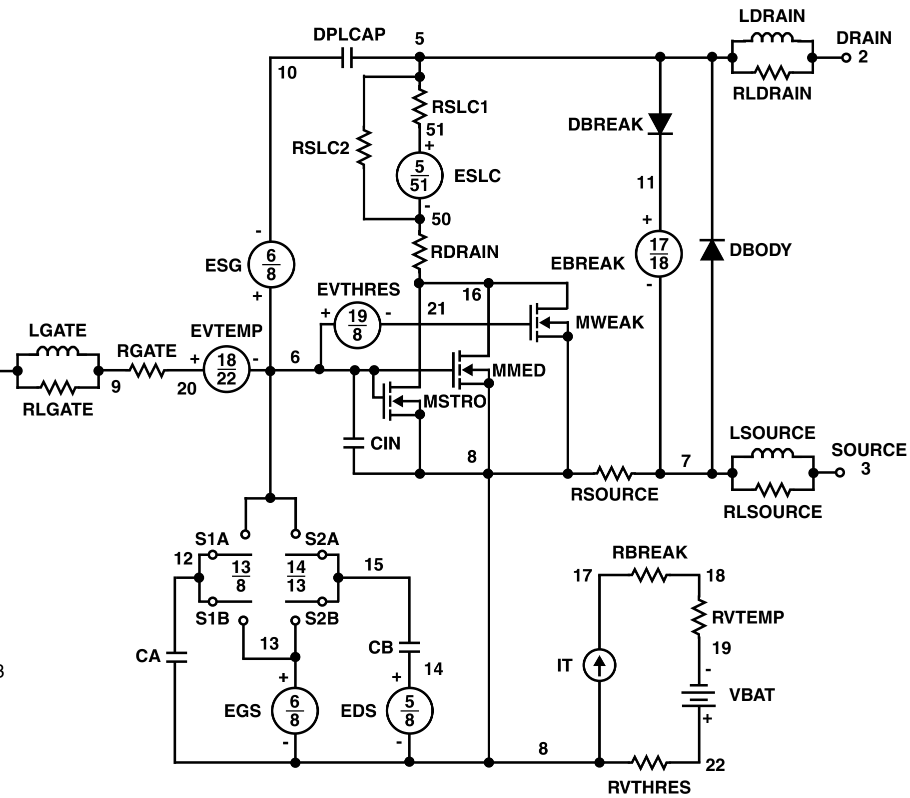


FIGURE 19. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUFA75852 2 1 3 ;   rev 26 Oct 1999



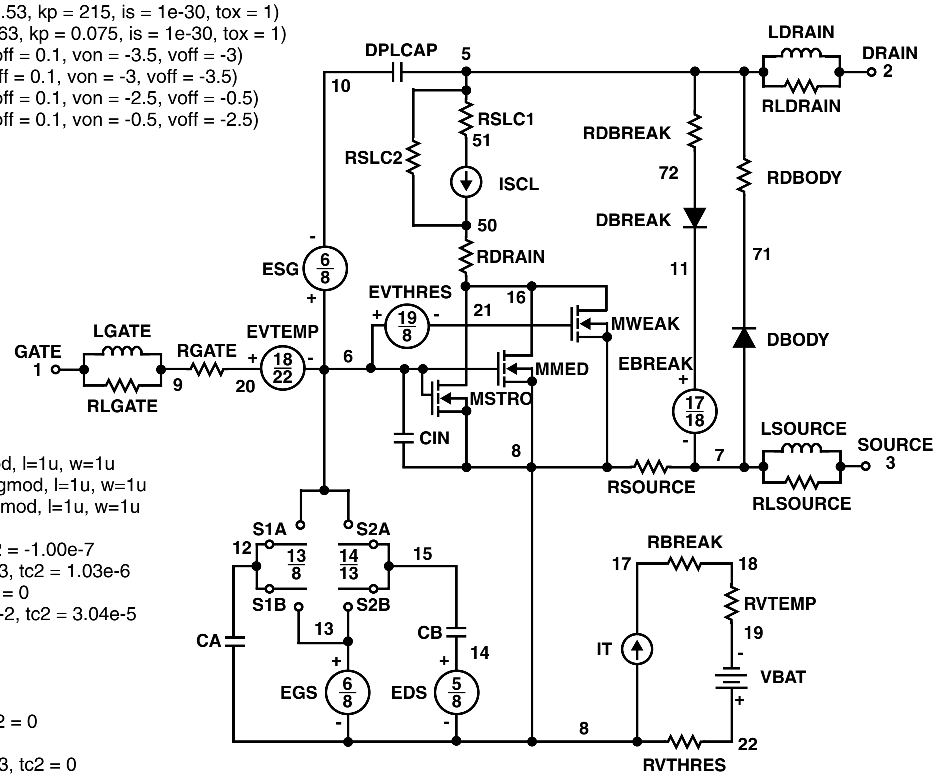

```
CA  12  8 12.0e-9
CB  15  14 12.0e-9
CIN  6  8 7.15e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 159.2
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1.0e-9
LGATE 1  9 7.46e-9
LSOURCE  3  7 3.87e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 9.50e-3
RGATE  9  20 0.80
RLDRAIN 2 5 10
RLGATE 1 9 74.6
RLSOURCE 3 7 38.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 2.37e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*245),2.5))}

.MODEL DBODYMOD D (IS = 6.03e-12 RS = 2.17e-3  TRS1 = 1.97e-3  TRS2 = 1.03e-6  CJO = 7.91e-9  TT = 1.69e-7 M = 0.60)
.MODEL DBREAKMOD D (RS = 3.53e-1  TRS1 = 0  TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 9.52e-9  IS = 1e-30  N = 1 M = 0.88)
.MODEL MMEDMOD NMOS (VTO = 3.05 KP = 8.50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.80)
.MODEL MSTROMOD NMOS (VTO = 3.53 KP = 215 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.63 KP = 0.075 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.0 )
.MODEL RBREAKMOD RES (TC1 = 1.12e-3  TC2 = -1.00e-7)
.MODEL RDRAINMOD RES (TC1 = 1.03e-2  TC2 = 3.04e-5)
.MODEL RSLCMOD RES (TC1 = 2.52e-3 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 1.01e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -3.65e-3 TC2 = -1.55e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.85e-3  TC2 = 0)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.5  VOFF= -3.0)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.0  VOFF= -3.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF= -0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.5  VOFF= -2.5)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 26 Oct 1999

```
template HUFA75852 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 6.03e-12, cjo = 7.91e-9, tt = 1.69e-7, m = 0.60)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 9.52e-9, is = 1e-30, n=1, m = 0.88 )
m..model mmedmod = (type=_n, vto = 3.05, kp = 8.50, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.53, kp = 215, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.63, kp = 0.075, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -3.5, voff = -3)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -3, voff = -3.5)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -2.5, voff = -0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = -0.5, voff = -2.5)

c.ca n12 n8 = 12.0e-9
c.cb n15 n14 = 12.0e-9
c.cin n6 n8 = 7.15e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9
l.lgate n1 n9 = 7.46e-9
l.lsource n3 n7 = 3.87e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.12e-3, tc2 = -1.00e-7
res.rdbody n71 n5 = 2.17e-3, tc1 = 1.97e-3, tc2 = 1.03e-6
res.rdbreak n72 n5 = 3.53e-1, tc1 = 0, tc2 = 0
res.rdrain n50 n16  = 9.50e-3, tc1 = 1.03e-2, tc2 = 3.04e-5
res.rgate n9 n20 = 0.80
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 74.6
res.rlsource n3 n7 = 38.7
res.rslc1 n5 n51  = 1e-6, tc1 = 2.52e-4, tc2 = 0
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2.37e-3, tc1 = 1.01e-3, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -2.85e-3, tc2 = 0
res.rvthres n22 n8  = 1, tc1 = -3.65e-3, tc2 = -1.55e-5

spe.ebreak n11 n7 n17 n18 = 159.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/245))** 2.5))
}
}
```



SPICE Thermal Model

REV 19 Oct 1999

HUFA75852T

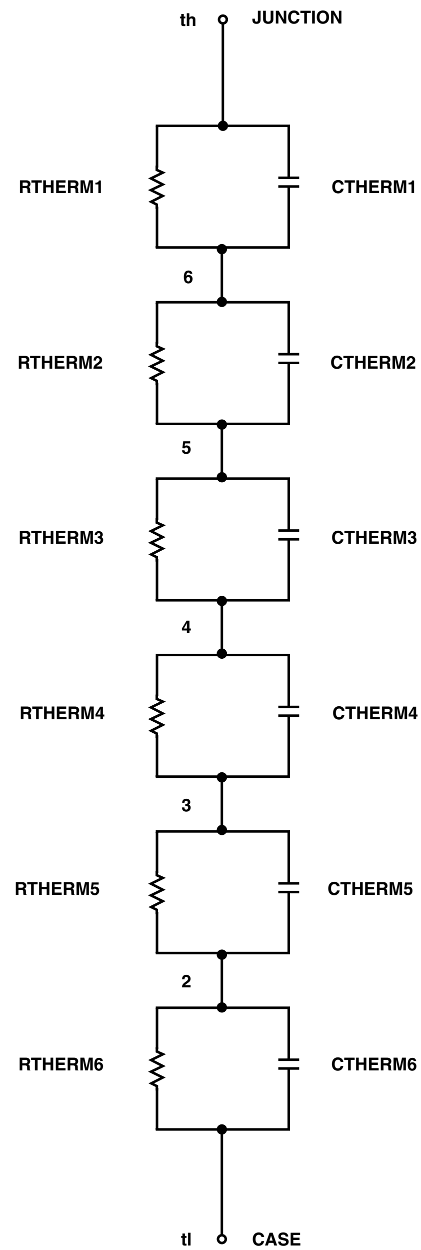
CTHERM1 th 6 9.75e-3
CTHERM2 6 5 3.90e-2
CTHERM3 5 4 2.50e-2
CTHERM4 4 3 2.95e-2
CTHERM5 3 2 6.55e-2
CTHERM6 2 tl 12.55

RTHERM1 th 6 1.96e-3
RTHERM2 6 5 4.89e-3
RTHERM3 5 4 1.38e-2
RTHERM4 4 3 7.73e-2
RTHERM5 3 2 1.17e-1
RTHERM6 2 tl 1.55e-2

SABER Thermal Model

SABER thermal model HUFA75852T

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 9.75e-3
ctherm.ctherm2 6 5 = 3.90e-2
ctherm.ctherm3 5 4 = 2.50e-2
ctherm.ctherm4 4 3 = 2.95e-2
ctherm.ctherm5 3 2 = 6.55e-2
ctherm.ctherm6 2 tl = 12.55

rtherm.rtherm1 th 6 = 1.96e-3
rtherm.rtherm2 6 5 = 4.89e-3
rtherm.rtherm3 5 4 = 1.38e-2
rtherm.rtherm4 4 3 = 7.73e-2
rtherm.rtherm5 3 2 = 1.17e-1
rtherm.rtherm6 2 tl = 1.55e-2
}
```



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FASTr™
GlobalOptoisolator™
GTO™
HiSeC™
ISOPLANAR™
LittleFET™
MicroFET™
MICROWIRE™
OPTOLOGIC™
OPTOPLANAR™
PACMAN™
POP™
PowerTrench ®
QFET™
QS™
QT Optoelectronics™
Quiet Series™
SILENT SWITCHER ®
SMART START™
Star* Power™
Stealth™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
UHC™
UltraFET™
VCX™

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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