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UCC2895MDWREP

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BiCMOS ADVANCED PHASE-SHIFT PWM CONTROLLER

Check for Samples: UCC2895-EP

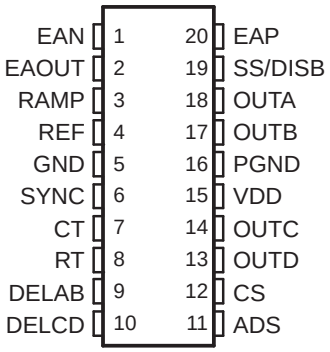
FEATURES

- **Programmable Output Turn-On Delay**
- **Adaptive Delay Set**
- **Bidirectional Oscillator Synchronization**
- **Capability for Voltage-Mode or Current-Mode Control**
- **Programmable Soft Start/Soft Stop and Chip Disable Via a Single Pin**
- **0% to 100% Duty-Cycle Control**
- **7-MHz Error Amplifier**
- **Operation to 1 MHz**
- **Low Active Current Consumption (5 mA Typ at 500 kHz)**
- **Very Low Current Consumption During Undervoltage Lock Out (150 µA Typ)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DW PACKAGE
(TOP VIEW)



(1) Additional temperature ranges available - contact factory

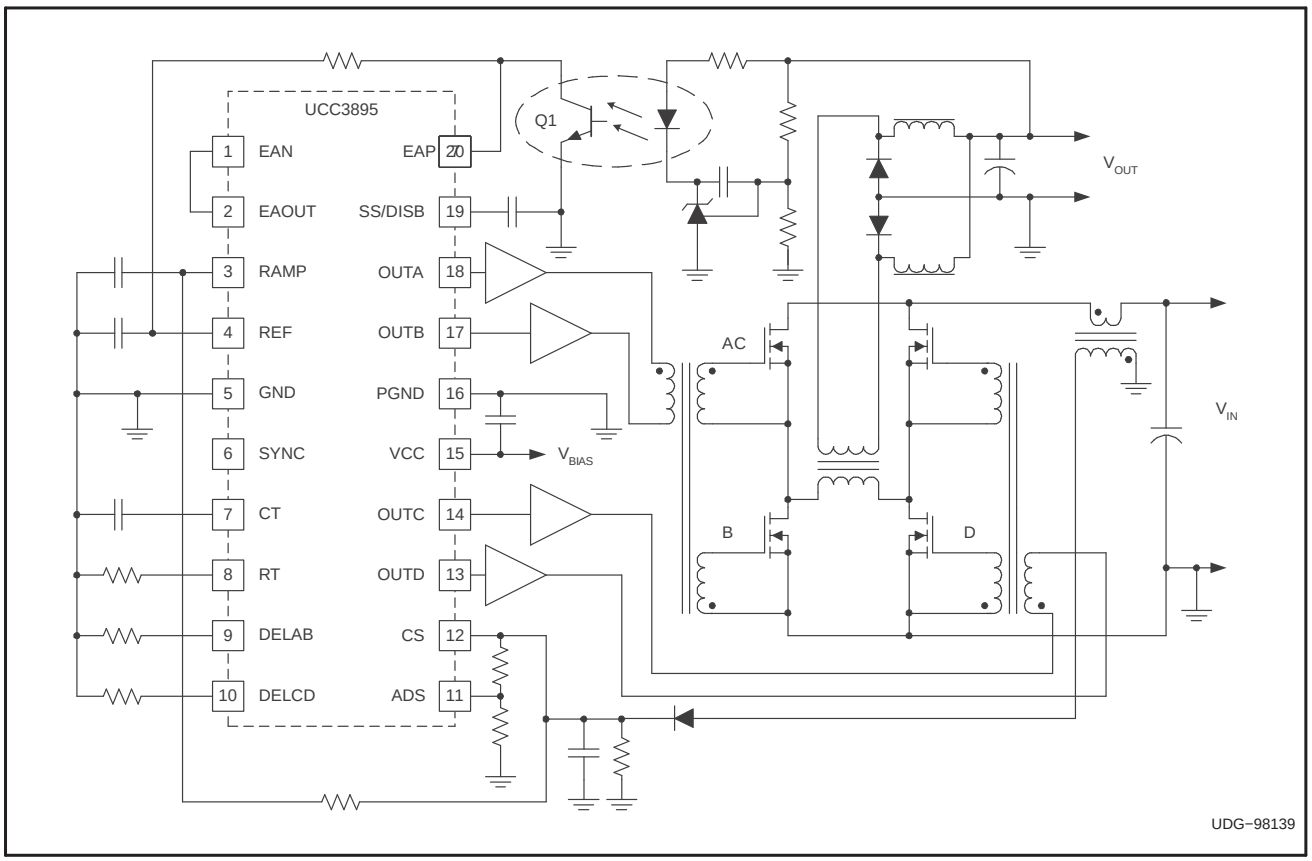
DESCRIPTION

The UCC2895-EP is a phase-shift pulse-width modulation (PWM) controller that implements control of a full-bridge power stage by phase shifting the switching of one half bridge with respect to the other. It allows constant frequency PWM in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The device can be used either as a voltage-mode or current-mode controller.

While the UCC2895-EP maintains the functionality of the UC2875/6/7/8 family, it improves on that controller family with additional features, such as enhanced control logic, adaptive delay set, and shutdown capability. Since the device is built in BCDMOS, it operates with dramatically less supply current than its bipolar counterparts. The UCC2895-EP can operate with a maximum clock frequency of 1 MHz.

The M-temp UCC2895-EP device is offered in the 20-pin SOIC (DW) package.

SIMPLIFIED APPLICATION DIAGRAM



ORDERING INFORMATION

T_A	PACKAGE (1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – DW	UCC2895MDWREP	UCC2895MEPG4

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Table 1. PIN DESCRIPTION

NAME	DESCRIPTION
ADS	Adaptive delay set.This function sets the ratio between the maximum and minimum programmed output delay dead time. When ADS is connected directly to CS, no delay modulation occurs. Maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2 V (the peak current threshold). ADS changes the output voltage on the delay (DELAB and DELCD) pins by: $$V_{DEL} = [0.75 \times (V_{CS} - V_{ADS})] + 0.5\ V$$ where V_{CS} and V_{ADS} are in volts. ADS must be limited to between 0 V and 2.5 V and must be less than, or equal to, CS. DELAB and DELCD also are clamped to a minimum of 0.5 V.
CS	Current sense. CS is the inverting input of the current-sense comparator, and the noninverting input of the overcurrent comparator and the ADS amplifier. The CS signal is used for cycle-by-cycle current limiting in peak current-mode control and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called soft stop, with full soft start.
CT	Oscillator timing capacitor (see Figure 3). The UCC2895-EP oscillator charges CT via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by: $$t_{OSC} = \frac{5 \times R_T \times C_T}{48} + 120\ ns$$ where CT is in farads, R_T is in ohms, and t_{OSC} is in seconds. C_T can range from 100 pF to 880 pF. Note that a large C_T and a small R_T combination results in extended fall times on the C_T waveform. The increased fall time increases the SYNC pulse width, thus, limiting the maximum phase shift between OUTA/ OUTB and OUTC/ OUTD outputs, which limits the maximum duty cycle of the converter.
DELAB, DELCD	Delay programming between complementary outputs. DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC2895-EP allows the user to select the delay in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half bridges to accommodate differences in resonant capacitor charging currents. The delay in each stage is set according to the formula: $$t_{DELAY} = \frac{(25 \times 10^{-12}) \times R_{DEL}}{V_{DEL}} + 25\ ns$$ where V_{DEL} is in volts, R_{DEL} is in ohms, and t_{DELAY} is in seconds. DELAB and DELCD can source approximately 1 mA maximum. Delay resistors must be chosen so that this maximum is not exceeded. Programmable output delay can be defeated by tying DELAB and/or DELCD to REF. For optimum performance, keep stray capacitance on these pins at <10 pF.
EAN	Error amplifier negative. Inverting input to the error amplifier. Keep below 3.6 V for proper operation.
EAOUT	Error amplifier output. EAOUT also is connected internally to the noninverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft-start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500 mV and allows the outputs to turn on again when EAOUT rises above 600 mV.
EAP	Error amplifier positive. Noninverting input to the error amplifier. Keep below 3.6 V for proper operation.
GND	Ground. Chip ground for all circuits except the output stages.
OUTA OUTB OUTC OUTD	Outputs. These outputs are 100-mA complementary MOS drivers and are optimized to drive FET driver circuits. OUTA and OUTB are fully complementary (assuming no programmed delay). They operate near 50% duty cycle and one-half the oscillating frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD drive the other half bridge and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB. Note that changing the phase relationship of OUTC and OUTD, with respect to OUTA and OUTB, requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients
PGND	Output stage ground. To keep output switching noise from critical analog circuits, the UCC2895-EP has two different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together closely near the IC. Also, since PGND carries high current, board traces must be low impedance.
RAMP	Inverting input of PWM comparator. RAMP receives either the C_T waveform in voltage and average current-mode controls, or the current signal (plus slope compensation) in peak current-mode control. An internal discharge transistor is provided on RAMP, which is triggered during the oscillator dead time.

Table 1. PIN DESCRIPTION (continued)

NAME	DESCRIPTION
RT	Oscillator timing resistor (see Figure 3). The oscillator in the UCC2895-EP operates by charging an external timing capacitor, CT, with a fixed current programmed by R_T. R_T current is calculated as: $$I_{RT}\,(A) = \frac{3\ V}{R_T\,(\Omega)}$$ R_T can range from 40 kΩ to 120 kΩ. Soft-start charging and discharging current also are programmed by I_{RT}.
REF	5 V ± 1.2% voltage reference. REF supplies power to internal circuitry, and also can supply up to 5 mA to external loads. The reference is shut down during undervoltage lockout, but is operational during all other disable modes. For best performance, bypass with a 0.1-µF low ESR, low ESL capacitor to ground. Do not use more than 1.0 µF.
SS/DISB	Soft start/disable. SS/DISB combines two independent functions: • Disable mode. A rapid shutdown of the chip is accomplished by any one of the following: externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, V_{DD} dropping below the UVLO threshold, or an overcurrent fault is sensed (CS = 2.5 V). In the case of REF pulled below 4 V or an UVLO condition, SS/DISB actively is pulled to ground via an internal MOSFET switch. If an overcurrent is sensed, SS/DISB sinks a current of 10 × I_{RT} until SS/DISB falls below 0.5 V. Note that, if SS/DISB is externally forced below 0.5 V, the pin starts to source current equal to I_{RT}. Also note that the only time the part switches into the low I_{DD} current mode is when the part is in undervoltage lockout. • Soft-start mode. After a fault or disable condition has passed and VDD is above the start threshold and/or SS/DISB falls below 0.5 V during a soft stop, SS/DISB switches to a soft-start mode. The pin now sources current equal to I_{RT}. A user-selected capacitor on SS/DISB determines the soft start and soft-start time. In addition, a resistor in parallel with the capacitor may be used, limiting the maximum voltage on SS/DISB. Note that SS/DISB actively clamps the EAOUT voltage to approximately the SS/DISB voltage during both soft-start, soft-stop, and disable conditions.
SYNC	Synchronization (see Figure 3). SYNC is bidirectional. When used as an output, SYNC can be used as a clock, which is the same as the chip's internal clock. When used as an input, SYNC overrides the chip's internal oscillator and acts as its clock signal. This bidirectional feature allows synchronization of multiple power supplies. SYNC also internally discharges the CT capacitor and any filter capacitors that are present on RAMP. The internal SYNC circuitry is level sensitive, with an input low threshold of 1.9 V and an input high threshold of 2.1 V. A resistor as small as 3.9 kΩ may be tied between SYNC and GND to reduce the synchronization pulse width.
VDD	Power supply. V_{DD} must be bypassed with a minimum of a 1.0-µF low ESR, low ESL capacitor to ground.

Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage	I_{DD} < 10 mA		17	V
	Supply current			30	mA
	REF current			15	mA
	OUT current			100	mA
	Analog inputs	EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB	–0.3	REF + 0.3	V
	Drive outputs	OUTA, OUTB, OUTC, OUTD	–0.3	to V_{CC} + 0.3	
	Power dissipation (at T_A = 25°C)	N package		1	W
		DW package		650	mW
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature range		–55	150	°C
	Lead temperature	Soldering, 10 s		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into and negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	10		16.5	V
C_{VDD}	Supply voltage bypass capacitor(2)		10 x C_{REF}		µF
C_{REF}	Reference bypass capacitor(3)	0.1		4.7	µF
C_T	Timing capacitor (for 500-KHz switching frequency)		200		pF
R_T	Timing resistor (for 500-KHz switching frequency)		82		
R_{DEL_AB} R_{DEL_CD}	Delay resistor	2.5		40	kΩ
T_J	Operating junction temperature(4)	–55		125	°C

(1) It is recommended that there be a single point grounded between GND and PGND directly under the device. There should be a seperate ground plane associated with the GND pin and all components associated with pins 1 through 12 plus 19 and 20 be located over this ground plane. Any connections associated with these pins to ground should be connected to this ground plane.
(2) The V_{DD} capacitor should be a low ESR, ESL ceramic capacitor located directly across the VDD and PGND pins. A larger bulk capacitor should belocated as physically close as possible to the VDD pins.
(3) The V_{REF} capacitor should be a low ESR, ESL ceramic capacitor located directly across the REF and GND pins. If a larger capacitor is desired for the V_{REF} then it should be located near the V_{REF} capacitor and connected to the VREF pin with a resistor of 51 Ω or greater. The bulk capacitor on VDD must be a factor of 10 greater than the total V_{REF} capacitance.
(4) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

Electrical Characteristics

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 1 µF, No load at outputs, $T_A = T_J$, T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO					
Start threshold		10.2	11	11.8	V
Stop threshold		8.2	9	9.8	V
Hysteresis		1	2	3	V
Supply Current					
Start-up current	V_{DD} = 8 V		150	250	µA
I_{DD} active			5	6	mA
V_{CC} clamp voltage	I_{DD} = 10 mA	16.5	17.5	18.5	V
Voltage Reference					
Output voltage	T_J = 25°C	4.94	5	5.06	V
	10 V < V_{DD} < 17.5 V, 0 mA < I_{REF} < 5 mA	4.85	5	5.15	
Short-circuit current	REF = 0 V, T_J = 25°C	10	20		mA
Error Amplifier					
Common-mode input voltage		–0.1		3.6	V
Offset voltage		–7		7	mV
Input bias current (EAP, EAN)		–1		1	µA
EAOUT V_{OH}	EAP–EAN = 500 mV, I_{EAOUT} = –0.5 mA	4	4.5	5	V
EAOUT V_{OL}	EAP–EAN = 500 mV, I_{EAOUT} = 0.5 mA	0	0.2	0.4	V
EAOUT source current	EAP–EAN = 500 mV, EAOUT = 2.5 V	1	1.5		mA
EAOUT sink current	EAP–EAN = –500 mV, EAOUT = 2.5 V	2.5	4.5		mA
Open-loop DC gain		75	85		dB
Unity gain bandwidth(1)		5	7		MHz
Slew rate	EAN from 1 V to 0 V, EAP = 500 mV, EAOUT from 0.5 V to 3 V(1)	1.5	2.2		V/µs
No-load comparator turn-off threshold		0.45	0.5	0.55	V
No-load comparator turn-on threshold		0.55	0.6	0.69	V
No-load comparator hysteresis		0.035	0.1	0.165	V

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 1 µF, No load at outputs, $T_A = T_J$, T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator					
Frequency	T_J = 25°C	473	500	527	kHz
Total variation	Line, Temperature(1)		2.5	5	%
SYNC V_{IH}		2.05	2.1	2.32	V
SYNC V_{IL}		1.85	1.9	1.95	V
SYNC V_{OH}	I_{SYNC} = –400 µA, C_T = 2.6 V	4.1	4.5	5	V
SYNC V_{OL}	I_{SYNC} = 100 µA, C_T = 0 V	0	0.5	1	V
SYNC output pulse width	SYNC load = 3.9 kΩ and 30 pF in parallel		85	135	ns
R_T voltage		2.9	3	3.1	V
C_T peak voltage		2.25	2.35	2.55	V
C_T valley voltage		0	0.2	0.65	V
PWM Comparator					
EAOUT to RAMP/input offset voltage	RAMP = 0 V, DELAB = DELCD = REF	0.72	0.85	1.05	V
Minimum phase shift (OUTA to OUTC, OUTB to OUTD)	RAMP = 0 V, EAOUT = 650 mV(2)	0	0.85	1.50	%
RAMP to OUTC/OUTD delay	RAMP from 0 V to 2.5 V, EAOUT = 1.2 V, DELAB = DELCD = REF(3)		70	120	ns
RAMP bias current	RAMP < 5 V, C_T < 2.2 V	–5		5	µA
RAMP sink current	RAMP = 5 V, C_T < 2.6 V	12	19		mA
Current Sense					
CS bias current	0 < CS< 2.5 V, 0 < ADS < 2.5 V	–4.5		20	µA
Peak current threshold		1.9	2	2.1	V
Overcurrent threshold		2.4	2.5	2.6	V
CS to output delay	CS from 0 to 2.3 V, DELAB = DELCD = REF		75	110	ns
Soft Start/Shutdown					
Soft-start source current	SS/DISB = 3 V, CS = 1.9 V	–40	–35	–30	µA
Soft-start sink current	SS/DISB = 3 V, CS = 2.6 V	325	350	375	µA
Soft-start/disable comparator threshold		0.44	0.5	0.56	V
Delay Set					
DELAB/DELCD output voltage	ADS = CS = 0 V	0.45	0.5	0.55	V
	ADS = 0 V, CS = 2 V	1.9	2	2.1	V
Output delay	ADS = CS = 0 V(3) (4)	450	525	600	ns
ADS bias current	0 V < ADS < 2.5 V, 0 V < CS < 2.5 V	–20		20	µA

(2) Minimum phase shift is defined as:

$$\Phi = 200 \times \frac{t_{f(OUTA)} - t_{f(OUTC)}}{t_{PERIOD}} \text{ or}$$

$$\Phi = 200 \times \frac{t_{f(OUTB)} - t_{f(OUTD)}}{t_{PERIOD}}$$

where:
$t_{f(OUTA)}$ = falling edge of OUTA signal
$t_{f(OUTB)}$ = falling edge of OUTB signal
$t_{f(OUTC)}$ = falling edge of OUTC signal
$t_{f(OUTD)}$ = falling edge of OUTD signal
$t_{(PERIOD)}$ = period of OUTA or OUTB signal

(3) Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is shown in Figure 1 and Figure 2 , where:
$t_{f(OUTA)}$ = falling edge of OUTA signal
$t_{r(OUTB)}$ = rising edge of OUTB signal

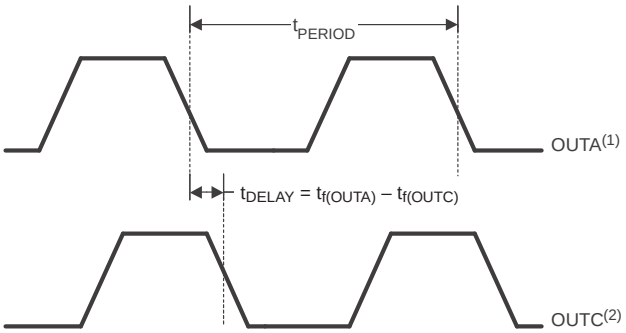
(4) Specified by design. Not production tested.

Electrical Characteristics (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 1 µF, No load at outputs, $T_A = T_J$, T_A = –55°C to 125°C (unless otherwise noted)

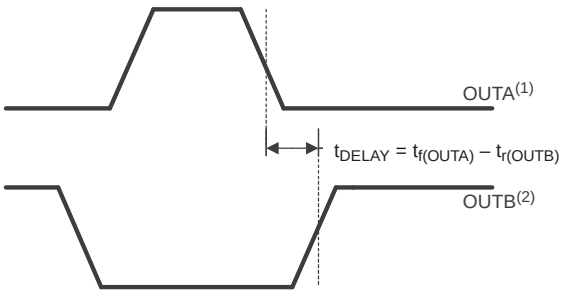
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output					
V_{OH} (all outputs)	I_{OUT} = –10 mA, V_{DD} to output		250	400	mV
V_{OL} (all outputs)	I_{OUT} = 10 mA		150	270	mV
Rise time	C_{LOAD} = 100 pF(5)		20	35	ns
Fall time	C_{LOAD} = 100 pF(5)		20	35	ns

(5) Specified by design. Not production tested.



(1) Also applies to OUTB
(2) Also applies to OUTD

Figure 1. OUTA/OUTC Output Delay



(1) Also applies to OUTC
(2) Also applies to OUTD

Figure 2. OUTA/OUTB Output Delay

APPLICATION INFORMATION

Programming DELAB, DELCD, and Adaptive Delay Set (ADS)

The UCC2895-EP allows the user to set the delay between switch commands within each leg of the full-bridge power circuit, according to the formula from the data sheet:

$$t_{DELAY} = \frac{(25 \times 10^{-12}) \times R_{DEL}}{V_{DEL}} + 25\ ns$$

For this equation, V_{DEL} is determined in conjunction with the desire to utilize (or not utilize) the ADS feature from:

$$V_{DEL} = [0.75 \times (V_{CS} - V_{ADS})] + 0.5\ V$$

Figure 3 shows the resistors needed to program the delay periods and the ADS function.

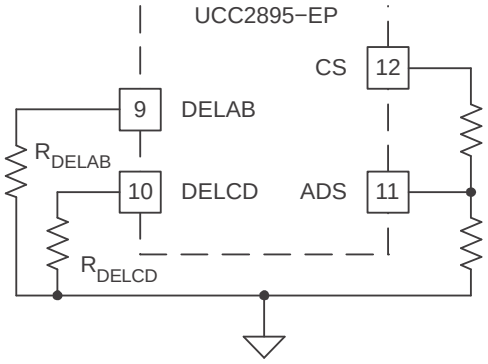


Figure 3. Resistors Needed in Programming

The ADS allows the user to vary the delay times between switch commands within each of the converter's two legs. The delay-time modulation is implemented by connecting ADS (pin 11) to CS, GND, or a resistive divider from CS to GND to set V_{ADS}. From the previous equation for V_{DEL}, if ADS is tied to GND, V_{DEL} rises in direct proportion to V_{CS}, causing a decrease in t_{DELAY} as the load increases. In this condition, the maximum value of V_{DEL} is 2 V. If ADS is connected to a resistive divider between CS and GND, the term (V_{CS} – V_{DS}) becomes smaller, reducing the level of V_{DEL}. This decreases the amount of delay modulation. In the limit of ADS tied to CS, V_{DEL} = 0.5 V and no delay modulation occurs. In the case with maximum delay modulation (ADS = GND) when the circuit goes from light load to heavy load, the variation of V_{DEL} is from 0.5 V to 2 V. This causes the delay times to vary by a 4:1 ratio as the load is changed.

The ability to program an adaptive delay is a desirable feature because the optimum delay time is a function of the current flowing in the primary winding of the transformer, and can change by a factor of 10:1 or more as circuit loading changes. Reference [1] delves into the many interrelated factors for choosing the optimum delay times for the most efficient power conversion and illustrates an external circuit to enable ADS using the UC2879. Implementing this adaptive feature is simplified in the UCC2895-EP controller, giving the user the ability to tailor the delay times to suit a particular application, with a minimum of external parts.

[1] L. Balogh, "Design Review: 100W, 400 kHz, DC/DC Converter With Current Doubler Synchronous Rectification Achieves 92% Efficiency," Unitrode Power Supply Design Seminar Manual, Unitrode Corporation, 1996, Topic 2.

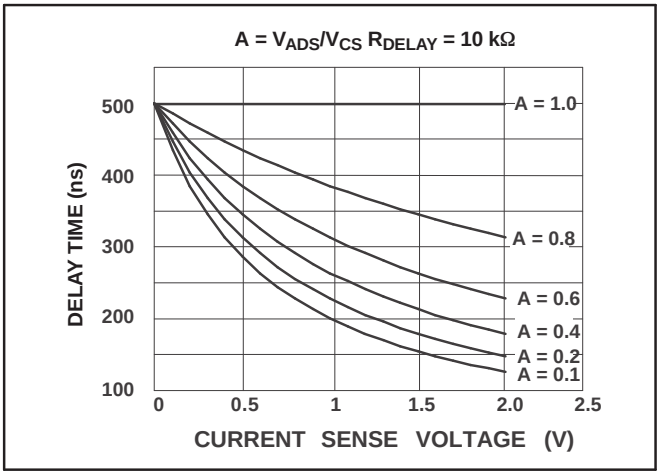


Figure 4. Resistors Needed for Programming

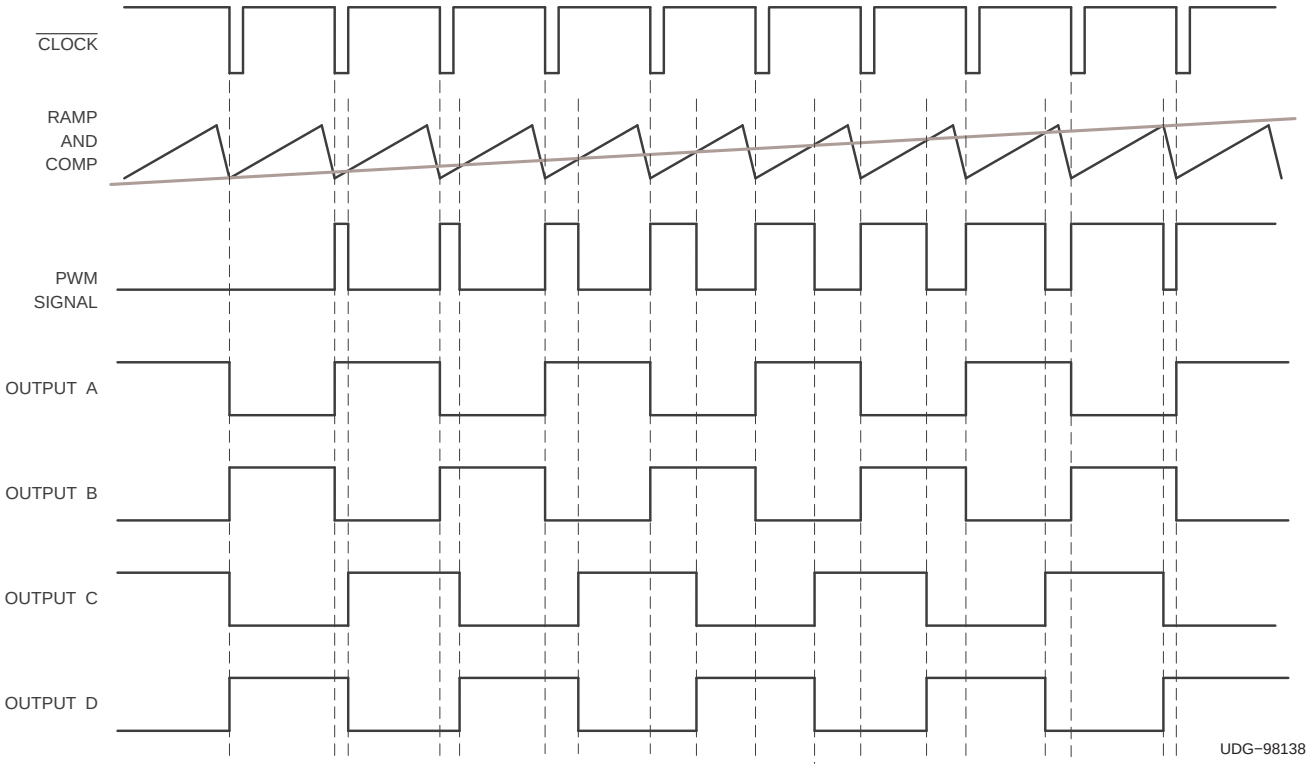


Figure 5. UCC2895-EP Timing (No Output Delay Shown)

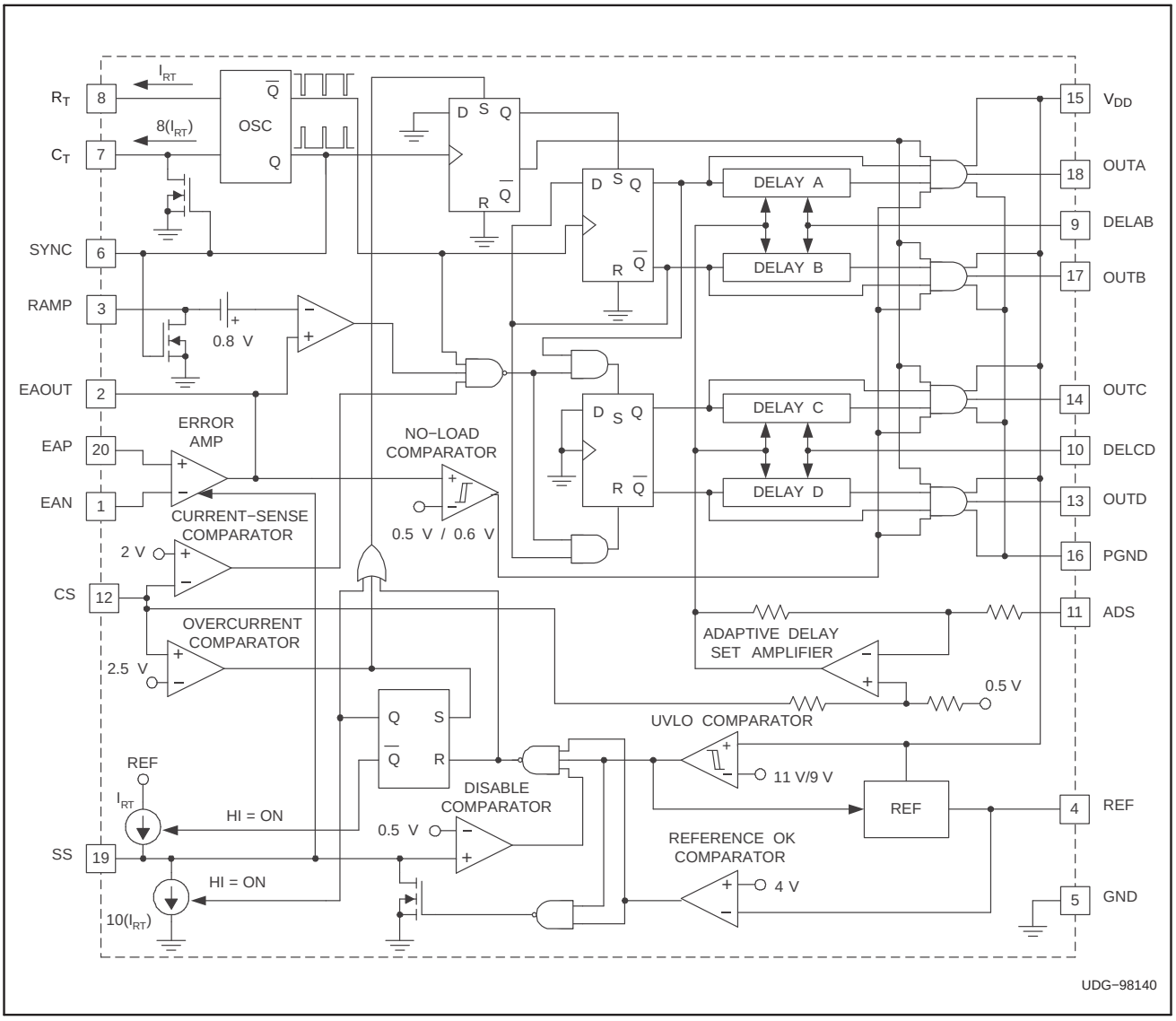


Figure 6. Block Diagram

CIRCUIT DESCRIPTION

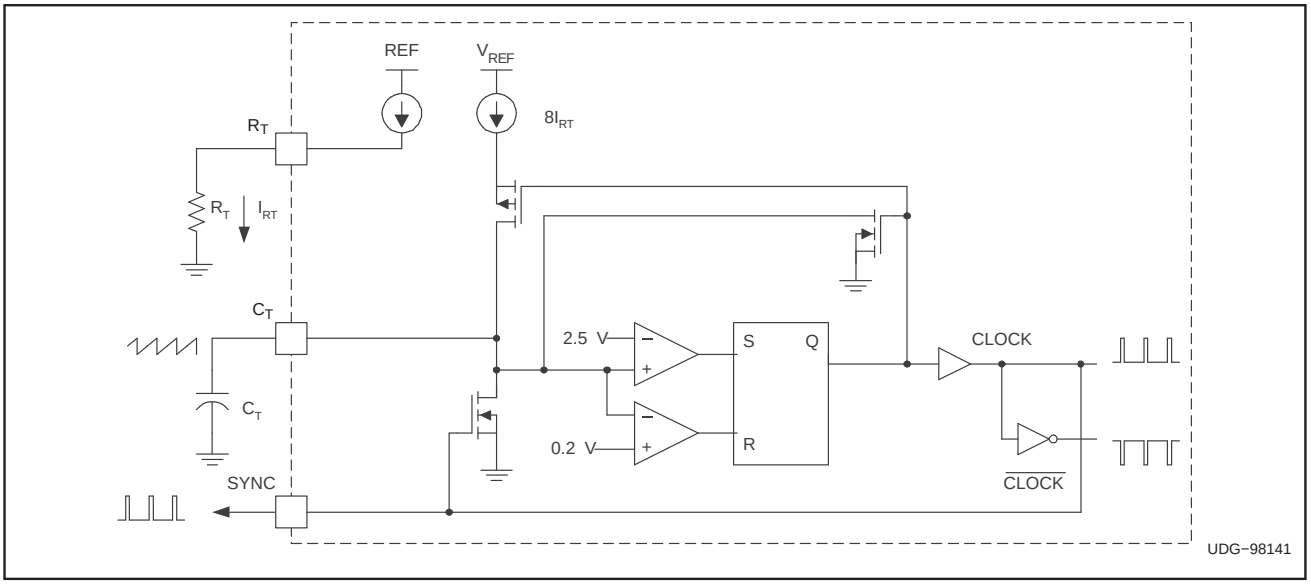


Figure 7. Oscillator Block Diagram

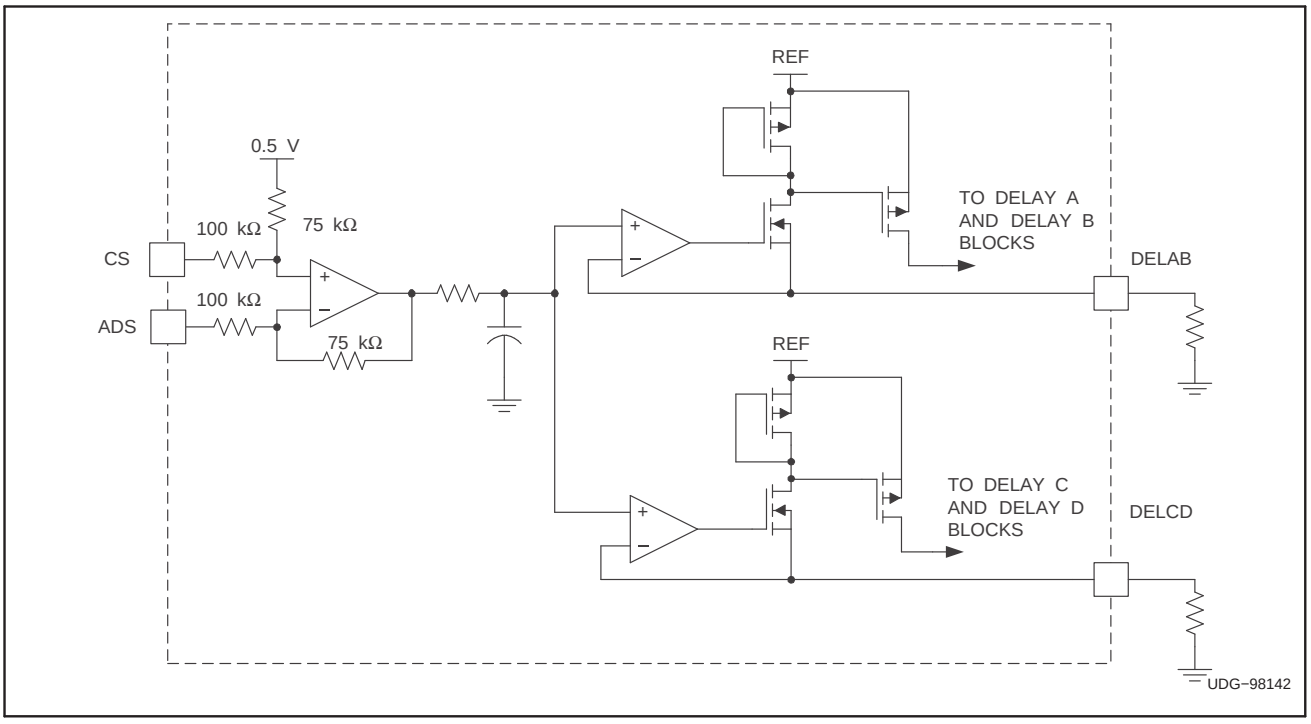


Figure 8. ADS Block Diagram

CIRCUIT DESCRIPTION (continued)

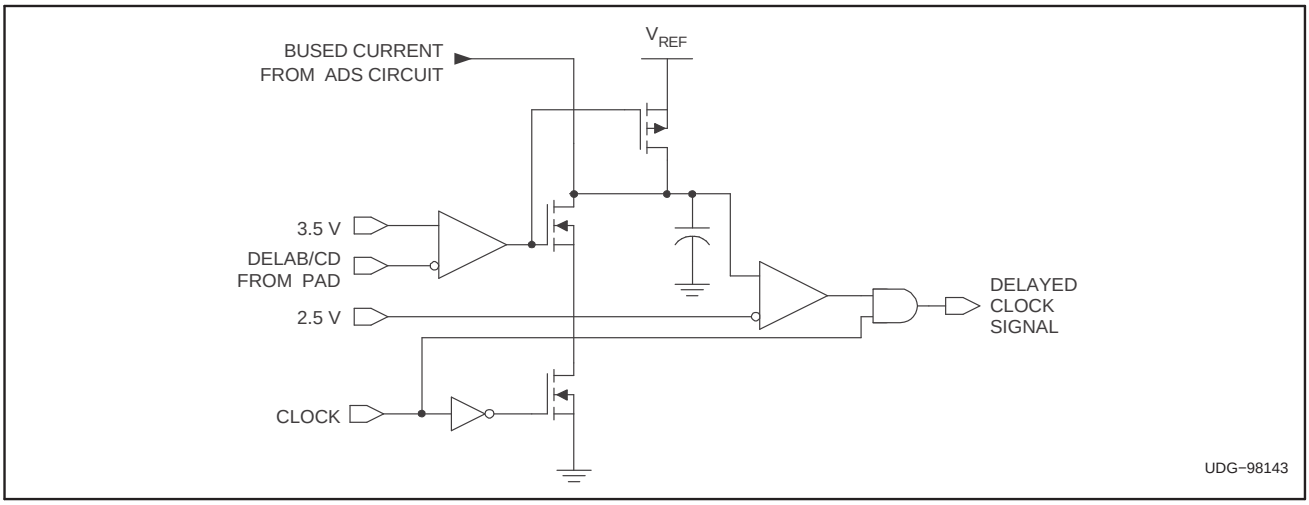


Figure 9. Delay Block Diagram (One Delay Block Per Output)

TYPICAL CHARACTERISTICS

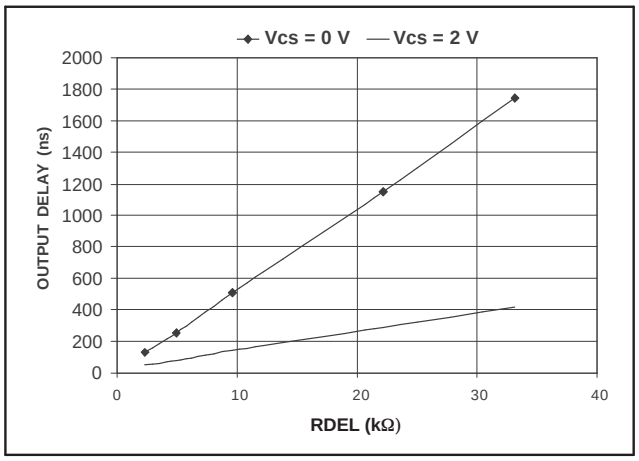


Figure 10. Delay Programming (Characterizes Output Delay Between A/B, C/D)

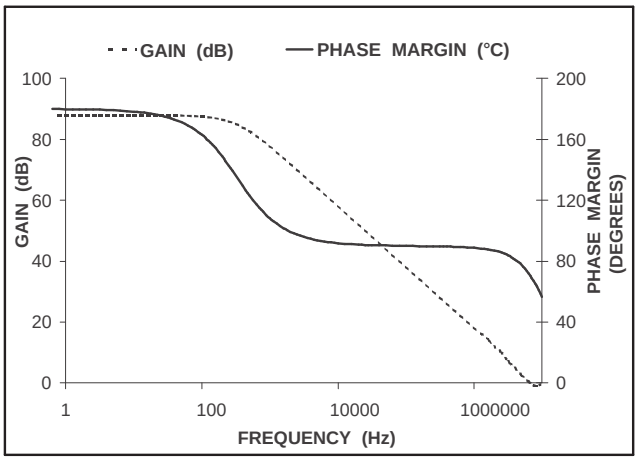


Figure 11. Error Amplifier Gain/Phase Margin

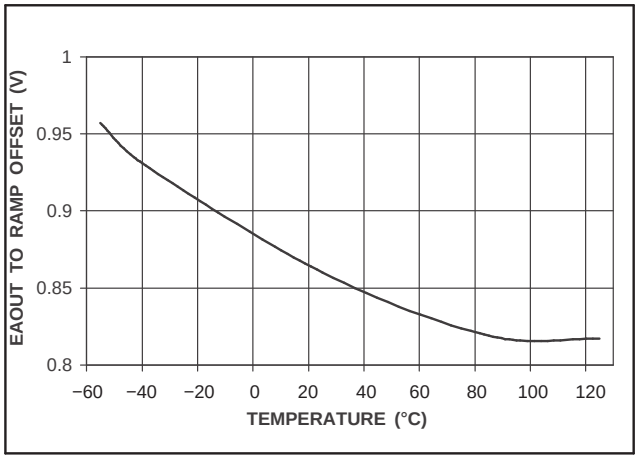


Figure 12. EAOUT to RAMP Offset Over Temperature

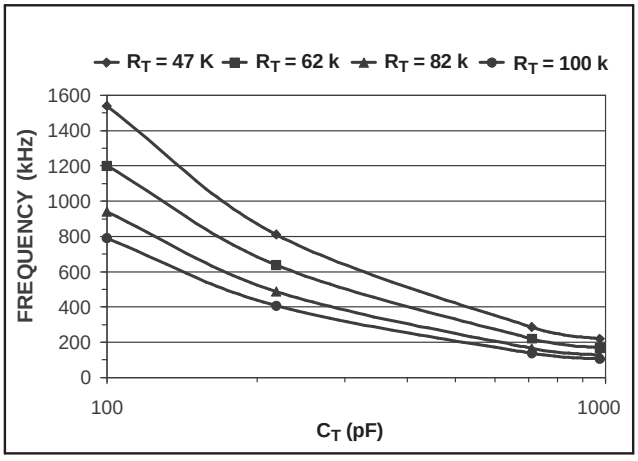


Figure 13. Frequency vs R_T/C_T (Oscillator Frequency)

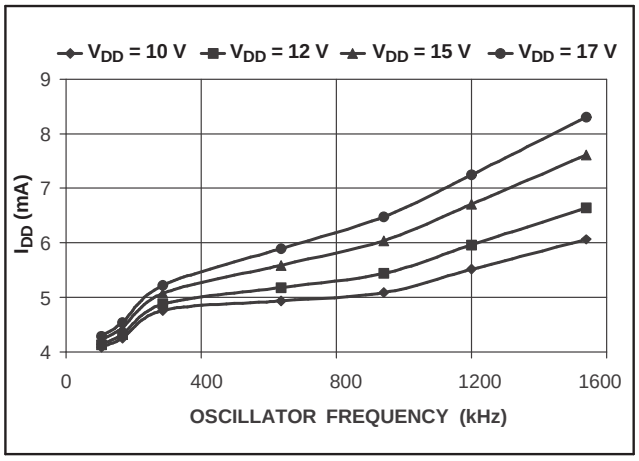


Figure 14. I_{DD} vs V_{DD}/Oscillator Frequency (No Output Loading)

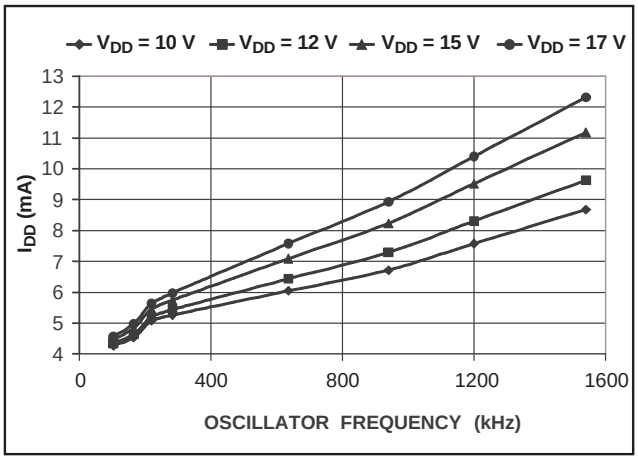


Figure 15. I_{DD} vs V_{DD}/Oscillator Frequency (With 0.1-nf Output Loads)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2895MDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCC2895MEP	Samples
V62/06614-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCC2895MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC2895-EP :

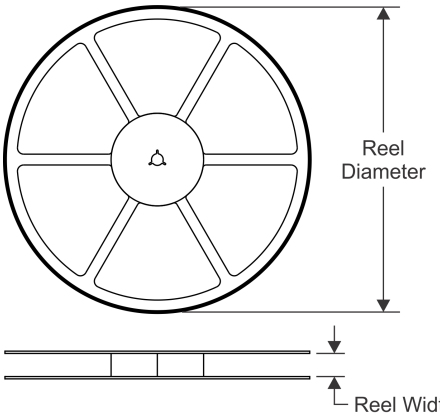
- Catalog: UCC2895
- Automotive: UCC2895-Q1

NOTE: Qualified Version Definitions:

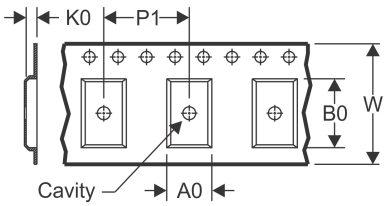
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

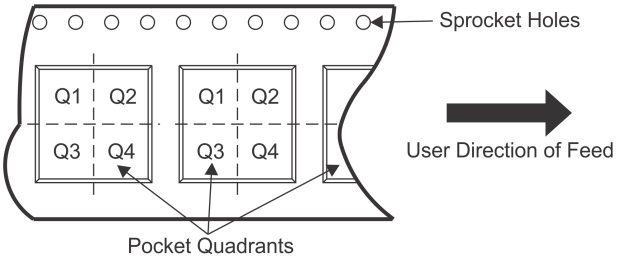


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

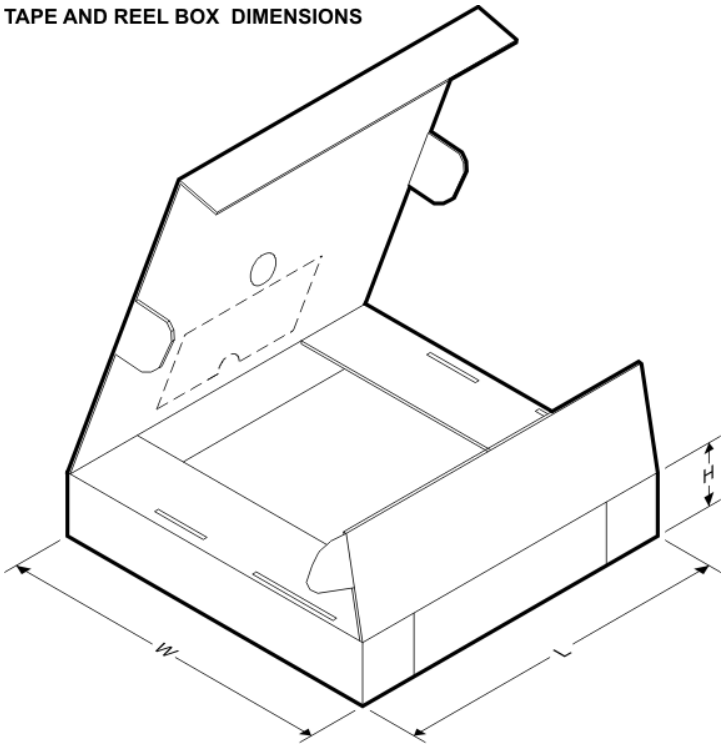


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2895MDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

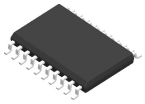
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2895MDWREP	SOIC	DW	20	2000	346.0	346.0	41.0

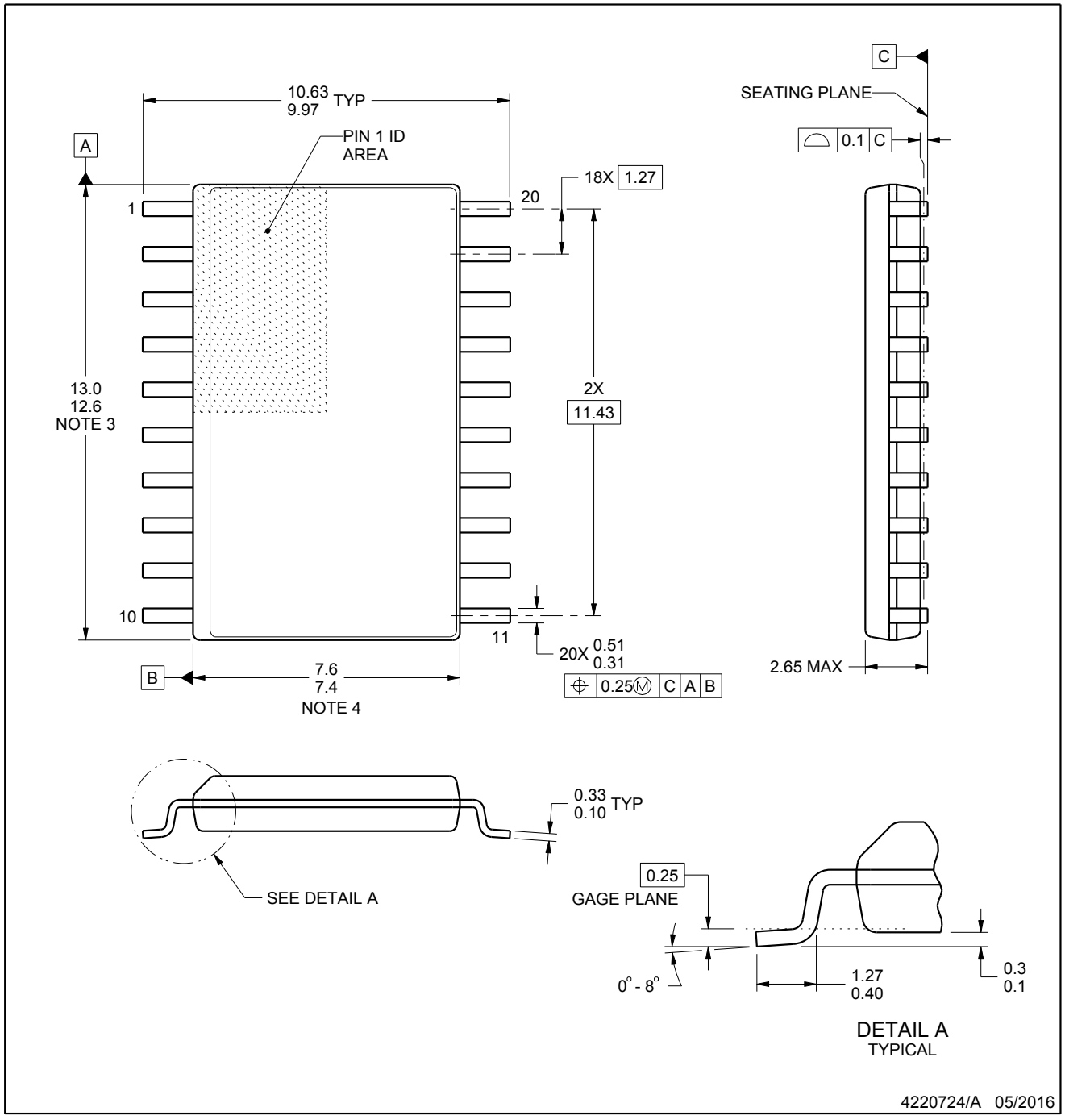


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

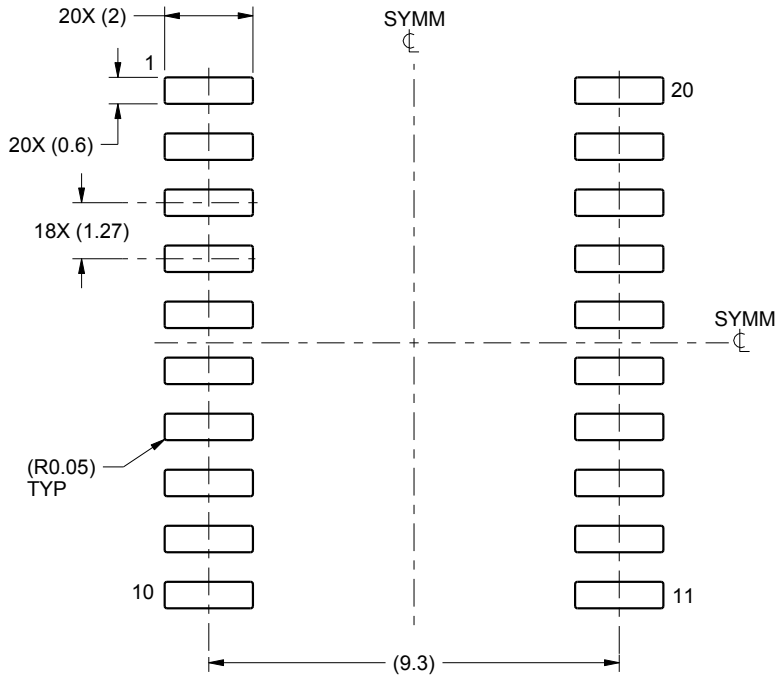
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

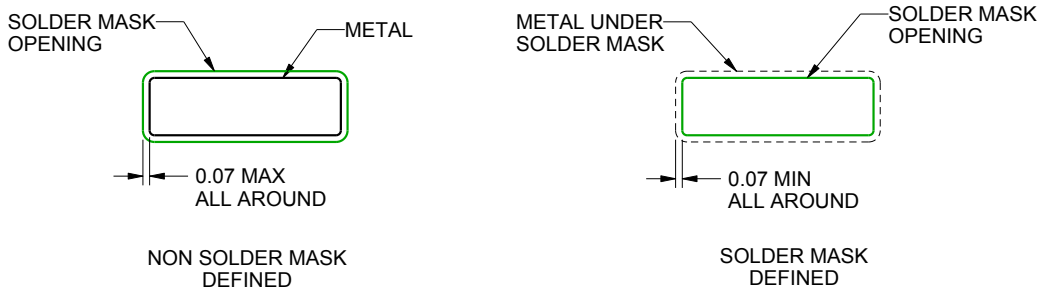
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

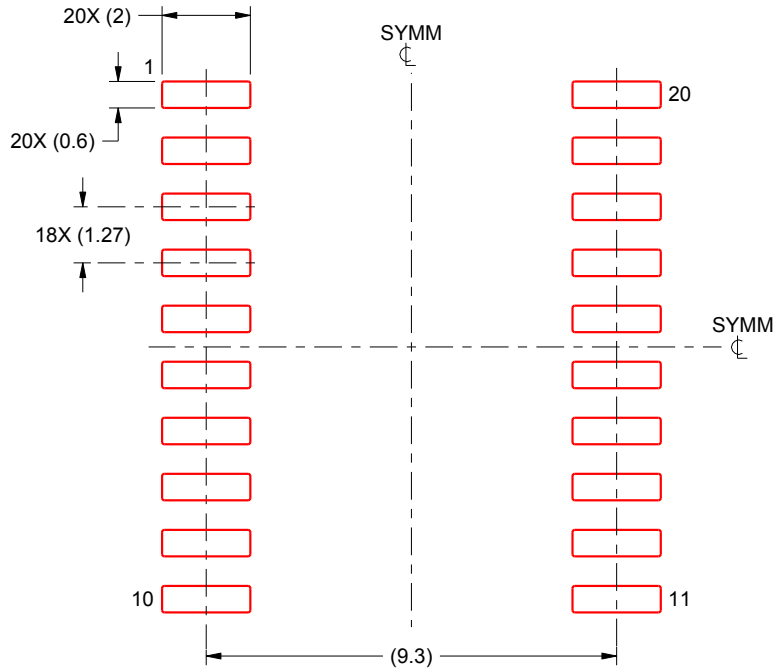
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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