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CY28416

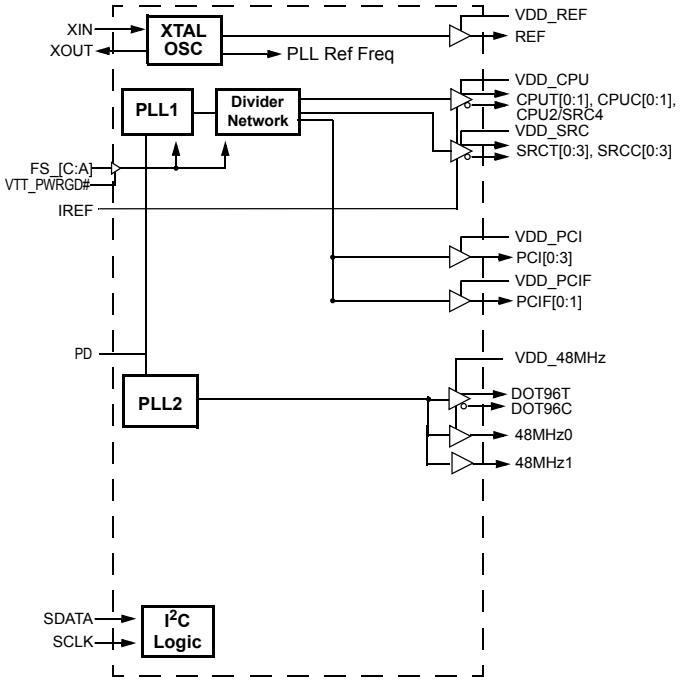
Next Generation FTG for Intel® Architecture

Features

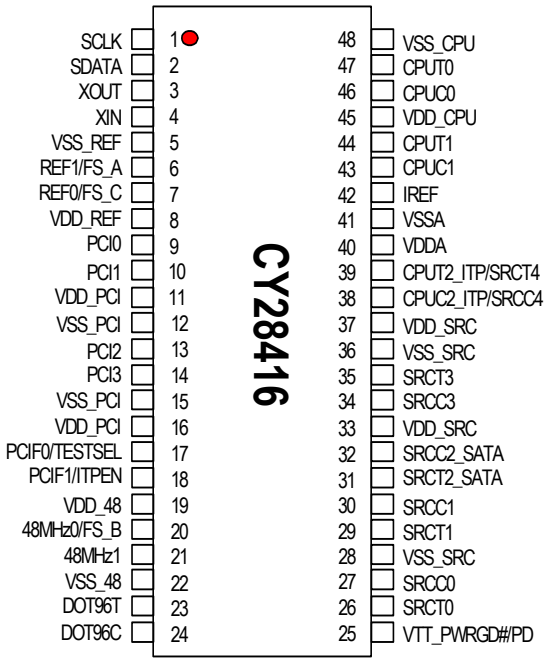
- Supports Intel Pentium®4-Type CPUs
- Selectable CPU Frequencies
- Two Differential CPU Clock Pairs
- Four 100-MHz Differential SRC Clock Pairs
- One CPU/SRC Selectable Differential Clock Pair
- One 96-MHz Differential Dot Clock Support
- Two 48-MHz Clocks
- Four 33-MHz PCI Clocks
- Two 33-MHz PCI Free Running Clocks
- Low Voltage Frequency Select Input
- I^2C Support Byte/Word/Block Read/Write Capabilities
- Ideal Lexmark Spread Spectrum Profile for Maximum EMI Reduction
- 3.3V Power Supply
- 48-pin SSOP Package

CPU	SRC	PCI	DOT	USB	REF
x2 / x3	x4 / x5	x 6	x 1	x 2	x 2

Block Diagram



Pin Configuration



48-PIN SSOP

Pin Definition

Pin No.	Name	Type	Description
47,46,44,43	CPUT/C[0:1]	O, DIF	**Differential CPU clock output**.
39,38	CPUT2_ITP/SRCT4 CPUC2_ITP/SRCC4	O, DIF	Selectable Differential CPU or SRC clock output. ITP_EN = 0 @VTT_PWRGD# assertion PIN 39,38 = SRCT4,SRCC4 ITP_EN = 1 @VTT_PWRGD# assertion PIN 39,38 = CPUT2_ITP,CPUC2_ITP
23,24	DOT96T, DOT96C	O, DIF	**Differential 96-MHz clock output**.
6	FS_A/REF1	I/O, SE	**3.3V tolerant input for CPU frequency/REF clock** *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications*.
20	FS_B/48 MHz0	I/O, SE	**3.3V tolerant input for CPU frequency/48-MHz clock** *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications*.
7	FS_C/REF0	I/O, SE	**3.3V tolerant input for CPU frequency/REF clock** *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications*.
42	IREF	I	A precision resistor is attached to this pin, which is connected to the internal current reference.
18	ITP_EN/PCIF1	I/O, SE	**Enable SRC4 or CPU2_ITP/PCIF clock.** (sampled on the VTT_PWRGD# assertion). 0 = SRC4, 1 = CPU2_ITP
9,10,13,14	PCI	O, SE	**33-MHz clock output**.
21	48 MHz1	O, SE	**48-MHz clock output**. (Uses same control SMBus register as 48 MHz0 to control enable/disable.)
1	SCLK	I	**SMBus compatible SCLOCK**.
2	SDATA	I/O	**SMBus compatible SDATA**.
26,27,29,30, 34,35	SRCT/C[0:3]	O, DIF	**Differential Serial reference clock**.
31,32	SRCT2_SATA, SRCC2_SATA	O, DIF	**Differential Serial reference clock**. Recommended output for SATA
17	TEST_SEL/PCIF0	I/O, SE, PD	**LVTTL input for selecting HI-Z or Normal operation/33-MHz Clock** 0 = Normal operation, 1 = HI-Z when VTT_PWRGD# is sampled
19	VDD_48	PWR	**3.3V power supply for outputs**
45	VDD_CPU	PWR	**3.3V power supply for outputs**
11, 16	VDD_PCI	PWR	**3.3V power supply for outputs**
8	VDD_REF	PWR	**3.3V power supply for outputs**
33, 37	VDD_SRC	PWR	**3.3V power supply for outputs**
40	VDDA	PWR	**3.3V power supply for PLL**
22	VSS_48	GND	**Ground for outputs**
48	VSS_CPU	GND	**Ground for outputs**
12, 15	VSS_PCI	GND	**Ground for outputs**
5	VSS_REF	GND	**Ground for outputs**
28, 36	VSS_SRC	GND	**Ground for outputs**
41	VSSA	GND	**Ground for PLL**
25	VTT_PWRGD#/PD	I, PD	**3.3V LVTTL Input**. This pin is a level-sensitive strobe used to latch the FS_A, FS_B, FS_C/TEST_SEL, and PCIF0/ITP_EN Inputs. After asserting VTT_PWRGD# (active LOW), this pin becomes a realtime input for asserting power-down (active HIGH)
4	XIN	I	**14.318-MHz Crystal Input**
3	XOUT	O	**14.318-MHz Crystal Output**

Frequency Select Pins (FS_A, FS_B, and FS_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A, FS_B, FS_C inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A, FS_B, and FS_C input values. For all logic levels of FS_A, FS_B, and FS_C VTT_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FS_A, FS_B, and FS_C transitions will be ignored, except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Frequency Select Table (FS_A FS_B)

FS_C	FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	DOT96	USB
1	0	1	100 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	0	266 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
1	0	0	RESERVED					
1	1	0						
1	1	1						

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 Bits	18:11	Command Code – 8 Bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge

Table 3. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N –8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge
		...	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	CPUT2_ITP/SRCT4 CPUC2_ITP/SRCC4	CPU[T/C]2_ITP/SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	RESERVED	RESERVED, Set = 1
5	1	RESERVED	RESERVED, Set = 1
4	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SRC[T/C]2_SATA	SRC[T/C]2_SATA Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	RESERVED	RESERVED, Set = 1

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	Spread Selection	0=Center Spread, 1= Down Spread (Default)
6	1	DOT_96T/C	DOT_96 MHz Output Enable 0 = Disable (Hi-Z), 1 = Enabled
5	1	48 MHz0, 48 MHz1	48-MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0	REF Output Enable 0 = Disabled, 1 = Enabled
3	1	REF1	REF Output Enable 0 = Disabled, 1 = Enabled
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enabled
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enabled
0	0	CPUT/C SRCT/C PCIF PCI	Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
5	1	RESERVED	RESERVED, Set = 1
4	1	RESERVED	RESERVED, Set = 1
3	1	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
2	1	PCI0	PCI0 Output Enable 0 = Disabled, 1 = Enabled
1	1	PCIF1	PCIF2 Output Enable 0 = Disabled, 1 = Enabled
0	1	PCIF0	PCIF1 Output Enable 0 = Disabled, 1 = Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	SRC[T/C]4	Allow control of SRC[T/C]4 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
6	0	RESERVED	RESERVED, Set = 0
5	0	RESERVED	RESERVED, Set = 0
4	0	SRC[T/C]3	Allow control of SRC[T/C]3 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC2_SATA	Allow control of SRC2_SATA with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC[T/C]1	Allow control of SRC[T/C]1 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC[T/C]0	Allow control of SRC[T/C]1 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	RESERVED	RESERVED, Set = 0

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	0	DOT96[T/C]	DOT_PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	PCIF1	Allow control of PCIF2 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
4	0	PCIF0	Allow control of PCIF1 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	RESERVED	RESERVED, Set = 0
2	1	RESERVED	RESERVED, Set = 1
1	1	RESERVED	RESERVED, Set = 1
0	1	RESERVED	RESERVED, Set = 1

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	SRC[T/C][4:0]	SRC[T/C] Stop Drive Mode 0 = Driven when SW PCI_STP# asserted,1 = Tri-state when SW PCI_STP# asserted
6	0	RESERVED	RESERVED, Set = 0
5	0	RESERVED	RESERVED, Set = 0
4	0	RESERVED	RESERVED, Set = 0
3	0	SRC[T/C][4:0]	SRC[T/C] PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted
2	0	CPU[T/C]2_ITP	CPU[T/C]2_ITP PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Tri-state when PD asserted

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	0		Test Clock Mode Entry Control 0 = Normal operation, 1 = Hi-Z mode
5	1	REF1	REF1 Output Drive Strength 0 = Low, 1 = High
4	1	REF0	REF0 Output Drive Strength 0 = Low, 1 = High
3	1	PCIF, SRC, PCI	SW PCI_STP# Function 0=SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF, and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF, and SRC outputs will resume in a synchronous manner with no short pulses.
2	Externally selected		FS_C. Reflects the value of the FS_C pin sampled on power-up 0 = FS_C was low during VTT_PWRGD# assertion
1	Externally selected		FS_B. Reflects the value of the FS_B pin sampled on power-up 0 = FS_B was low during VTT_PWRGD# assertion
0	Externally selected		FS_A. Reflects the value of the FS_A pin sampled on power-up 0 = FS_A was low during VTT_PWRGD# assertion

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	0	Revision Code Bit 1	Revision Code Bit 1
4	1	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	50 ppm	50 ppm	5 ppm

Crystal Recommendations

The CY28416 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28416 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal, not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is **not true.**

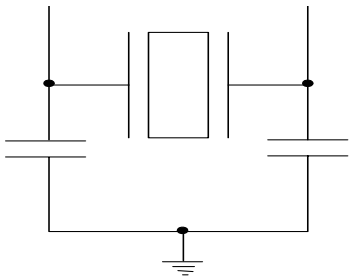


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

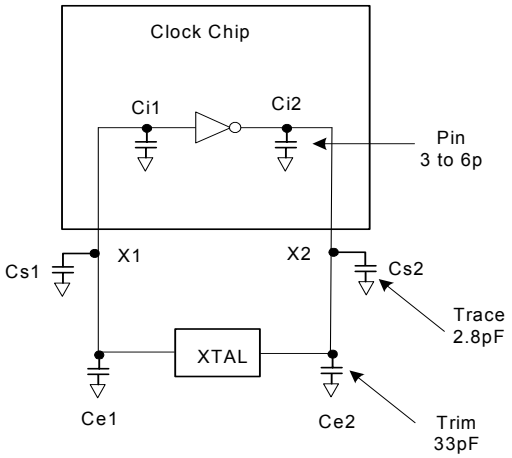


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .....Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs .....Stray capacitance (terraced)

Ci .....Internal capacitance (lead frame, bond wires etc.)

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs must be held LOW on their next HIGH-to-LOW transition and differential clocks must held high or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to ‘0’, the clock output must be held with “Diff clock” pin driven high at 2 x Iref, and “Diff clock#” tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to “1”, then both the “Diff clock” and the “Diff clock#” are tri-state. Note the example in *Figure 3* shows CPUT = 133 MHz and PD drive mode = ‘1’ for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, 200, 266, 333, and 400 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted high in less than 10 μs after asserting VTT_PWRGD#.

PD Deassertion

The power-up latency needs to be less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a tri-state condition resulting from power down must be driven high in less than 300 μs of PD deassertion to a voltage greater than 200 mV. After the clock chip’s internal PLL is powered up and locked, all outputs are to be enabled within a few clock cycles of each other. *Figure 4* is an example showing the relationship of clocks coming up. Unfortunately, we can not show all possible combinations, designers need to insure that from the first active clock output to the last takes no more than two full PCI clock cycles.

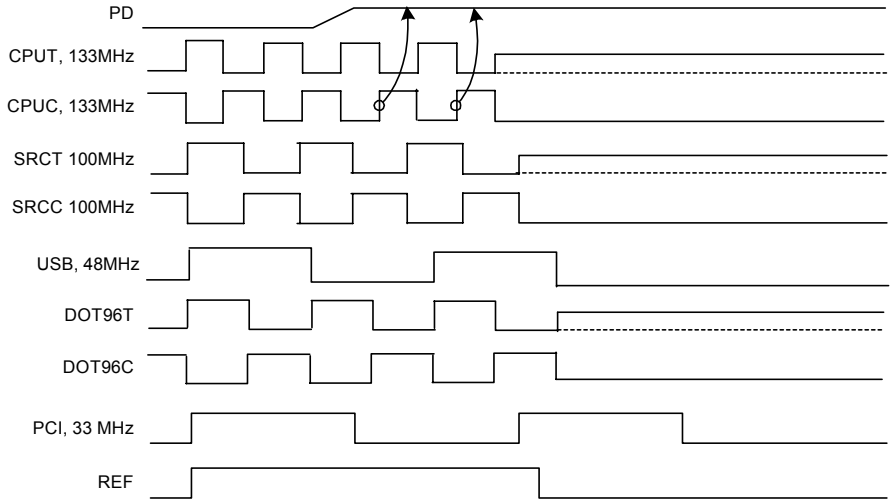


Figure 3. Power-down Assertion Timing Waveform

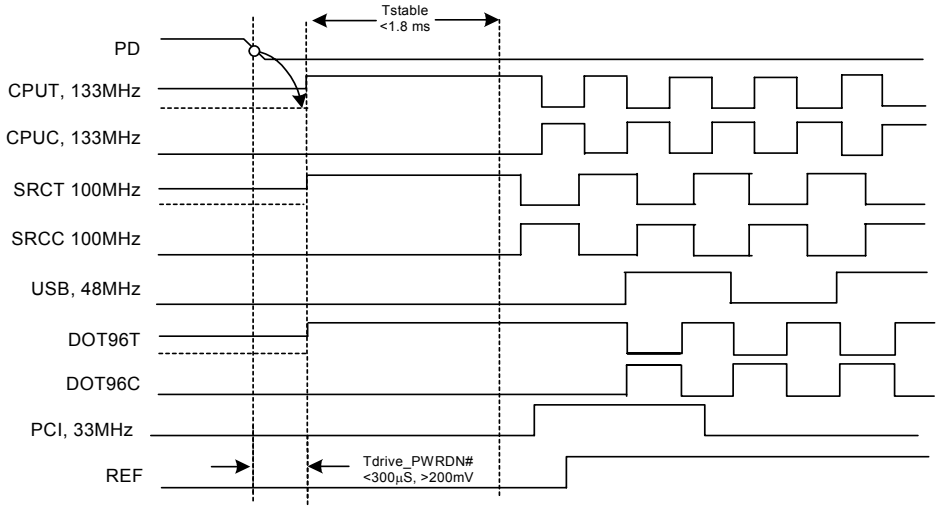


Figure 4. Power-down Deassertion Timing Waveform

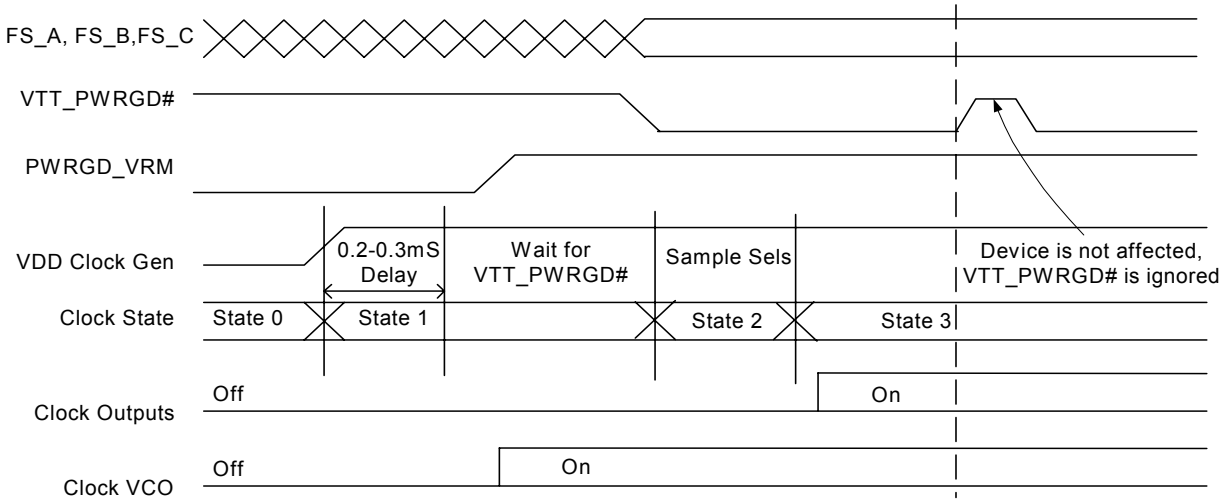


Figure 5. VTT_PWRGD# Timing Diagram

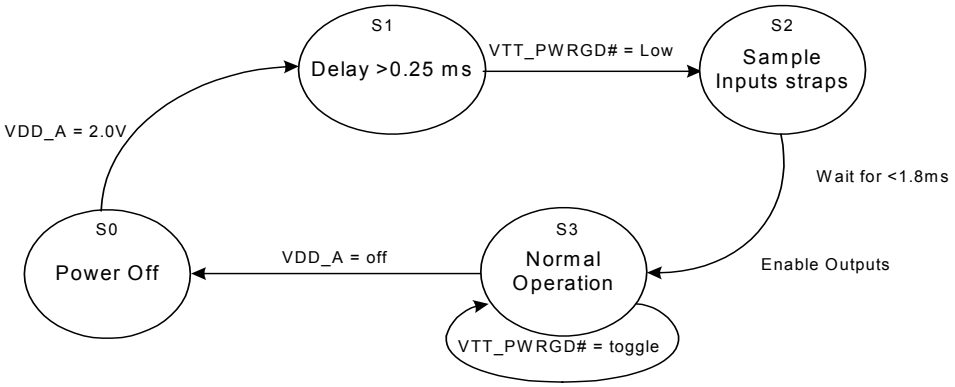


Figure 6. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	–	15	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	45	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD_A VDD_REF, VDD_PCI, VDD_3V66, VDD_48, VDD_CPU	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A:C] Input Low Voltage		0.7	V_{DD} + 0.5	V
V_{IH_FS}	FS_[A:C] Input High Voltage		V_{SS} – 0.3	0.35	V
V_{IL}	Input Low Voltage		V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V_{IN} < V_{DD}	–5	–	µA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V_{IN} < V_{DD}	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		2	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		0.7V_{DD}	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	0.3V_{DD}	V
$I_{DD3.3V}$	Dynamic Supply Current	At max load and freq per *Table 6* and *Figure 7*	–	400	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs driven	–	70	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-stated	–	2	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	40	60	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.9970	10.003	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.4978	7.5023	ns
T_{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	5.9982	6.0018	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.9985	5.0015	ns
T_{PERIOD}	266-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	3.7489	3.7511	ns
$T_{PERIODSS}$	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	9.9970	10.0533	ns
$T_{PERIODSS}$	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	7.4978	7.5400	ns
$T_{PERIODSS}$	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	5.9982	6.0320	ns
$T_{PERIODSS}$	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	4.9985	5.0266	ns
$T_{PERIODSS}$	266-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	3.7489	3.7700	ns
T_{SKEW}	Any CPUT/C to CPUT/C Clock Skew, SSC	Measured at crossing point V_{OX}	–	160	ps
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	90	ps
T_{CCJ}	CPU2/SRC4 Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	150	ps
T_R / T_F	CPUT and CPUC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mv
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7*. Measure SE	–	0.2	V
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.9970	10.003	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.9970	10.0533	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	130	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		220	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7*. Measure SE	–	0.2	V
PCI/PCIF					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.0090	ns
T_{PERIOD}	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.1598	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCIF and PCI rise and fall times	Measured between 0.4V and 2.4V	0.3	1.2	ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
DOT					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at crossing point V_{OX}	10.4135	10.4198	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	DOT96T and DOT96C Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	780	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		200	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7*. Measure SE	–	0.2	V
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.8271	20.8396	ns
T_{HIGH}	USB high time	Measurement at 2.4V	8.090	10.200	ns
T_{LOW}	USB low time	Measurement at 0.4V	7.690	9.950	ns
T_R / T_F	Rise and Fall Times	Measured between 0.4V and 2.4V	0.4	1.4	ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	400	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
T_R / T_F	REF Rise and Fall Times	Measured between 0.4V and 2.4V	0.2	2.1	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
ENABLE/DISABLE and SETUP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Table 6. Maximum Lumped Capacitive Output Loads

Clock	Max Load	Unit
PCI Clocks	30	pF
48M Clock	20	pF
REF Clock	30	pF

Test and Measurement Set-up

For Differential CPU and SRC Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

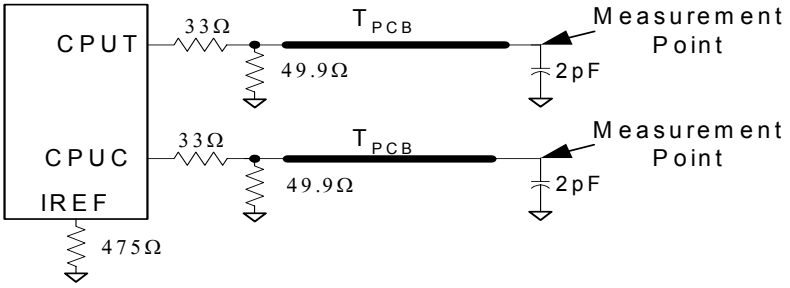


Figure 7. 0.7V Load Configuration

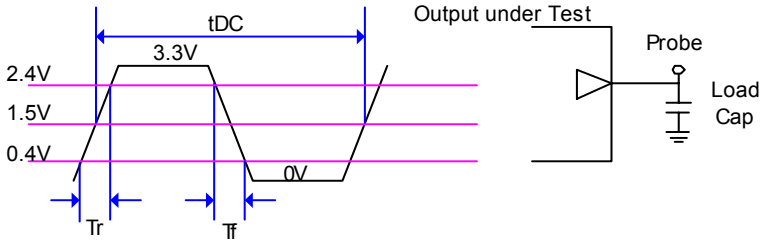


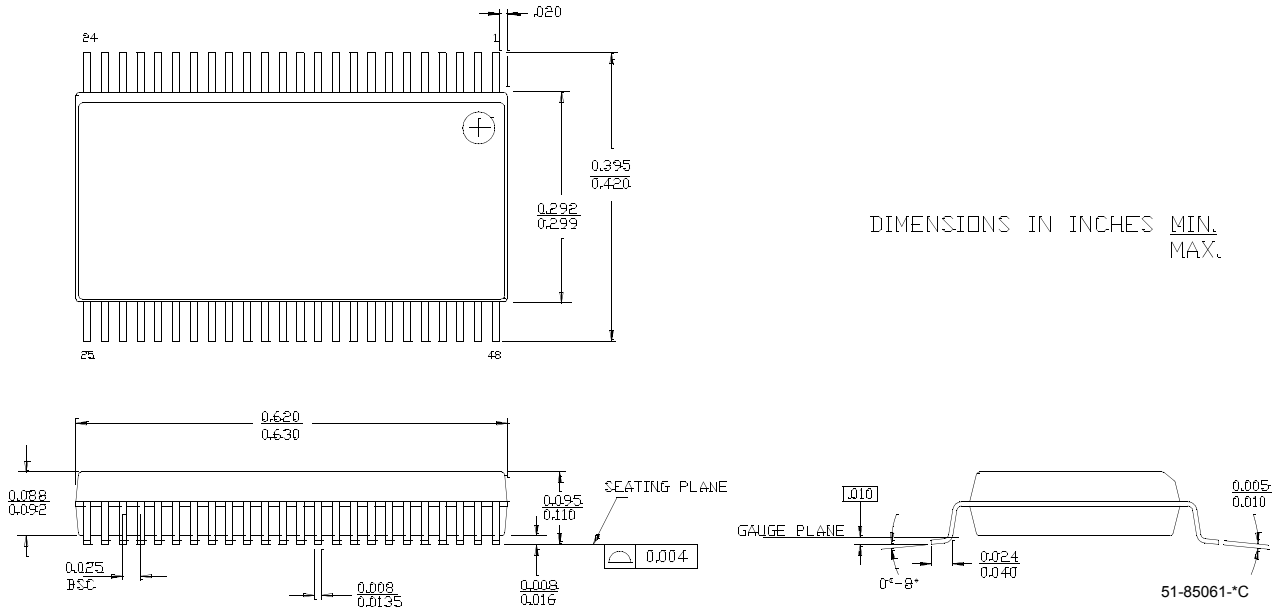
Figure 8. Lumped Load For Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28416OXC	48-pin SSOP	Commercial, 0° to 70°C
CY28416OXCT	48-pin SSOP—Tape and Reel	Commercial, 0° to 70°C

Package Drawings and Dimensions

48-lead Shrunk Small Outline Package O48



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Document History Page

Document Title: CY28416 Next Generation FTG for Intel® Architecture Document #: 38-07657 Rev. *C				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224420	See ECN	RGL/TUJ	New Data Sheet
*A	318277	See ECN	RGL	Changed VTTPWRGD and PCIF0 pins from PU to PD
*B	375236	See ECN	RGL	Changed definition of Byte 1 bit 7 Fix AC parameters table as per char data
*C	385998	See ECN	RGL	Removed Preliminary Changed CPU cycle-to-cycle jitter max to 90ps Changed SRC crossing voltage min to 220mV Changed DOT crossing voltage min to 200mV