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**FAIRCHILD**  
SEMICONDUCTOR®

# FDS2734

## N-Channel UltraFET Trench® MOSFET

250V, 3.0A, 117mΩ

### Features

- Max  $r_{DS(on)}$  = 117mΩ at  $V_{GS} = 10V$ ,  $I_D = 3.0A$
- Max  $r_{DS(on)}$  = 126mΩ at  $V_{GS} = 6V$ ,  $I_D = 2.8A$
- Fast switching speed
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability
- RoHS compliant

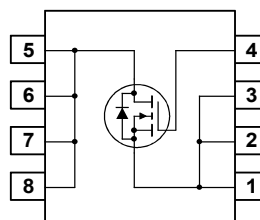
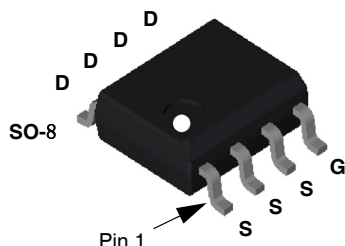


### General Descriptions

This single N-Channel MOSFET is produced using Fairchild Semiconductor's advanced UltraFET Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC-DC conversion



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	250	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Note 1a)	3.0	A
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12.5	mJ
$P_D$	Power dissipation (Note 1a)	2.5	W
	Power dissipation (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction- to -Ambient (Note 1a)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction- to- Ambient (Note 1b)	125	
$R_{\theta JC}$	Thermal Resistance, Junction -to- Case (Note 1)	25	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS2734	FDS2734	SO-8	13"	12mm	2500 units

FDS2734 Single N-Channel UltraFET Trench® MOSFET

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	250			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		157		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 200\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-10.7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3.0\text{A}$ ,		97	117	m $\Omega$
		$V_{GS} = 6\text{V}, I_D = 2.8\text{A}$ ,		101	126	
		$V_{GS} = 10\text{V}, I_D = 3.0\text{A}, T_J = 125^\circ\text{C}$		205	225	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 3.0\text{A}$ ,		15.1		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1960	2610	pF
$C_{oss}$	Output Capacitance			85	130	pF
$C_{rss}$	Reverse Transfer Capacitance			26	40	pF
$R_G$	Gate Resistance	$f = 1\text{MHz}$		0.7		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{V}, I_D = 3\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 6\Omega$		23	37	ns
$t_r$	Rise Time			11	19	ns
$t_{d(off)}$	Turn-Off Delay Time			40	64	ns
$t_f$	Fall Time			11	19	ns
$Q_g$	Total Gate Charge	$V_{DS} = 125\text{V}, V_{GS} = 10\text{V}$ $I_D = 3.0\text{A}$		32	45	nC
$Q_{gs}$	Gate to Source Gate Charge			9		nC
$Q_{gd}$	Gate to Drain Charge			8		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 3.0\text{A}$		0.74	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.0\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		72	108	ns
$Q_{rr}$	Reverse Recovery Charge			185	278	nC

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2: Pulse Test Width  $< 300\mu\text{s}$ , Duty Cycle  $< 2\%$ .  
3: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $I_{AS} = 5\text{A}$ ,  $V_{DD} = 100\text{V}$ ,  $V_{GS} = 10\text{V}$

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

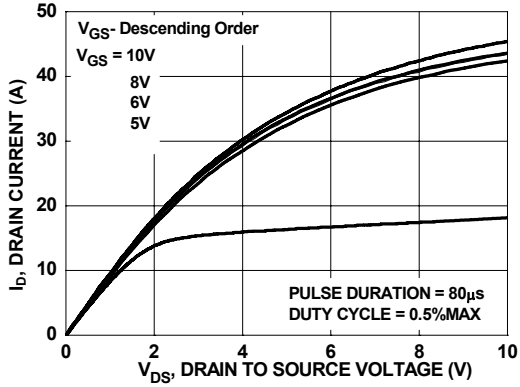


Figure 1. On Region Characteristics

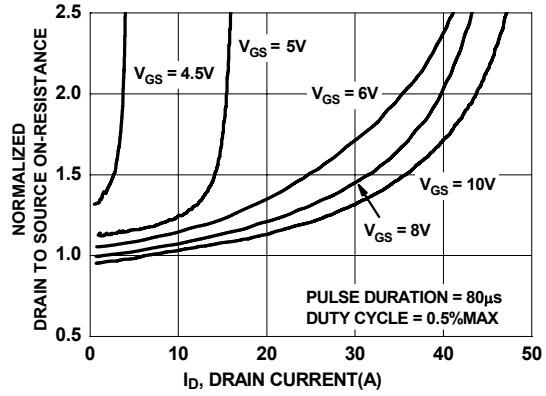


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

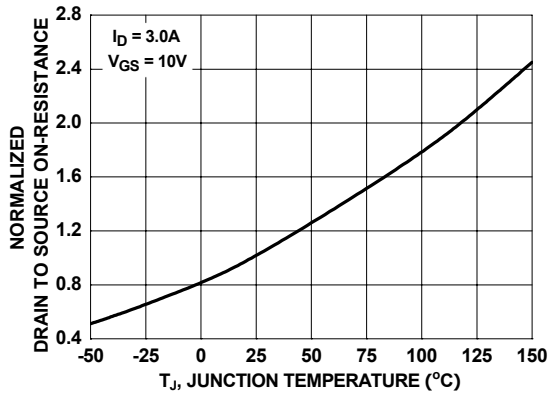


Figure 3. Normalized On Resistance vs Junction Temperature

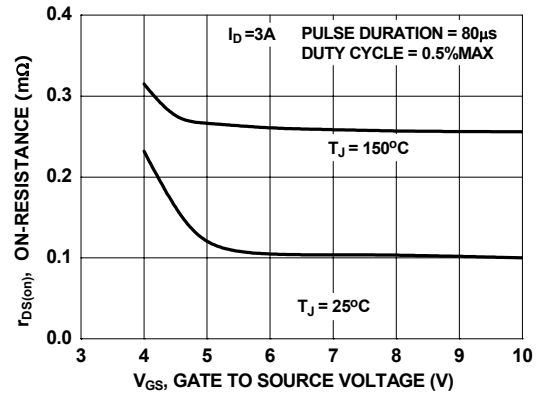


Figure 4. On-Resistance vs Gate to Source Voltage

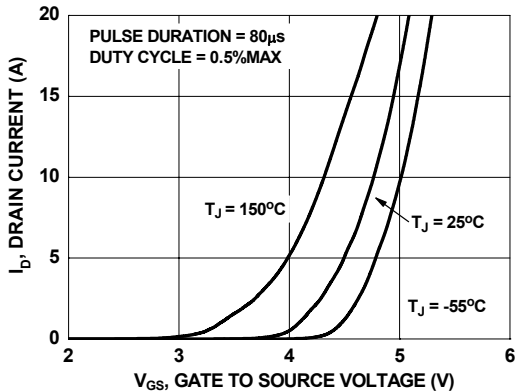


Figure 5. Transfer Characteristics

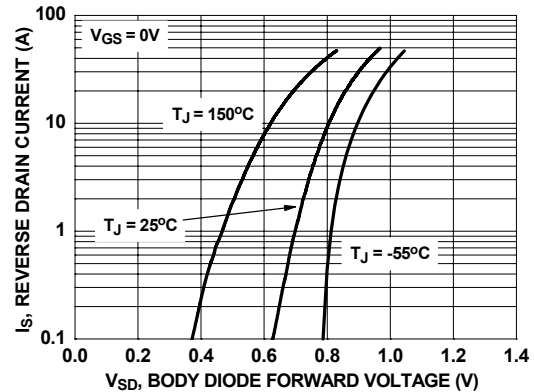
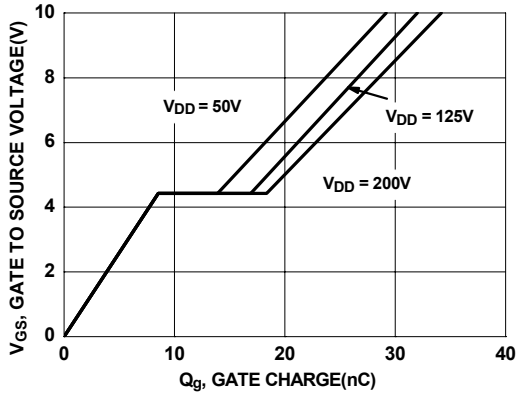
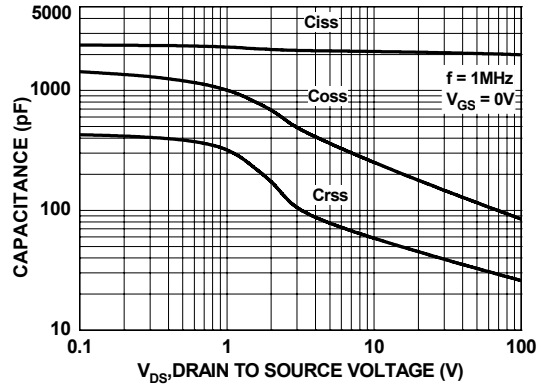


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

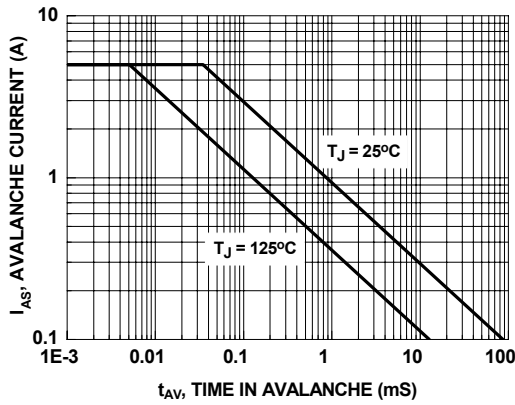
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



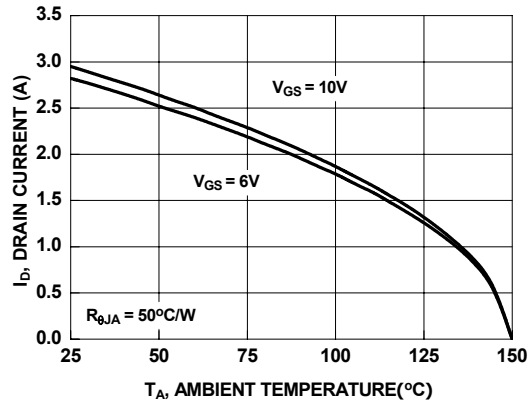
**Figure 7. Gate Charge Characteristics**



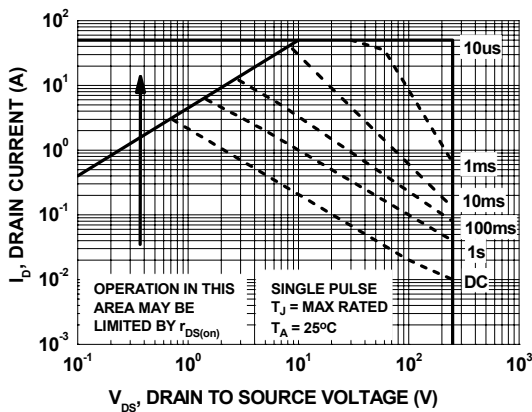
**Figure 8. Capacitance vs Drain to Source Voltage**



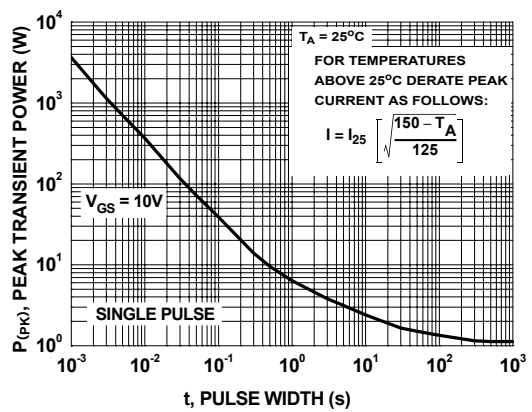
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

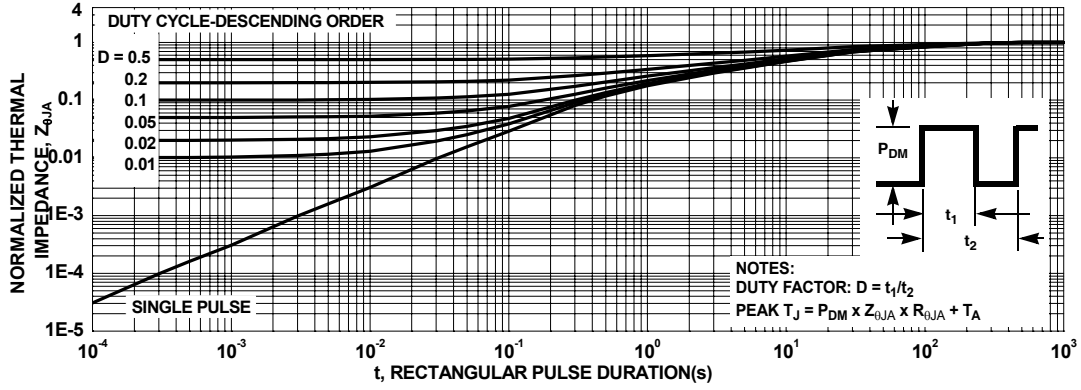


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1b  
 Transient thermal response will change depending on the circuit board design

**FDS2734 Single N-Channel UltraFET Trench<sup>®</sup> MOSFET**

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