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TPS3836E18-EP / J25-EP / H30-EP / L30-EP / K33-EP  
 TPS3837E18-EP / J25-EP / L30-EP / K33-EP  
 TPS3838E18-EP / J25-EP / L30-EP / K33-EP

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SGLS322D-MAY 2006-REVISED NOVEMBER 2008

## NANOPOWER SUPERVISORY CIRCUITS

### FEATURES

- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Supply Current of 220 nA (Typ)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3 V, 3.3 V
- Power-On Reset Generator With Selectable Delay Time of 10 ms or 200 ms
- Push/Pull  $\overline{\text{RESET}}$  Output (TPS3836), RESET Output (TPS3837), or Open-Drain RESET Output (TPS3838)
- Manual Reset
- 5-Pin SOT-23 Package

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (-55°C/125°C) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

### APPLICATIONS

- Applications Using Automotive Low-Power DSPs, Microcontrollers, or Microprocessors
- Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Automotive Systems

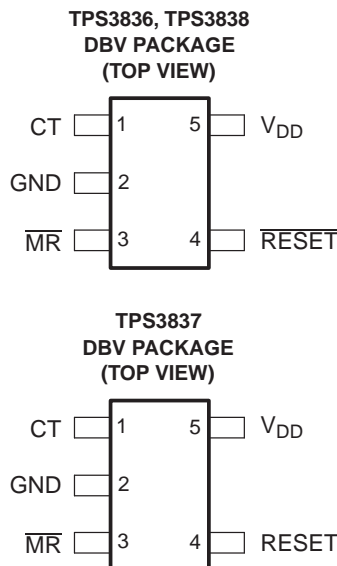
(1) Custom temperature ranges available

### DESCRIPTION

The TPS3836, TPS3837, TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for digital signal processing (DSP) and processor-based systems.

During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{DD}$  and keeps  $\overline{\text{RESET}}$  output active as long as  $V_{DD}$  remains below the threshold voltage ( $V_{IT}$ ). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after  $V_{DD}$  has risen above  $V_{IT}$ .

When CT is connected to GND, a fixed delay time of typical 10 ms is asserted. When connected to  $V_{DD}$ , the delay time is typically 200 ms.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TPS3836E18-EP / J25-EP / H30-EP / L30-EP / K33-EP**

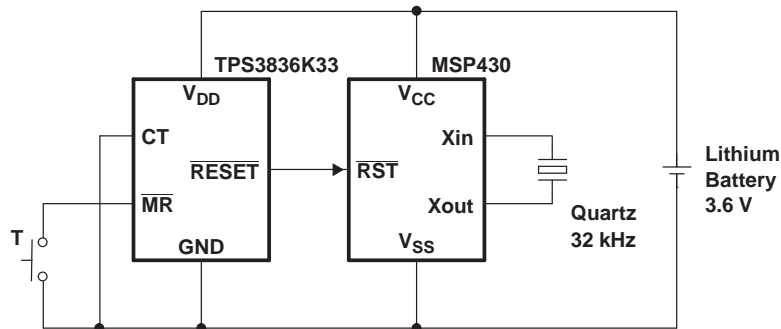
**TPS3837E18-EP / J25-EP / L30-EP / K33-EP**

**TPS3838E18-EP / J25-EP / L30-EP / K33-EP**

When the supply voltage drops below  $V_{IT}$ , the output becomes active (low) again.

All the devices of this family have a fixed-sense  $V_{IT}$  set by an internal voltage divider.

The TPS3836 has an active-low push-pull  $\overline{\text{RESET}}$  output. The TPS3837 has active-high push-pull RESET, and the TPS3838 integrates an active-low open-drain  $\overline{\text{RESET}}$  output.



**Figure 1. Typical Operating Circuit**

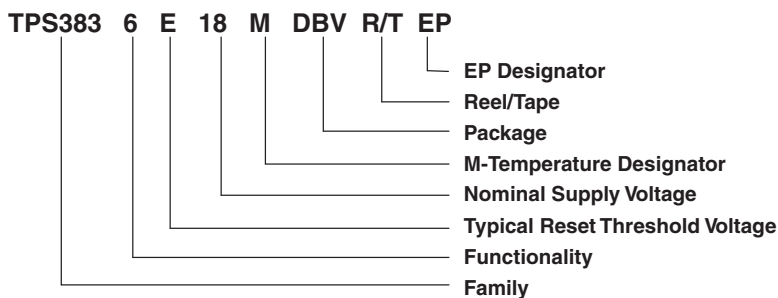
The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3 V, and 3.3 V. The circuits are available in a 5-pin SOT-23 package. The TPS3836, TPS3837, and TPS3838 families are characterized for operation over a temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**ORDERING INFORMATION**

T <sub>A</sub>	ORDERABLE PART NUMBER <sup>(1)</sup>	THRESHOLD VOLTAGE	SYMBOL
-55°C to 125°C	TPS3836J25MDBVTEP	2.25 V	PKRM
	TPS3836L30MDBVREP	2.64 V	BTX
	TPS3837K33MDBVREP	2.93 V	PKZM

(1) DBVR indicates reel of 3000 parts, DBVT indicates tape of 250 parts.

**ORDERING INFORMATION**



**FUNCTION TABLE**

$\overline{\text{MR}}$	$V_{\text{DD}} > V_{\text{IT}}$	RESET <sup>(1)</sup>	RESET <sup>(2)</sup>
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3836 and TPS3838

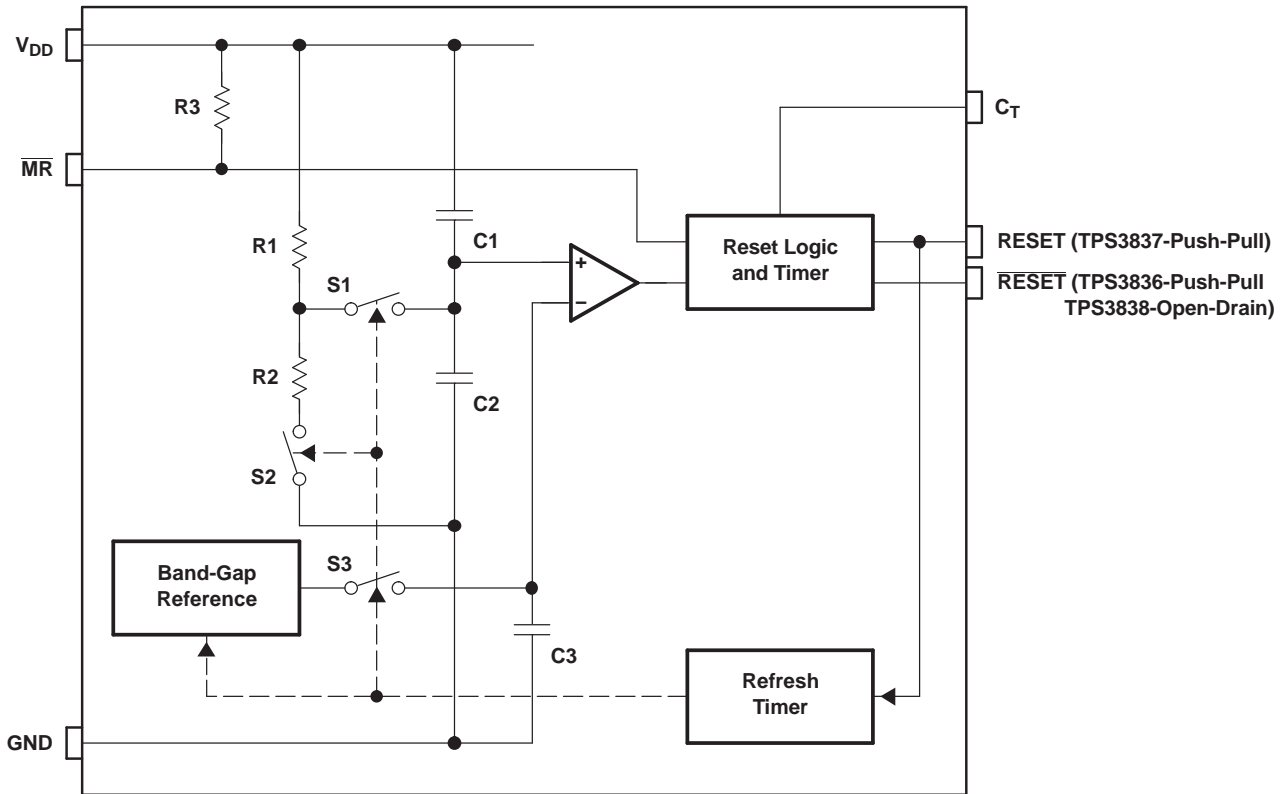
(2) TPS3837

TPS3836E18-EP / J25-EP / H30-EP / L30-EP / K33-EP

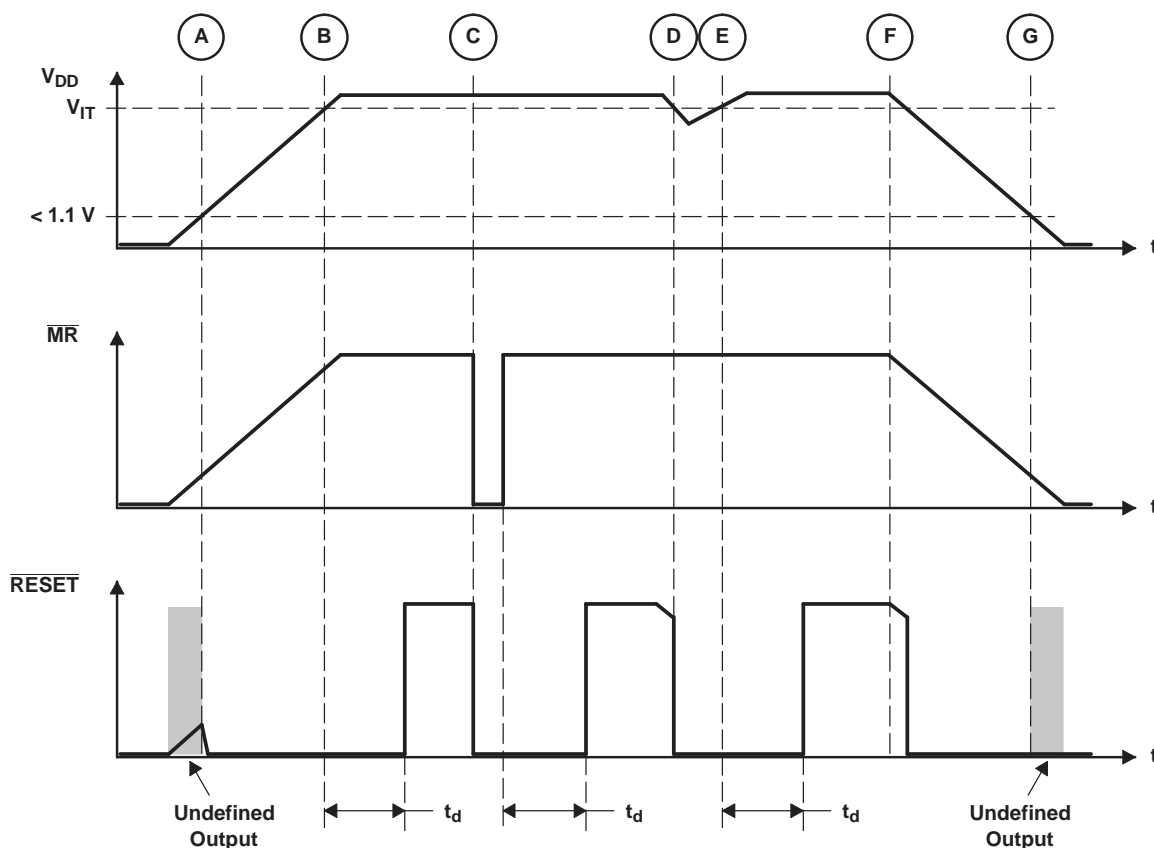
TPS3837E18-EP / J25-EP / L30-EP / K33-EP

TPS3838E18-EP / J25-EP / L30-EP / K33-EP

**FUNCTIONAL BLOCK DIAGRAM**



**TIMING DIAGRAM**



**Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

$V_{DD}$	Supply voltage <sup>(2)</sup>	7 V
	All other pins <sup>(2)</sup>	-0.3 V to 7 V
$I_{OL}$	Maximum low output current	5 mA
$I_{OH}$	Maximum high output current	-5 mA
$I_{IK}$	Input clamp current ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 10$ mA
$I_{OK}$	Output clamp current ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 10$ mA
$T_A$	Operating free-air temperature range	-55°C to 125°C
$T_{stg}$	Storage temperature range	-65°C to 150°C
$T_J$	Maximum junction temperature	150°C
	Soldering temperature	260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, the device must not be continuously operated at 7 V for more than  $t = 1000$  h.

**TPS3836E18-EP / J25-EP / H30-EP / L30-EP / K33-EP**
**TPS3837E18-EP / J25-EP / L30-EP / K33-EP**
**TPS3838E18-EP / J25-EP / L30-EP / K33-EP**

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### Thermal Resistance Table

RESISTANCE	HIGH	LOW
$\theta_{JC}$ (°C/W)	130.9	148.1
$\theta_{JA}$ (°C/W)	205.6	347

### Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	1.6	6	V
$V_I$	Input voltage	0	$V_{DD} + 0.3$	V
$V_{IH}$	High-level input voltage	$0.7 \times V_{DD}$		V
$V_{IL}$	Low-level input voltage		$0.3 \times V_{DD}$	V
$\Delta t/\Delta v$	Input transition rise and fall rate at $\overline{MR}$		100	ns/V
$T_A$	Operating free-air temperature	-55	125	°C

### Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{OH}$	High-level output voltage	$\overline{RESET}$ (TPS3836)	$V_{DD} = 3.3\text{ V}, I_{OH} = -2\text{ mA}$	$0.8 \times V_{DD}$			V	
			$V_{DD} = 6\text{ V}, I_{OH} = -3\text{ mA}$					
		$\overline{RESET}$ (TPS3837)	$V_{DD} = 2\text{ V}, I_{OH} = -1\text{ mA}$					
			$V_{DD} = 3.3\text{ V}, I_{OH} = -2\text{ mA}$					
$V_{OL}$	Low-level output voltage	$\overline{RESET}$ (TPS3836/8)	$V_{DD} = 2\text{ V}, I_{OL} = 1\text{ mA}$				V	
			$V_{DD} = 3.3\text{ V}, I_{OL} = 2\text{ mA}$					
		$\overline{RESET}$ (TPS3837)	$V_{DD} = 3.3\text{ V}, I_{OL} = 2\text{ mA}$					
			$V_{DD} = 6\text{ V}, I_{OL} = 3\text{ mA}$					
Power-up reset voltage <sup>(1)</sup>		TPS3836/8	$V_{DD} \geq 1.1\text{ V}, I_{OL} = 50\text{ }\mu\text{A}$			0.2	V	
		TPS3837	$V_{DD} \geq 1.1\text{ V}, I_{OH} = -50\text{ }\mu\text{A}$	$T_A = 25^\circ\text{C}$	$0.8 \times V_{DD}$			
				$T_A = \text{Full range}$	$0.6 \times V_{DD}$			
$V_{IT}$	Negative-going input threshold voltage <sup>(2)</sup>	TPS383xE18		1.64	1.71	1.73	V	
		TPS383xJ25		2.16	2.25	2.31		
		TPS383xH30		2.7	2.79	2.85		
		TPS383xL30		2.54	2.64	2.71		
		TPS383xK33	$T_A = 25^\circ\text{C}$	2.82	2.93	3.1		
$T_A = \text{Full range}$	2.72		2.93	3.2				
$V_{hys}$	Hysteresis at $V_{DD}$ input		$1.7\text{ V} < V_{IT} < 2.5\text{ V}$		30		mV	
			$2.5\text{ V} < V_{IT} < 3.5\text{ V}$		40			
			$3.5\text{ V} < V_{IT} < 5\text{ V}$		50			
$I_{IH}$	High-level input current	$\overline{MR}$ <sup>(3)</sup>	$\overline{MR} = 0.7 \times V_{DD}, V_{DD} = 6\text{ V}$	$T_A = 25^\circ\text{C}$	-30	-60	-90	$\mu\text{A}$
				$T_A = \text{Full range}$	-20	-60	-120	
		CT	$CT = V_{DD} = 6\text{ V}$		-25		25	nA
$I_{IL}$	Low-level input current	$\overline{MR}$ <sup>(3)</sup>	$\overline{MR} = 0\text{ V}, V_{DD} = 6\text{ V}$	$T_A = 25^\circ\text{C}$	-130	-200	-340	$\mu\text{A}$
				$T_A = \text{Full range}$	-90	-200	-350	
		CT	$CT = 0\text{ V}, V_{DD} = 6\text{ V}$		-25		25	nA
$I_{OH}$	High-level output current	TPS3838	$V_{DD} = V_{IT} + 0.2\text{ V}, V_{OH} = V_{DD}$				25	nA

 (1) The lowest voltage at which  $\overline{RESET}$  output becomes active,  $t_r, V_{DD} \geq 15\text{ }\mu\text{s/V}$ 

 (2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1  $\mu\text{F}$ ) should be placed near the supply terminal.

 (3) If manual reset is unused,  $\overline{MR}$  should be connected to  $V_{DD}$  to minimize current consumption.

## Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD</sub>	Supply current	V <sub>DD</sub> > V <sub>IT</sub> , V <sub>DD</sub> < 3 V	T <sub>A</sub> = 25°C	220	500	nA
			T <sub>A</sub> = Full range		600	
		V <sub>DD</sub> > V <sub>IT</sub> , V <sub>DD</sub> > 3 V	T <sub>A</sub> = 25°C	250	550	
			T <sub>A</sub> = Full range		650	
		V <sub>DD</sub> < V <sub>IT</sub>	T <sub>A</sub> = 25°C	10	25	μA
			T <sub>A</sub> = Full range		30	
Internal pullup resistor at $\overline{MR}$				33		kΩ
C <sub>I</sub>	Input capacitance at $\overline{MR}$ , CT	V <sub>I</sub> = 0 V to V <sub>DD</sub>		5		pF

## Timing Requirements

 R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
t <sub>w</sub>	Pulse width	At V <sub>DD</sub>	6	μs
		At $\overline{MR}$	1	μs

## Switching Characteristics

 R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

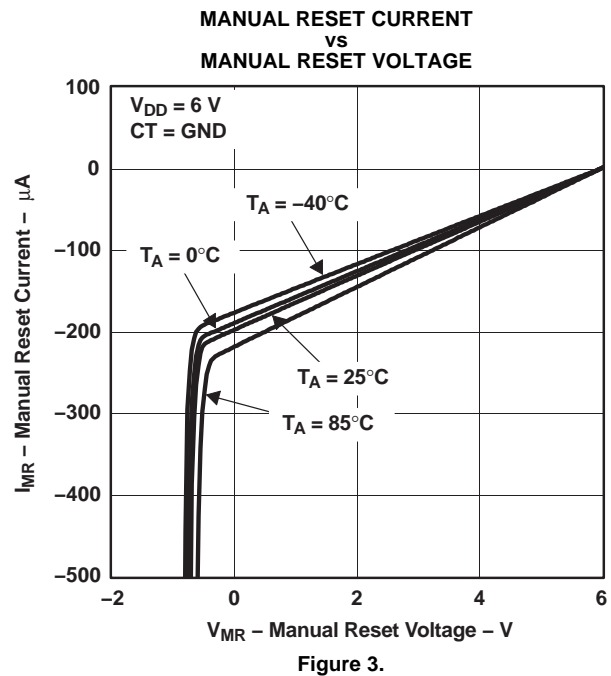
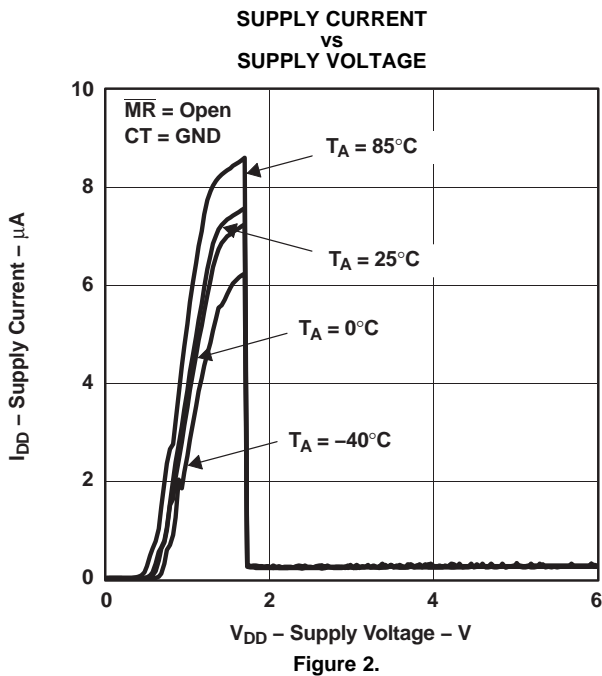
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, $\overline{MR}$ = 0.7 × V <sub>DD</sub> , See timing diagram	5	10	15	ms
		CT = GND				
		CT = V <sub>DD</sub>		200		
t <sub>PHL</sub>	Propagation (delay) time, high- to low-level output	V <sub>DD</sub> to $\overline{RESET}$ delay (TPS3836, TPS3838) V <sub>IL</sub> = V <sub>IT</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT</sub> + 0.2 V V <sub>IL</sub> = 1.6 V		10		μs
t <sub>PLH</sub>	Propagation (delay) time, low- to high-level output	V <sub>DD</sub> to RESET delay (TPS3837) V <sub>IL</sub> = V <sub>IT</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT</sub> + 0.2 V V <sub>IL</sub> = 1.6 V		10		
t <sub>PHL</sub>	Propagation (delay) time, high- to low-level output	V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, V <sub>IL</sub> = 0.3 × V <sub>DD</sub> , V <sub>IH</sub> = 0.7 × V <sub>DD</sub>		0.3		μs
t <sub>PLH</sub>	Propagation (delay) time, low- to high-level output	$\overline{MR}$ to RESET delay (TPS3836, TPS3838) V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, V <sub>IL</sub> = 0.3 × V <sub>DD</sub> , V <sub>IH</sub> = 0.7 × V <sub>DD</sub>		0.3		μs

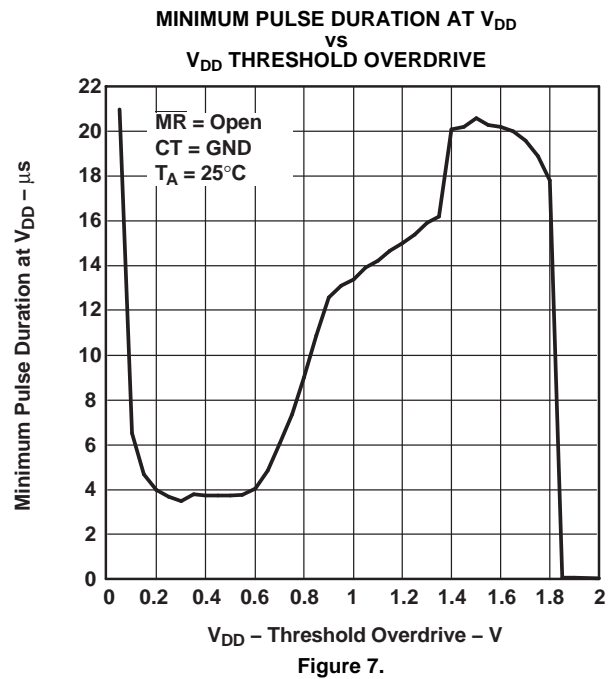
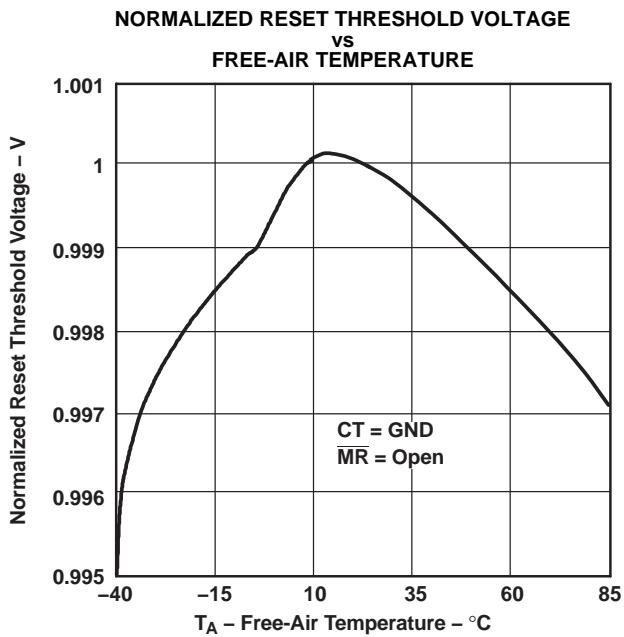
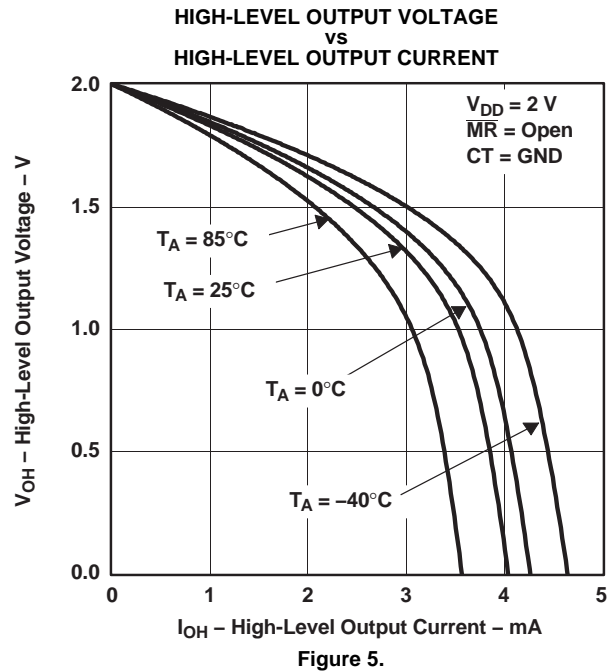
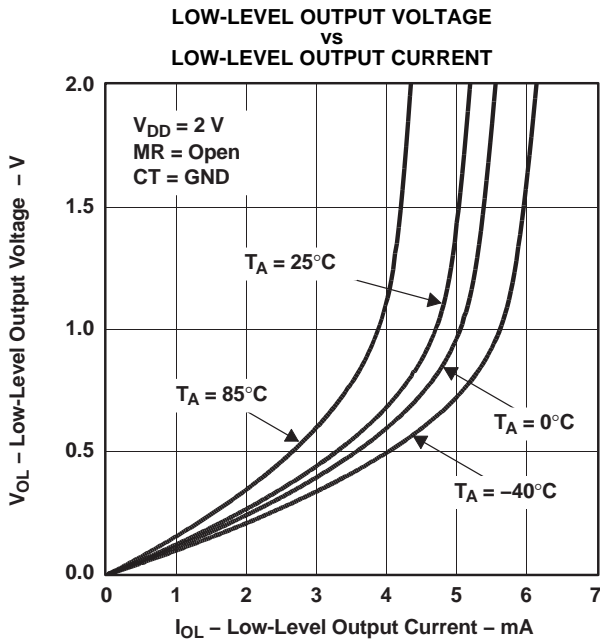


**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			<b>FIGURE</b>
$I_{DD}$	Supply current	vs Supply voltage	2
$I_{MR}$	Manual reset current	vs Manual reset voltage	3
$V_{OL}$	Low-level output voltage	vs Low-level output current	4
$V_{OH}$	High-level output voltage	vs High-level output current	5
	Normalized reset threshold voltage	vs Free-air temperature	6
	Minimum pulse duration at $V_{DD}$	vs $V_{DD}$ threshold overdrive	7





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3836J25MDBVTEP	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKRM	<a href="#">Samples</a>
TPS3836L30MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTX	<a href="#">Samples</a>
TPS3837K33MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKZM	<a href="#">Samples</a>
TPS3837K33QDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLSQ	<a href="#">Samples</a>
V62/06637-09XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLSQ	<a href="#">Samples</a>
V62/06637-15XE	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKRM	<a href="#">Samples</a>
V62/06637-17XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTX	<a href="#">Samples</a>
V62/06637-22XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKZM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3836J25-EP, TPS3836L30-EP, TPS3837K33-EP :**

● Catalog: [TPS3836J25](#), [TPS3836L30](#), [TPS3837K33](#)

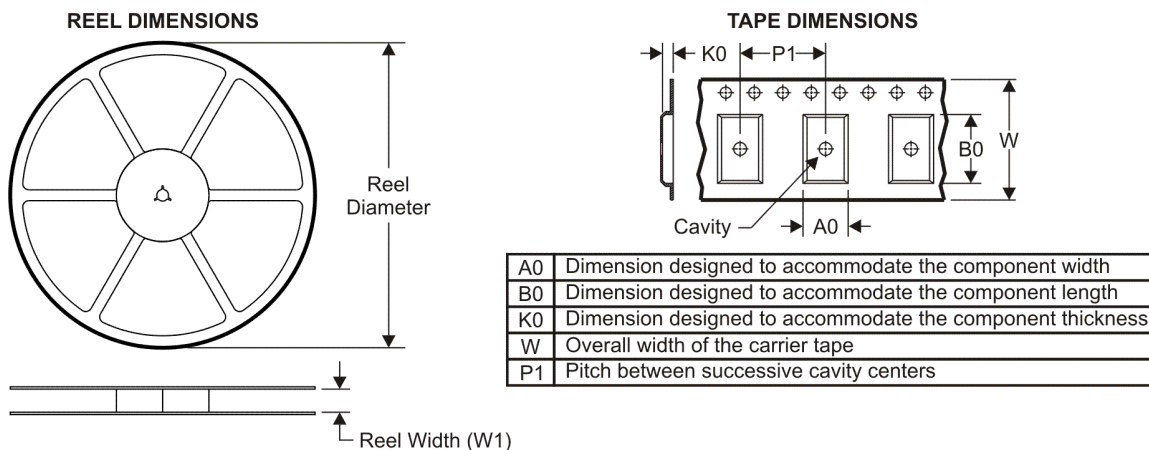
● Automotive: [TPS3836J25-Q1](#), [TPS3836L30-Q1](#), [TPS3837K33-Q1](#)

**NOTE: Qualified Version Definitions:**

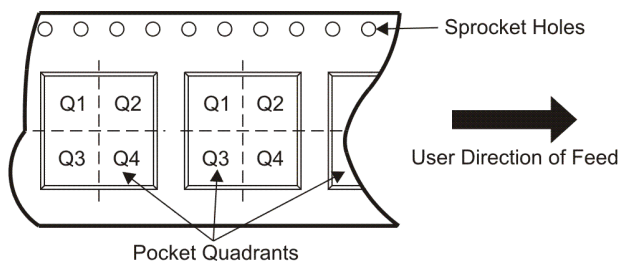
● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**



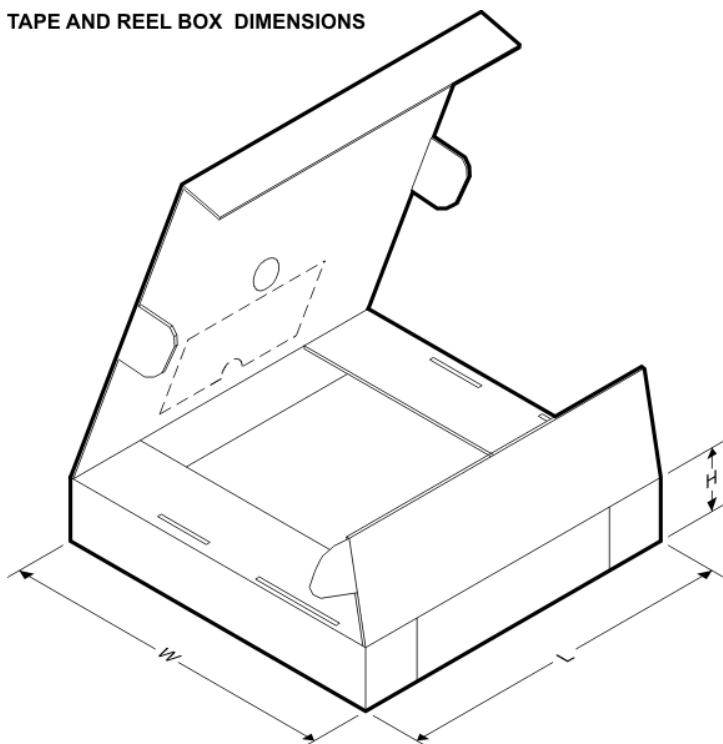
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3836J25MDBVTEP	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3836L30MDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3837K33MDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3837K33QDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



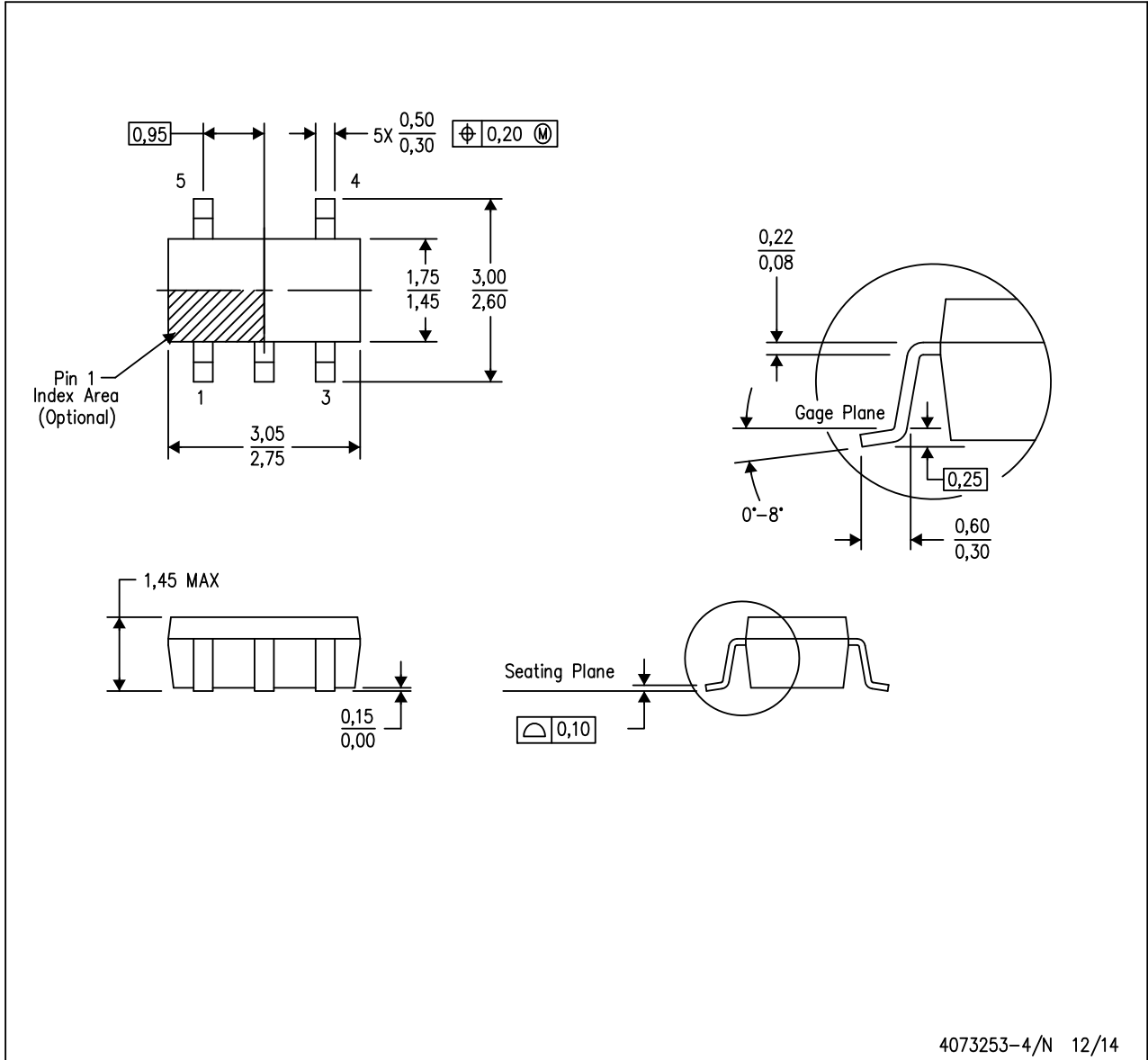
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3836J25MDBVTEP	SOT-23	DBV	5	250	182.0	182.0	20.0
TPS3836L30MDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3837K33MDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3837K33QDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0

**MECHANICAL DATA**

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

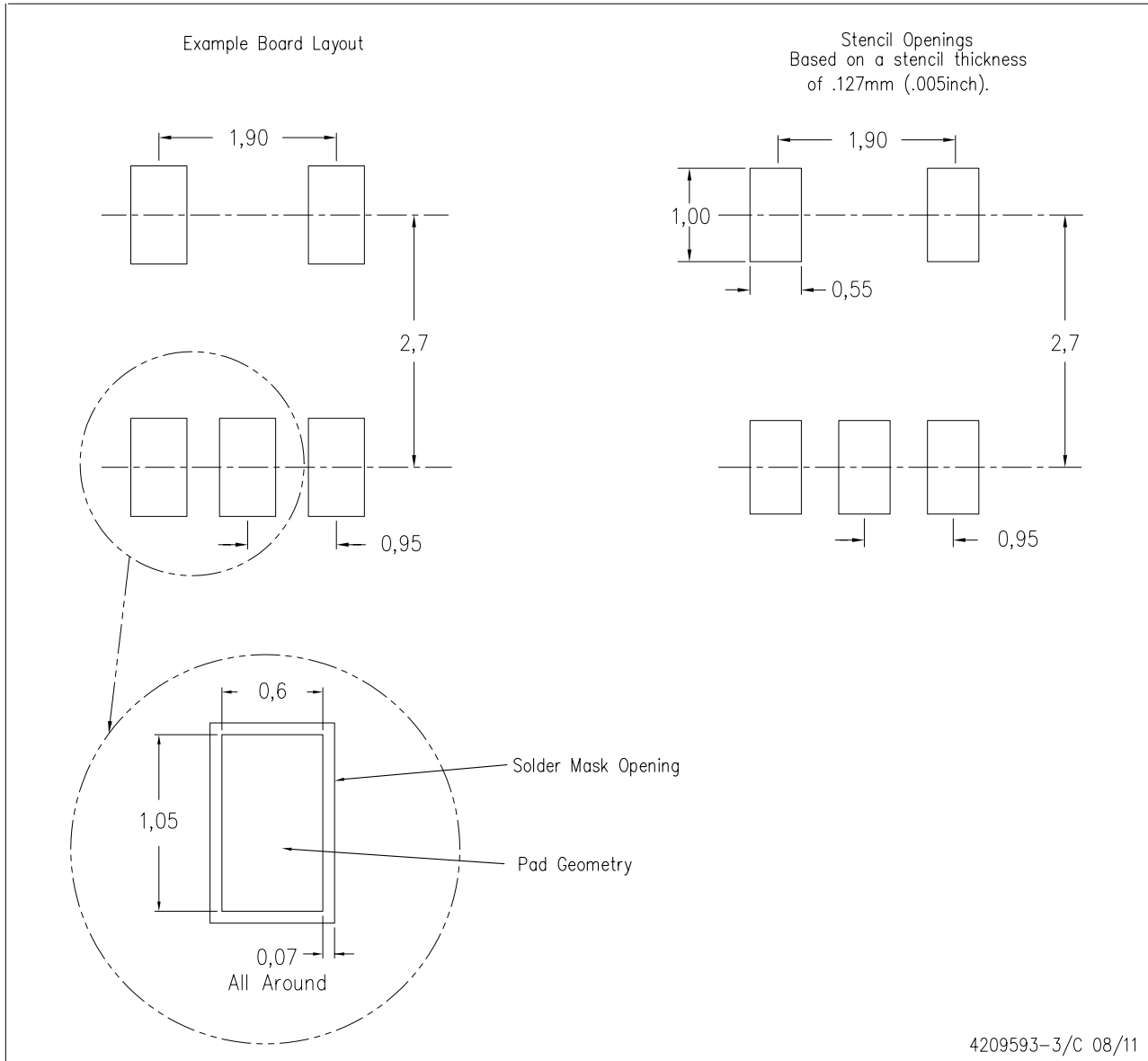


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

**LAND PATTERN DATA**

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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