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TISP61089HDMR-S

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TISP61089HDM

DUAL FORWARD-CONDUCTING P-GATE THYRISTOR PROGRAMMABLE OVERVOLTAGE PROTECTOR

TISP61089HDM Overvoltage Protector

Intended for Use in GR-1089-CORE Issue 3 Compliant Line Cards

Dual, Voltage-Programmable SLIC Protector
– Low 15 mA max. Gate Triggering Current
– Supports Battery Voltages Down to -155 V
– High 150 mA min. Holding Current

Rated for GR-1089-CORE Issue 3 Conditions

Impulse Waveshape	GR-1089-CORE Test		I_{PPSM}
	Section	Test #	A
2/10	4.6.7 4.6.8	4 1	500
10/1000	4.6.7 4.6.7.1	1, 3 1	100

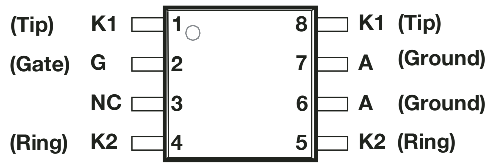
Meets GR-1089-CORE First Level A.C. Power Fault Conditions

GR-1089-CORE Section 4.6.10 Test #	I RMS	Power Fault Duration
	A	s
1	0.33	900
2	0.17	900
3	1	1
4	1	1
6	0.5	30
7	2.2	2
8	3	1.1
9	5	0.4

GR-1089-CORE Second Level A.C. Power Fault Conditions are Detailed in the 'Applications Information' Section

.... **UL Recognized Component**

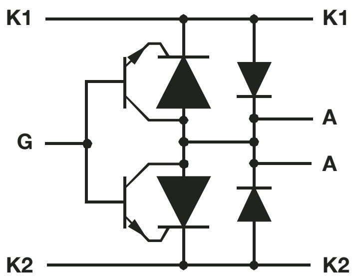
8-SOIC (210 mil) Package (Top View)



NC - No internal connection
Terminal typical application names shown in parenthesis

MD-8SOIC(210)-001-b

Device Symbol



The negative protection voltage is controlled by the voltage, V_{GG}, applied to the G terminal.

SD-TISP6-001-a

How To Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP61089HDM	8-SOIC (210 mil)	Embossed Tape Reeled	TISP61089HDMR-S	61089H	2000

Description

The TISP61089HDM is a dual forward-conducting buffered p-gate thyristor (SCR) overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61089HDM limits voltages that exceed the SLIC supply rail voltage. The TISP61089HDM parameters are specified to allow equipment compliance with Telcordia GR-1089-CORE, Issue 3 and ITU-T recommendations K.20, K.21 and K.45.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -20 V to -155 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
MAY 2004 – REVISED AUGUST 2007

TISP61089HDM Overvoltage Protector

BOURNS®

Description (Continued)

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector SCR will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of TISP61089HDM SCR helps prevent d.c. latchup.

The TISP61089HDM is designed to be used with a pair of Bourns® B1250T fuses for overcurrent protection. Level 2 power fault compliance requires the series overcurrent element to become open-circuit or high impedance. For equipment compliant to ITU-T recommendations K.20, K.21 or K.45 only, the series resistor value is set by the coordination requirements. For coordination with a 400 V limit GDT, a minimum series resistor value of 6.5 Ω is recommended.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0	V_{DRM}	-170	V
Repetitive peak gate-cathode voltage, V_{KA} = 0	V_{GKRM}	-167	V
Non-repetitive peak impulse current (see Notes 1, 2 and 3) 10/1000 µs (Telcordia GR-1089-CORE, Issue 3) 5/310 µs (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700 µs) 10/360 µs (Telcordia GR-1089-CORE, Issue 3) 1.2/50 µs voltage waveshape (Telcordia GR-1089-CORE, Issue 3), including 3 Ω non-inductive resistor 2/10 µs (Telcordia GR-1089-CORE, Issue 3)	I_{PPSM}	 100 150 100 500 500	A
Non-repetitive peak on-state current, 50 Hz / 60 Hz (see Notes 1, 2, 3 and 4) 0.5 s 1 s 2 s 5 s 30 s 900 s	I_{TSM}	 7.7 6.1 4.8 3.7 2.8 2.6	A
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES:
1. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Ratings are obtained by using the gate circuitry as shown in Fig. 3.
3. Rated currents only apply if pins 1 & 8 (Tip) are connected together, pins 4 & 5 (Ring) are connected together and pins 6 & 7 (Anode) are connected together.
4. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

	Parameter	Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_A = 25 °C T_A = 85 °C			-5 -50	µA
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	10/1000 µs, I_{TM} = 100 A, V_{GG} = -100 V 5/310 µs, I_{TM} = 150 A, V_{GG} = -100 V 2/10 µs, I_{TM} = 200 A, V_{GG} = -100 V (see Note 5)				12 12 20	V
V_F	Forward voltage	I_F = 5 A, t_W = 200 µs				3	V
V_{FRM}	Peak forward recovery voltage	10/1000 µs, I_F = 100 A, V_{GG} = -100 V 5/310 µs, I_F = 150 A, V_{GG} = -100 V 2/10 µs, I_F = 200 A, V_{GG} = -100 V (see Note 5)				6 7 10	V

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted) (Continued)

	Parameter	Test Conditions		Min	Typ	Max	Unit
I_H	Holding current	I_T = -1 A, di/dt = 1 A/ms, V_{GG} = -100 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_A = 25 °C T_A = 85 °C			-5 -50	µA
I_{GT}	Gate trigger current	I_T = -3 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -100 V				15	mA
V_{GT}	Gate-cathode trigger voltage	I_T = -3 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -100 V				2.5	V
C_{KA}	Cathode-anode off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = -50 V, I_G = 0				40	pF

NOTE: 5. Voltage measurements should be made with an oscilloscope with limited bandwidth (20 MHz) to avoid high frequency noise.

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-7 PCB, EIA/JESD51-2 Environment, P_{TOT} = 4 W (See Note 6)		55		°C/W

NOTE 6. EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Parameter Measurement Information

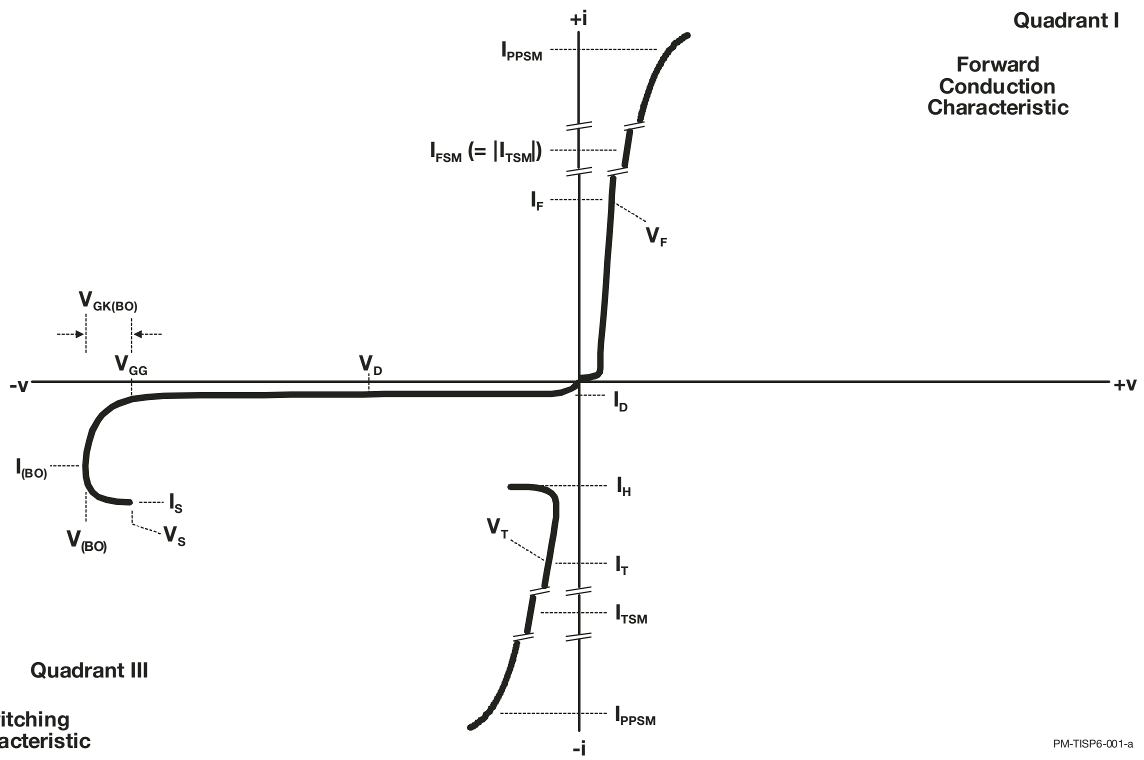


Figure 1. Voltage-Current Characteristic
Unless Otherwise Noted, All Voltages are Referenced to the Anode

Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

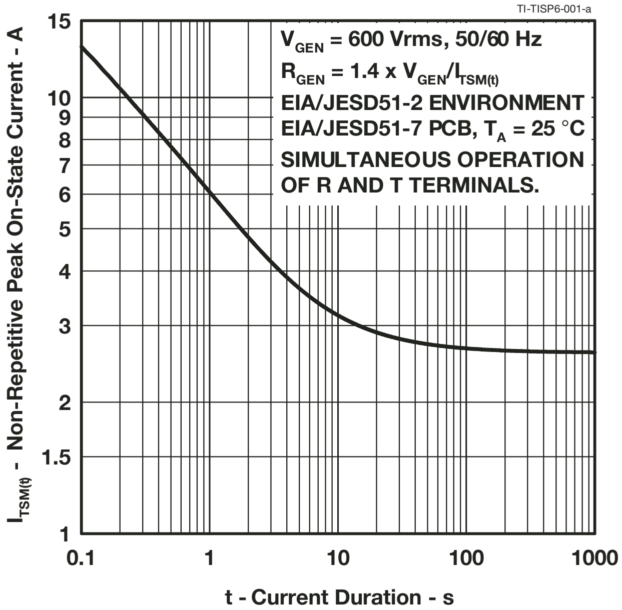


Figure 2.

APPLICATIONS INFORMATION

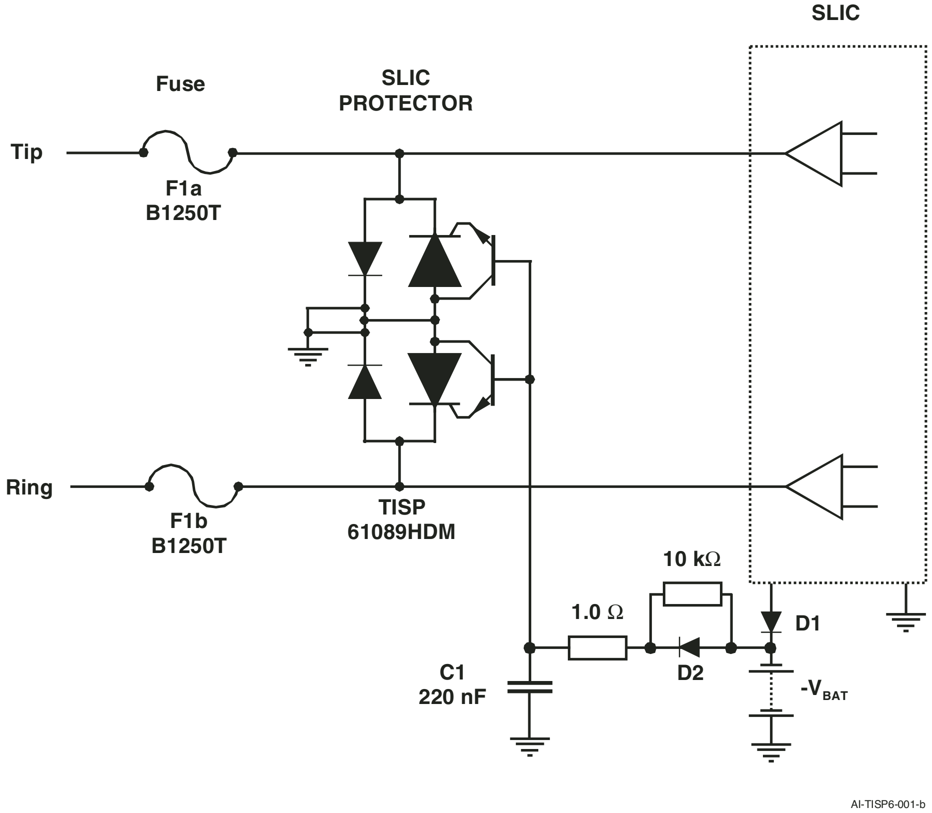


Figure 3. Line Protection with TISP61089HDM

Figure 3 illustrates how a typical SLIC protection circuit may look for a TISP61089HDM and a pair of Bourns® Telefuse™ overcurrent protectors. This is a generic circuit that is designed to withstand both lightning surge testing and AC power fault testing. As applications can differ, it is recommended you contact your Bourns representative for detailed applications guidance on your specific design.

APPLICATIONS INFORMATION (Continued)

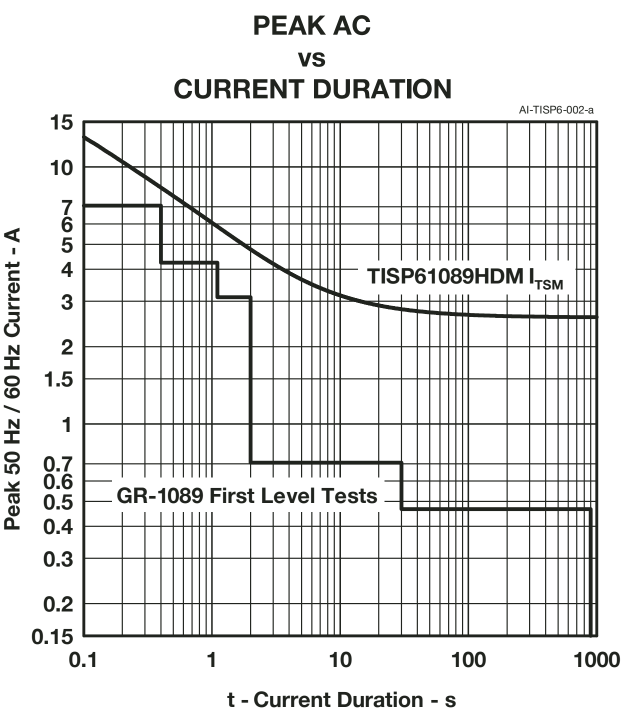


Figure 4.

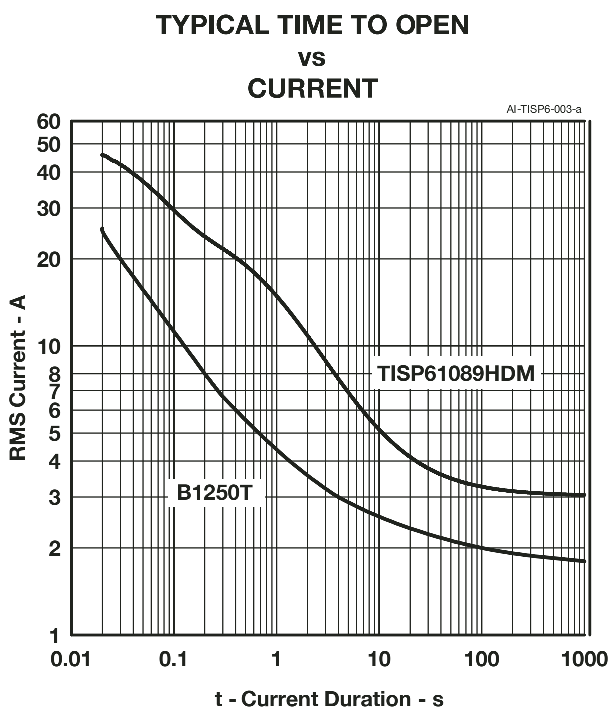


Figure 5.

GR-1089-CORE Issue A.C. Power Fault testing has been comprehended in the design of the TISP61089HDM. For compliance, circuit designs must pass both First Level and Second Level A.C. Power Fault testing.

First Level Power Fault testing requires that the equipment shall not be damaged and continues to operate correctly without disruption to other parts of the system. In laboratory tests it has been shown that the circuit shown in Figure 3 can pass these tests without damage. Figure 4 shows the TISP61089HDM I_{TSM} rating to be above the level of GR-1089-CORE First Level tests.

Second Level Power Fault testing may result in the equipment becoming non-operational, but any component failure should not allow the equipment to become a hazard. The system should not burn, fragment, or become an electrical safety hazard. The test data in Figure 5 illustrates that the TISP61089HDM and the B1250T are current coordinated, as the fuse interrupt time is shorter than the time it takes to damage the TISP61089HDM package for a given current.

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