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BTS737S3

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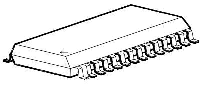
Smart High-Side Power Switch
Four Channels: 4 x 35mΩ
Advanced Current Sense

Product Summary

Operating Voltage	$V_{bb(on)}$	5.0 ...40V	
Active channels		one	four parallel
On-state Resistance	R_{ON}	35mΩ	9mΩ
Nominal load current	$I_{L(NOM)}$	5.4A	11.1A
Current limitation	$I_{L(SCr)}$	40A	40A

Package

P-DSO-28



General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Providing embedded protective functions

Applications

- µC compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive and capacitve loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

- Very low standby current
- Improved electromagnetic compatibility (EMC)
- CMOS compatible input
- Stable behaviour at undervoltage
- Wide operating voltage range

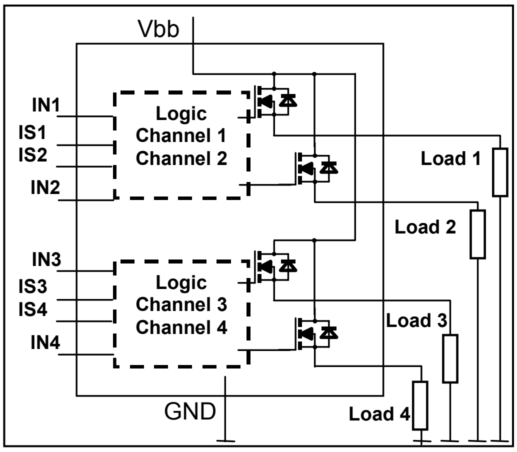
Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Reverse battery protection with external resistor
- Overvoltage protection with external resistor (incl. load dump)
- Loss of ground protection
- Electrostatic discharge protection (ESD)

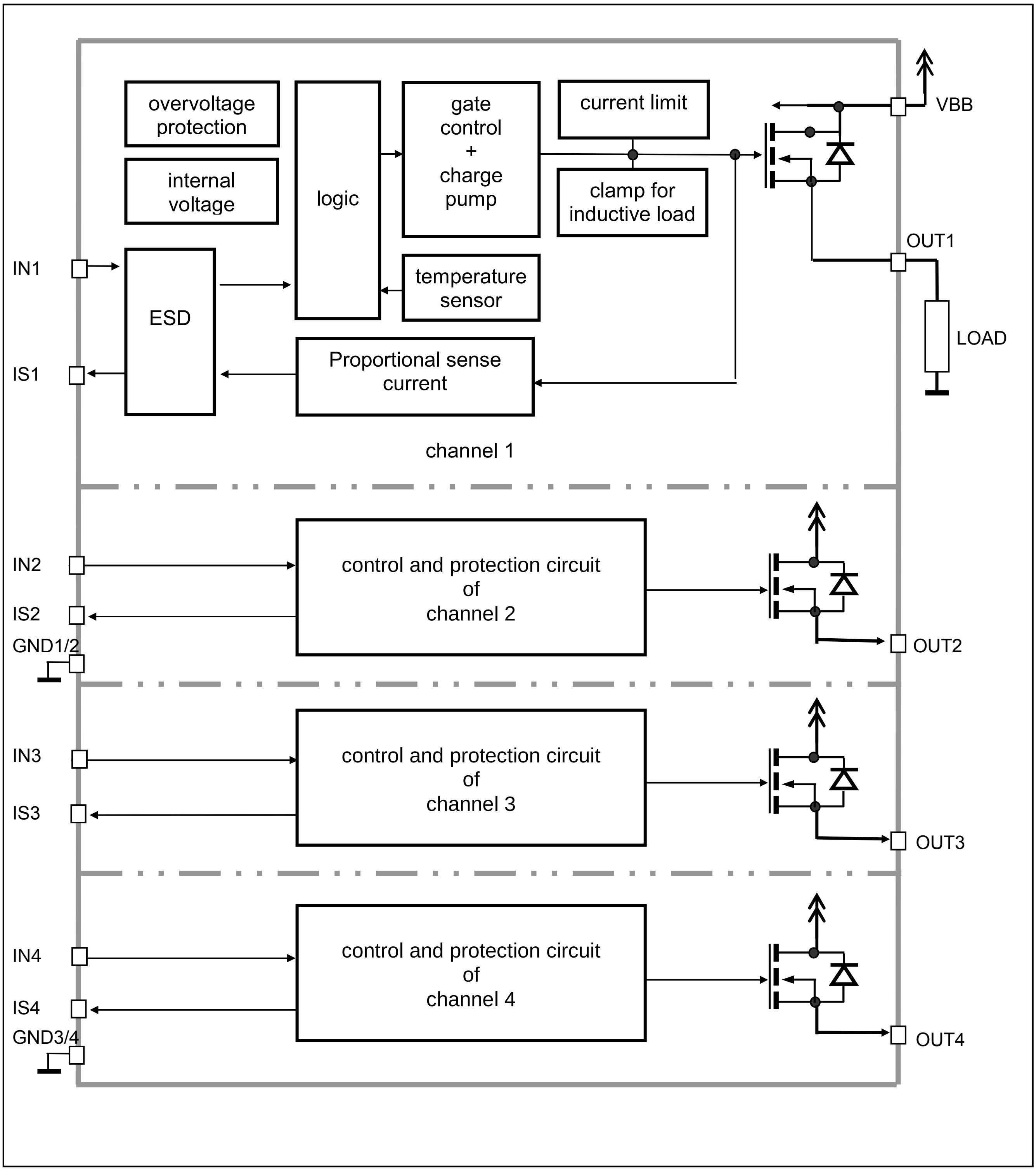
Diagnostic Function

- Proportional load current sense (with defined fault signal during thermal shutdown and current limit)

Block Diagram



Functional diagram

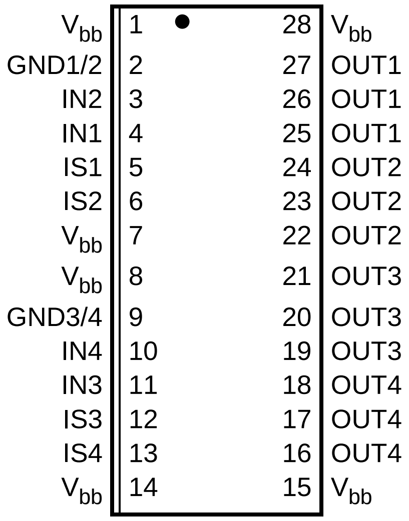

overvoltage protection
internal voltage
logic
gate control + charge pump
current limit
clamp for inductive load
VBB
OUT1
LOAD
IN1
ESD
temperature sensor
IS1
Proportional sense current
channel 1
IN2
IS2
GND1/2
control and protection circuit of channel 2
OUT2
IN3
IS3
control and protection circuit of channel 3
OUT3
IN4
IS4
GND3/4
control and protection circuit of channel 4
OUT4

Pin Definitions and Functions

Pin	Symbol	Function
1, 7, 8, 14, 15, 28	V_{bb}	**Positive power supply voltage**. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 4 and also for low thermal resistance
4	IN1	**Input 1,2, 3,4** activates channel 1,2,3,4 in case of logic high signal
3	IN2	
11	IN3	
10	IN4	
25,26,27	OUT1	**Output 1,2,3,4** protected high-side power output of channel 1,23,4. Design the wiring for the max. short circuit current
22,23,24	OUT2	
19,20,21	OUT3	
16,17,18	OUT4	
5	IS1	**Diagnostic feedback 1 .. 4** of channel 1 to 4 Providing a sense current, proportional to the load current
6	IS2	
12	IS3	
13	IS4	
2	GND1/2	**Ground** of chip 1 (channel 1,2)
9	GND3/4	**Ground** of chip 2 (channel 3,4)

Pin configuration

(top view)



V_{bb}	1	28	V_{bb}
GND1/2	2	27	OUT1
IN2	3	26	OUT1
IN1	4	25	OUT1
IS1	5	24	OUT2
IS2	6	23	OUT2
V_{bb}	7	22	OUT2
V_{bb}	8	21	OUT3
GND3/4	9	20	OUT3
IN4	10	19	OUT3
IN3	11	18	OUT4
IS3	12	17	OUT4
IS4	13	16	OUT4
V_{bb}	14	15	V_{bb}

Maximum Ratings at T_j = 25°C unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 6)	V_{bb}	40	V
Supply voltage for full short circuit protection1) $T_{j,start}$ = -40 ...+150°C	V_{bb}	36	V
Load current (Short-circuit current, see page 6)	I_L	$I_{L(lim)}$2)	
Load dump protection3) $V_{LoadDump} = V_A + V_s$, V_A = 13.5 V R_I4) = 2 Ω, t_d = 400 ms; IN = low or high, each channel loaded with R_L = 4.7 Ω,	$V_{Load\,dump}$5)	60	V
Operating temperature range	T_j	-40 ...+150	°C
Storage temperature range	T_{stg}	-55 ...+150	
Power dissipation (DC)6) T_a = 25°C: (all channels active) T_a = 85°C:	P_{tot}	3.7 1.9	W
Maximal switchable inductance, single pulse V_{bb} = 12V, $T_{j,start}$ = 150°C6), I_L = 4.0 A, E_{AS} = 0.8J, 0Ω one channel: I_L = 6.0 A, E_{AS} = 1.0J, 0Ω two parallel channels: I_L = 9.5 A, E_{AS} = 1.5J, 0Ω four parallel channels: see diagrams on page 10	Z_L	33 37 64	mH
Electrostatic discharge capability (ESD) IN: (Human Body Model) IS: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 R=1.5kΩ; C=100pF	V_{ESD}	1.0 4.0 8.0	kV
Input voltage (DC)	V_{IN}	-10 ... +16	V
Current through input pin (DC)	I_{IN}	±0.3	mA
Current through sense pin (DC)	I_{IS}	±0.3	
see internal circuit diagram page 9			

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1) Single pulse

2) Current limit is a protection function. Operation in current limitation is considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 75Ω resistor for the GND connection is recommended.

4) R_I = internal resistance of the load dump test pulse generator

5) $V_{Load\,dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

6) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

Thermal Characteristics

Parameter and Conditions		Symbol	Values			Unit
			min	typ	Max	
Thermal resistance junction - soldering point[7][8],	each channel:	R_{thjs}	--	--	11	K/W
junction – ambient[8]		R_{thja}				
@ 6 cm^2 cooling area	one channel active:		--	40	--	
	all channels active:		--	33	--	

Electrical Characteristics

Parameter and Conditions, each of the four channels at T_j = -40...+150°C, V_{bb} = 12 V unless otherwise specified		Symbol	Values			Unit
			min	typ	Max	
Load Switching Capabilities and Characteristics						
On-state resistance (V_{bb} to OUT); I_L = 5 A	each channel, T_j = 25°C:	R_{ON}	--	30	35	mΩ
see diagram, page 11	T_j = 150°C:		--	55	64	
Nominal load current	one channel active:	$I_{L(NOM)}$	5.0	5.4	--	A
	two parallel channels active:		6.7	7.4	--	
	four parallel channels active:		10.5	11.1	--	
Device on PCB[8], T_a = 85°C, $T_j \le$ 150°C						
Output current while GND disconnected, V_{IN} = 0, see diagram page 10; (not subject to production test - specified by design)		$I_{L(GNDhigh)}$	--	--	1	mA
Turn-on time[9]	IN _⌐‾ to 90% V_{OUT}:	t_{on}	--	50	150	µs
Turn-off time	IN ‾¬_ to 10% V_{OUT}:	t_{off}	--	120	250	
$R_L = 12\,\Omega$						
Slew rate on[9] V_{OUT} rising from 10 to 30% of V_{bb}, $R_L = 12\,\Omega$:		dV/dt_{on}	0.2	--	0.9	V/µs
Slew rate off[9] V_{OUT} falling from 70 to 40% of V_{bb}, $R_L = 12\,\Omega$:		$-dV/dt_{off}$	0.1	--	0.9	V/µs

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[7] Soldering point: upper side of solder edge of device pin 7,8. See page 16.

[8] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

[9] See timing diagram on page 12.

Operating Parameters

Operating voltage	$V_{bb(on)}$	5.0	--	40	V
Overvoltage protection[10] $I_{bb} = 40$ mA	$V_{bb(AZ)}$	41	47	52	V
Standby current[11] T_j =-40...25°C:	$I_{bb(off)}$	--	10	25	µA
$V_{IN} = 0$; see diagram page 12 T_j =150°C:		--	40	80	
T_j =125°C: (not subject to production test - specified by design)			--	25	
Off-State output current T_j =-40...25°C:	$I_{L(off)}$	--	1	6	µA
(included in $I_{bb(off)}$) $V_{IN} = 0$; each channel; T_j=150°C:		--	--	15	
Operating current, $V_{IN} = 5$V, $I_{GND} = I_{GND1/2} + I_{GND3/4}$, one channel on:	I_{GND}	--	1.6	--	mA
four channels on:		--	6.0	--	

Protection Functions[12]

Current limit, (see timing diagrams, page 13)	$I_{L(lim)}$	36	45	58	A
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel	$I_{L(SCr)}$	--	40	--	A
two,three or four parallel channels		--	40		
(see timing diagrams, page 13)				--	
Initial short circuit shutdown time $T_{j,start}$ =25°C: (see timing diagrams on page 13)	$t_{off(SC)}$	--	4	--	ms
Output clamp (inductive load switch off)[13] at $V_{ON(CL)} = V_{bb} - V_{OUT}$, $I_L = 40$ mA	$V_{ON(CL)}$	41	47	52	V
Thermal overload trip temperature	T_{jt}	150	--	--	°C
Thermal hysteresis	ΔT_{jt}	--	10	--	K

Reverse Battery[14] (not subject to production test - specified by design)

Reverse battery voltage	$-V_{bb}$	--	--	14	V
Drain-source diode voltage ($V_{out} > V_{bb}$) I_L = -2A; Tj = +150°C:	$-V_{ON}$	--	500	--	mV

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[10] Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 75Ω resistor for the GND connection is recommended). See also $V_{ON(CL)}$ in table of protection functions and circuit diagram on page 9.

[11] Measured with load; for the whole device; all channels off.

[12] Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

[13] If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$.

[14] Requires a 75 Ohm resistor in the GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode.
The temperature protection and sense functionality is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 4 and circuit page 9).

Input[15]

Input resistance (see circuit page 9)	R_I	2.5	3.5	6.0	kΩ
Input turn-on threshold voltage	$V_{IN(T+)}$	1.7	--	3.2	V
Input turn-off threshold voltage	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.3	--	V
Off state input current V_{IN} = 0.4 V:	$I_{IN(off)}$	1	--	35	µA
On state input current V_{IN} = 5 V:	$I_{IN(on)}$	20	50	90	µA

Diagnostic Characteristics

Current sense ratio, static on-condition, $k_{ILIS} = I_L : I_{IS}$	k_{ILIS}	--	5 300	--	
I_L = 10 A:		4575	5300	6000	
I_L = 2 A:		4100	5300	6300	
I_L = 1 A:		4200	5300	6600	
I_L = 0.5 A:		3580	5800	8080	
Sense signal in case of fault-conditions[16]	V_{fault}	5.4	6.3	7.5	V
Sense signal delay after thermal shutdown[17] (not subject to production test - specified by design)	$t_{delay(fault)}$	--	--	1	ms
Sense current saturation	$I_{IS,lim}$	4	--	--	mA
Current sense output voltage limitation $I_{IS} = 0$, $I_L = 5$ A:	$V_{IS(lim)}$	5.4	6.3	7.5	V
Current sense leakage/offset current $V_{IN}=0$, $V_{IS} = 0$, $I_L = 0$:	$I_{IS(LL)}$	--	--	1	µA
$V_{IN}=5$ V, $V_{IS} = 0$, $I_L = 0$:	$I_{IS(LH)}$	--	2.5	--	
Current sense settling time to $I_{IS\ static}$ ±10% after positive input slope, I_L = 0 5 A, (not subject to production test - specified by design)	$t_{son(IS)}$	--	--	300	µs

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[15] If ground resistors R_{GND} are used, add the voltage drop across these resistors.

[16] In the case of current limitation or thermal shutdown the sense signal is no longer a current proportional to the load current, but a fixed voltage of typ. 6 V.

[17] In the case of thermal shutdown the V_{fault} signal remains for $t_{delay(fault)}$ longer than the restart of the switch (see diagram on page 14).

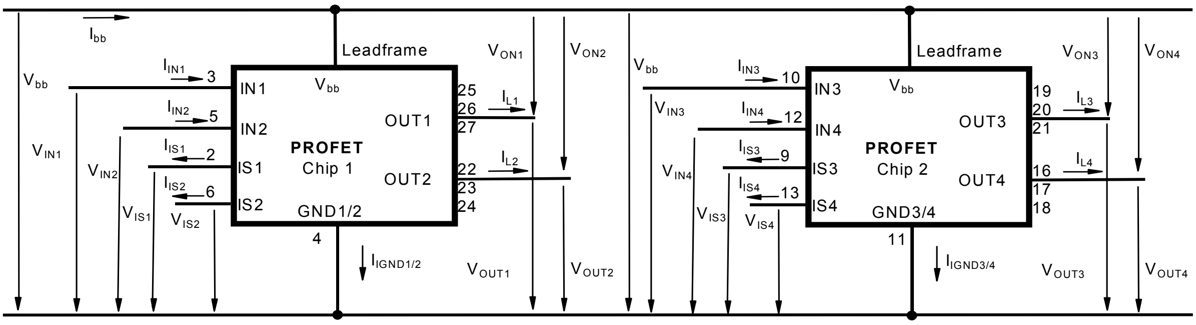
Truth Table

	Input level	Output level	Current Sense IIS
Normal Operation	**L** **H**	**L** **H**	**0** **nominal**
Current-Limitation18)	**H**	**H**	V_{fault}
Short circuit to GND	**L** **H**	**L** **L**	**0** V_{fault}
Overtemperature	**L** **H**	**L** **L**	**0** V_{fault}
Short circuit to Vbb	**L** **H**	**H** **H**	**0** **<nominal**19)
Open load	**L** **H**	**Z** **H**	**0** **0**
Negative output Voltage clamp	**L**	**L**	**0**

L = "Low" Level   X = don't care   Z = high impedance, potential depends on external circuit
H = "High" Level V_{fault} = 6V typ, constant voltage independent of external used sense resistor.

Parallel switching of channels is possible by connecting the inputs and outputs in parallel. The current sense outputs have to be connected with a single sense resistor.

Terms


I_{bb}
V_{bb}
V_{IN1}
V_{IN2}
V_{IS1}
V_{IS2}
I_{IN1} 3
I_{IN2} 5
I_{IS1} 2
I_{IS2} 6
Leadframe
IN1
IN2
IS1
IS2
V_{bb}
PROFET
Chip 1
OUT1
OUT2
GND1/2
4
$I_{GND1/2}$
25
26
27
22
23
24
I_{L1}
I_{L2}
V_{ON1}
V_{ON2}
V_{OUT1}
V_{OUT2}
V_{bb}
V_{IN3}
V_{IN4}
V_{IS3}
V_{IS4}
I_{IN3} 10
I_{IN4} 12
I_{IS3} 9
I_{IS4} 13
Leadframe
IN3
IN4
IS3
IS4
V_{bb}
PROFET
Chip 2
OUT3
OUT4
GND3/4
11
$I_{GND3/4}$
19
20
21
16
17
18
I_{L3}
I_{L4}
V_{ON3}
V_{ON4}
V_{OUT3}
V_{OUT4}

Leadframe (V_{bb}) is connected to pin 1, 7, 8, 14, 15, 28.

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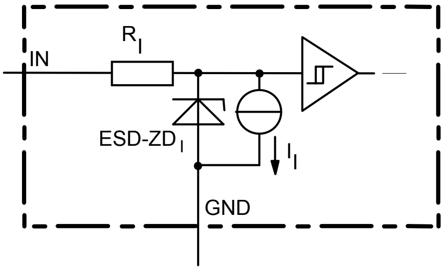
18) Current limitation is only possible while the device is switched on.

19) Low ohmic short to V_{bb} may reduce the output current I_L and therefore also the sense current I_{IS}.

Input circuit (ESD protection), IN1 to IN4


IN
R_I
ESD-ZD I
I_I
GND

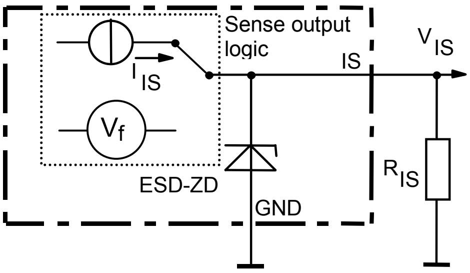
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Sense output

Normal operation: $I_S = I_L / k_{ILIS}$

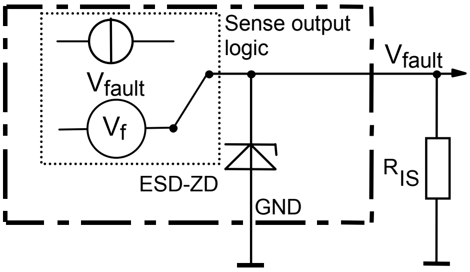
$V_{IS} = I_S * R_{IS}$; $R_{IS} = 1$ kΩ nominal

$R_{IS} > 500\Omega$


Sense output logic
I_{IS}
V_f
IS
V_{IS}
ESD-ZD
GND
R_{IS}

ESD-Zener diode: V_{ESD} = 6.1 V typ., max 14 mA;

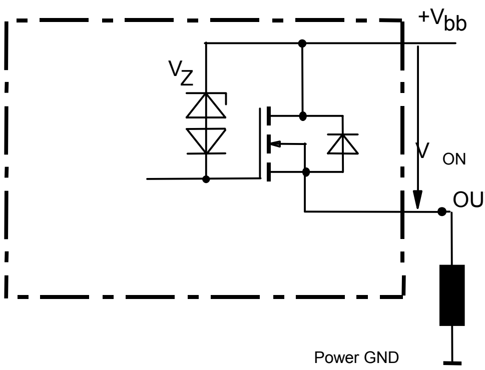
Operation under fault condition so as thermal shut down or current limitation


Sense output logic
V_{fault}
V_f
V_{fault}
ESD-ZD
GND
R_{IS}

V_{fault} = 6V typ

$V_{fault} < V_{ESD}$ under all conditions

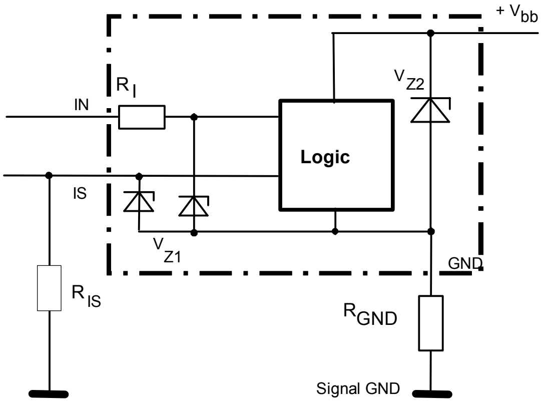
Overvoltage output clamp, OUT1 or OUT2


$+V_{bb}$
V_Z
V_{ON}
OUT
Power GND

V_{ON} clamped to $V_{ON(CL)}$ = 47 V typ.

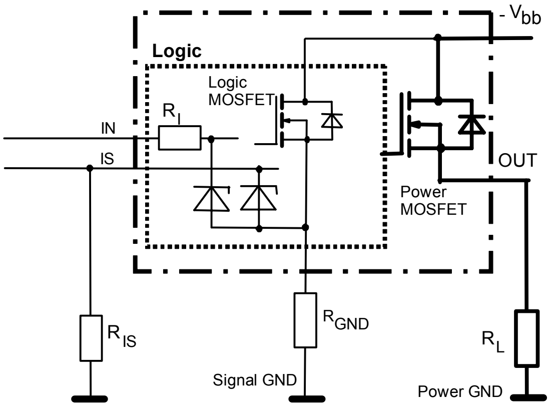
Overvoltage protection of logic part

GND1/2 or GND3/4


$+ V_{bb}$
R_I
IN
V_{Z2}
Logic
IS
V_{Z1}
GND
R_{IS}
R_{GND}
Signal GND

V_{Z1} = 6.1 V typ., V_{Z2} = 47 V typ., R_I = 3.5 kΩ typ., R_{GND} = 75 Ω

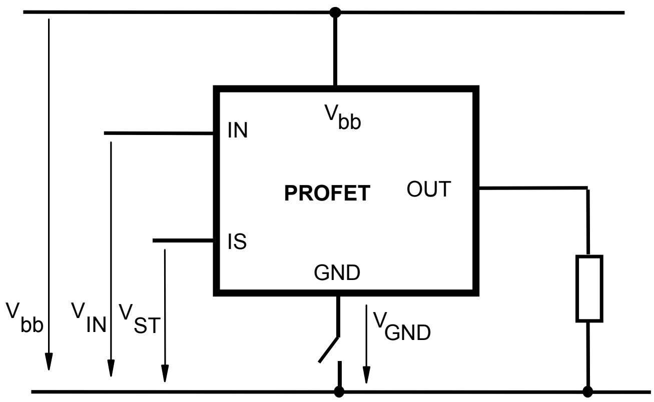
Reverse battery protection


$- V_{bb}$
Logic
Logic MOSFET
R_I
IN
IS
OUT
Power MOSFET
R_{IS}
R_{GND}
R_L
Signal GND
Power GND

R_{GND} = 75 Ω, R_I = 3.5 kΩ typ,

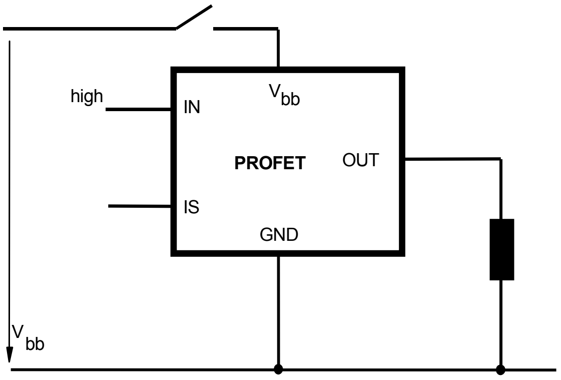
Temperature protection and sense functionality is not active during inverse current operation.

GND disconnect



Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$.
Due to $V_{GND} > 0$, no V_{ST} = low signal available.

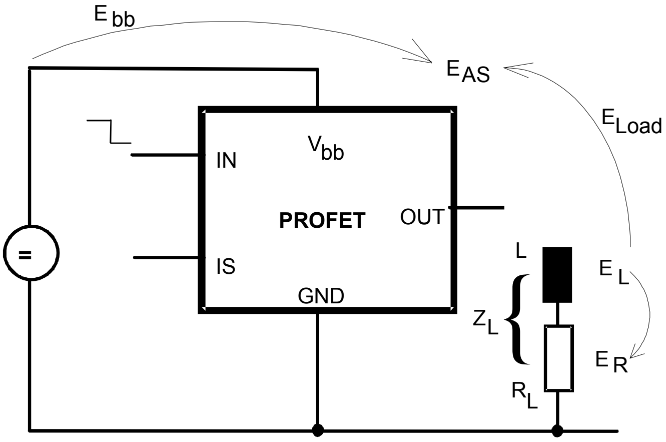
Vbb disconnect with energized inductive load



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 10) each switch is protected against loss of V_{bb}.

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = {}^1\!/_2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

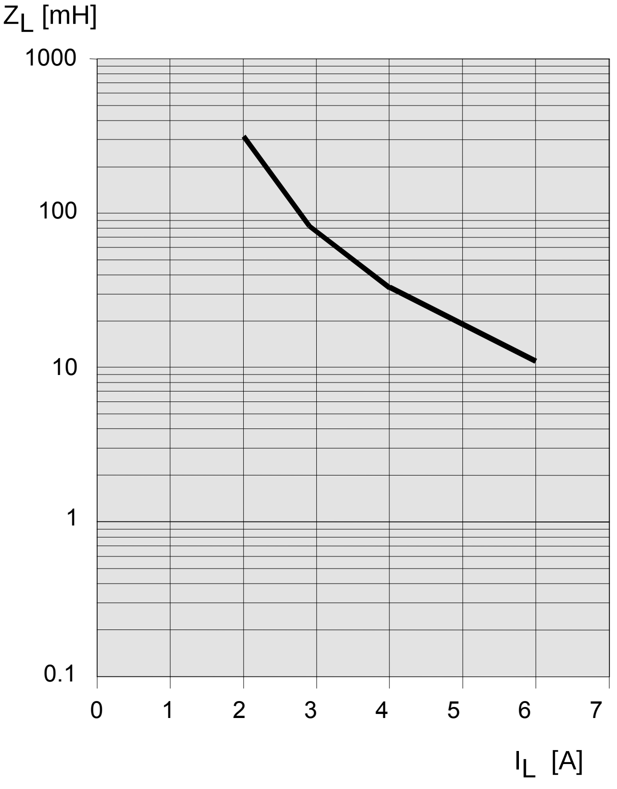
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t)\,dt,$$

with an approximate solution for $R_L > 0\,\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L}\left(V_{bb} + |V_{OUT(CL)}|\right)\ ln\left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

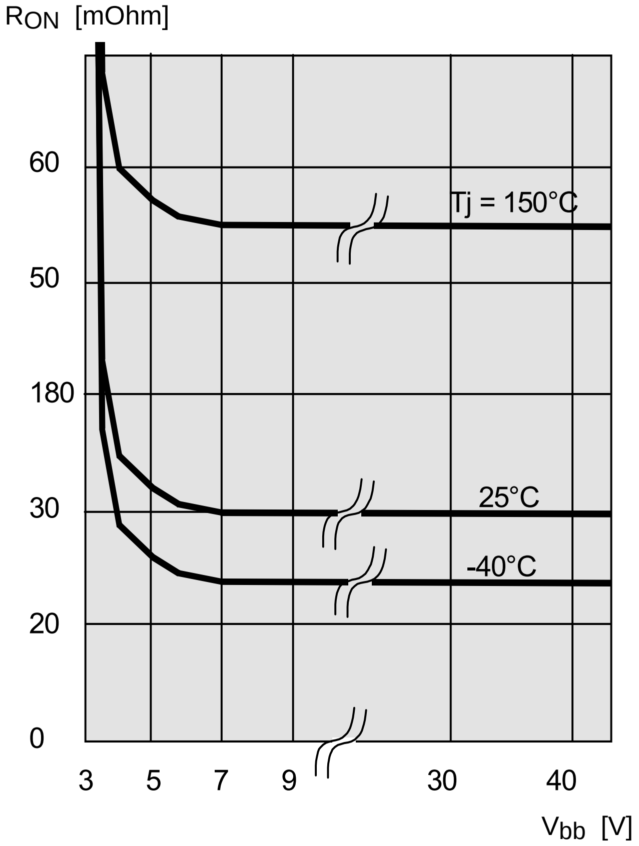
Maximum allowable load inductance for a single switch off (one channel)[6)]

$L = f(I_L)$; $T_{j,start} = 150°C$, $V_{bb} = 12\,V$, $R_L = 0\,\Omega$



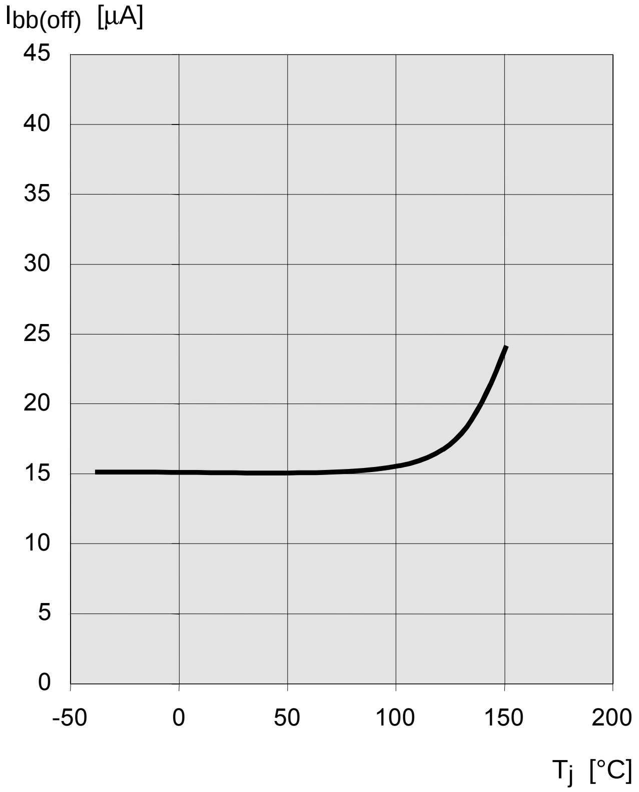
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$; I_L = 2 A, IN = high



Typ. standby current

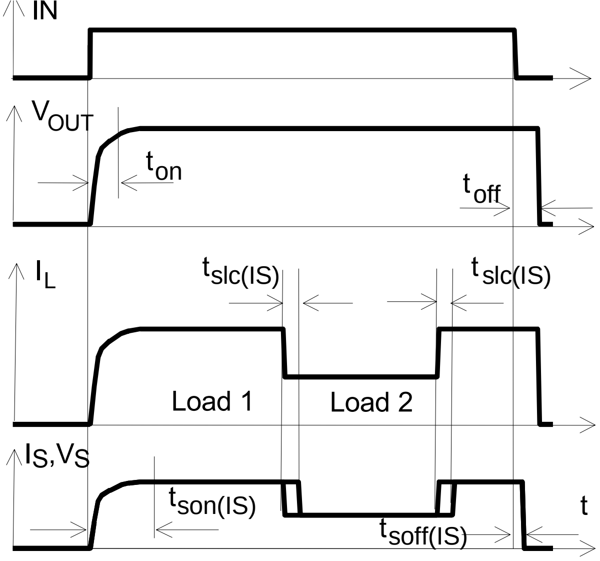
$I_{bb(off)} = f(T_j)$; V_{bb} = 9...34 V, IN1,2,3,4 = low



Functionality diagrams

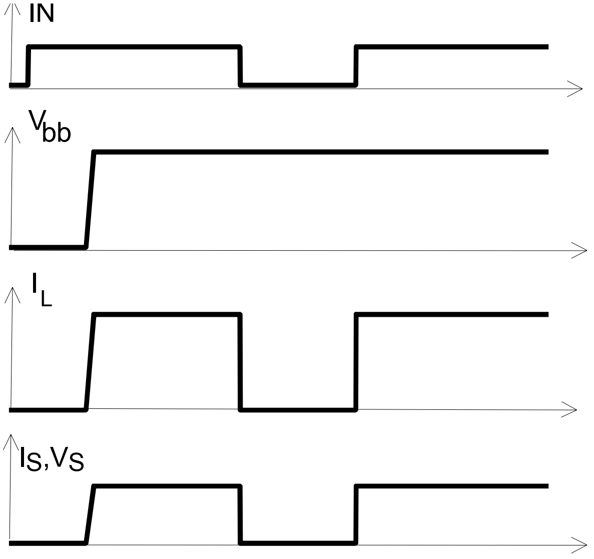
All diagrams are shown for chip 1 (channel 1/2). For chip 2 (channel 3/4) the diagrams are valid too. The channels 1 and 2, respectively 3 and 4, are symmetric and consequently the diagrams are valid for each channel as well as for permuted channels

Figure 1a: Switching a resistive load, change of load current in on-condition:



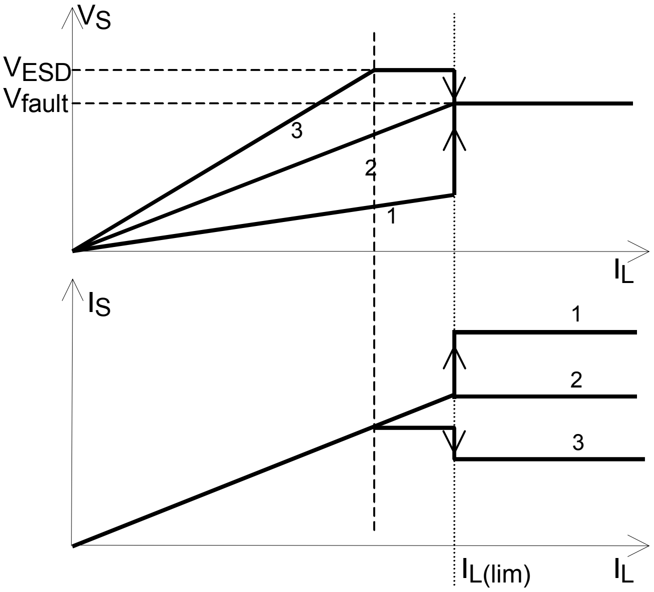
The sense signal is not valid during settling time after turn on or change of load current.

Figure 1b: V_{bb} turn on:



proper turn on under all conditions

Figure 1c: Behaviour of sense output:
Sense current (I_S) and sense voltage (V_S) as function of load current dependent on the sense resistor
Shown is V_S and I_S for three different sense resistors. Curve 1 refers to a low resistor, curve 2 to a medium-sized resistor and curve 3 to a big resistor. Note, that the sense resistor may not fall short of a minimum value of 500Ω.

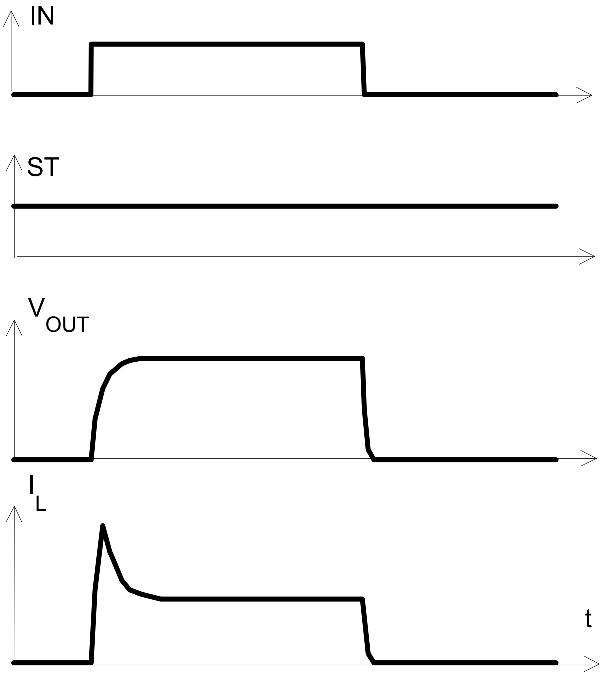


$I_S = I_L / k_{ILIS}$

$V_{IS} = I_S * R_{IS}$; R_{IS} = 1 kΩ nominal

$R_{IS} > 500\Omega$

Figure 2a: Switching a lamp:


IN
ST
VOUT
IL
t

The initial peak current should be limited by the lamp and not by the current limit of the device.

Figure 2b: Switching a lamp with current limit:
The behaviour of IS and VS is shown for a resistor, which refers to curve 1 in figure 1c

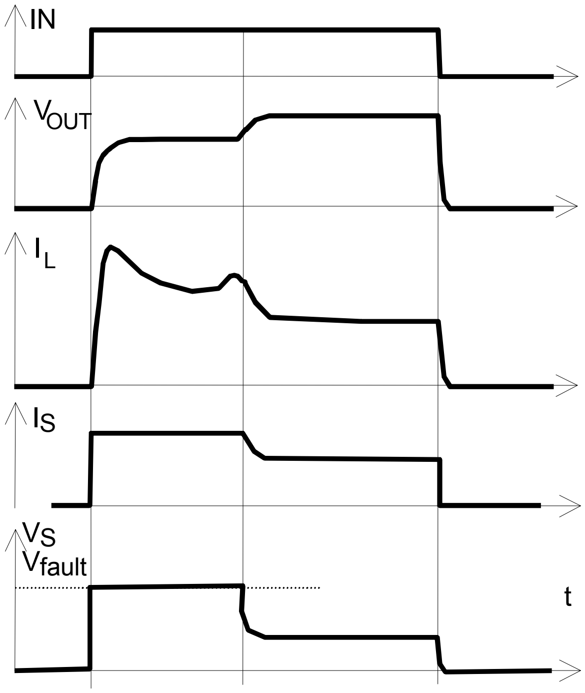
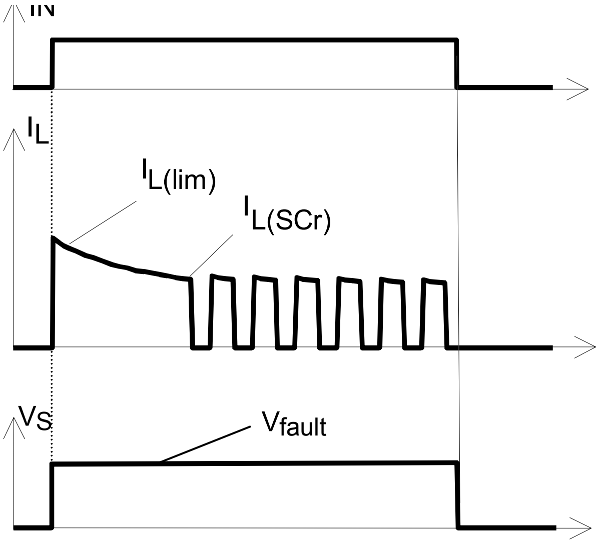

IN
VOUT
IL
IS
VS
Vfault
t

Figure 3a: Short circuit:
shut down by overtempertature, reset by cooling


IN
IL
IL(lim)
IL(SCr)
VS
Vfault

Heating up may require several milliseconds, depending on external conditions
$I_{L(lim')}$ = 45 A typ. increases with decreasing temperature.

Figure 3b: Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)

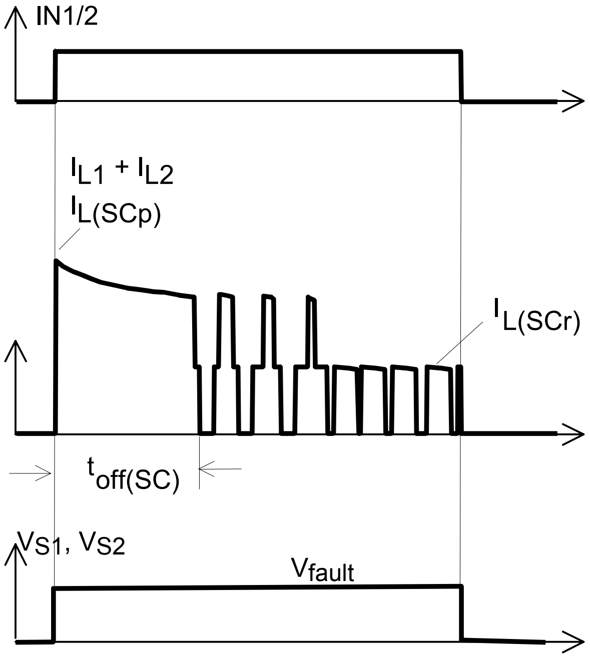

IN1/2
IL1 + IL2
IL(SCp)
IL(SCr)
toff(SC)
VS1, VS2
Vfault

Figure 4a: Overtemperature:
Reset if $T_j < T_{jt}$
The behaviour of IS and VS is shown for a resistor, which refers to curve 1 in figure 1c

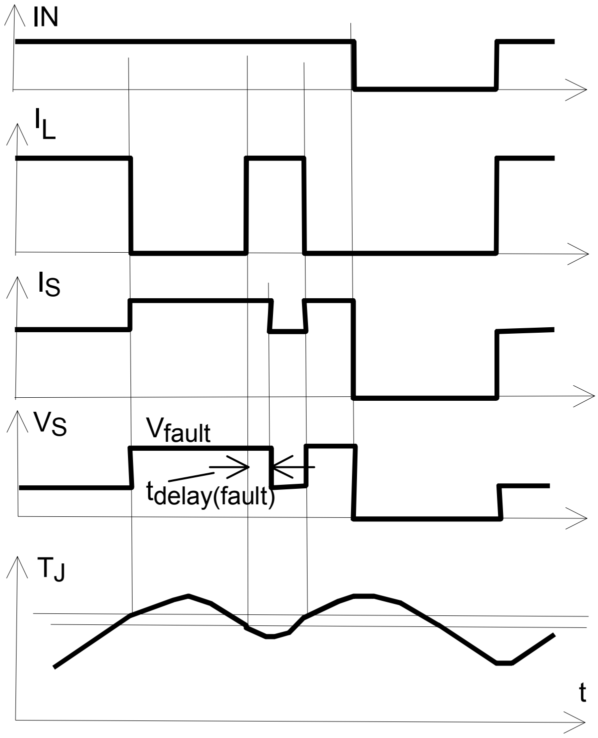


Figure 6a: Current sense versus load current:

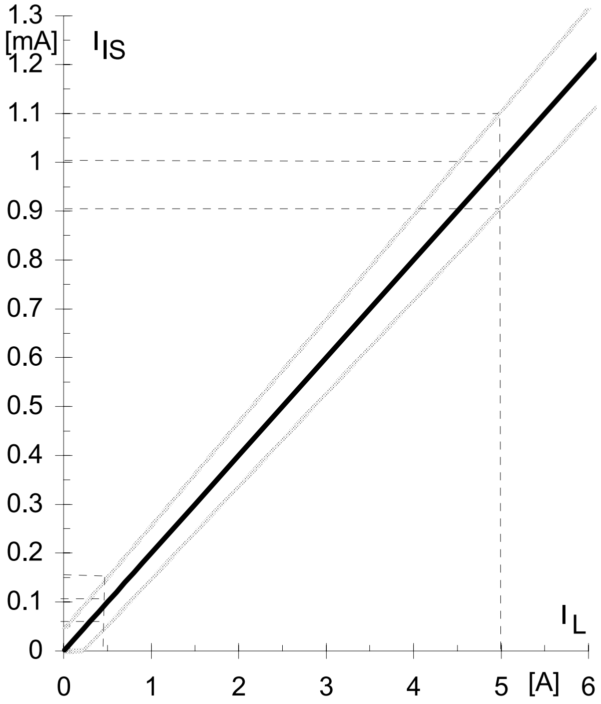
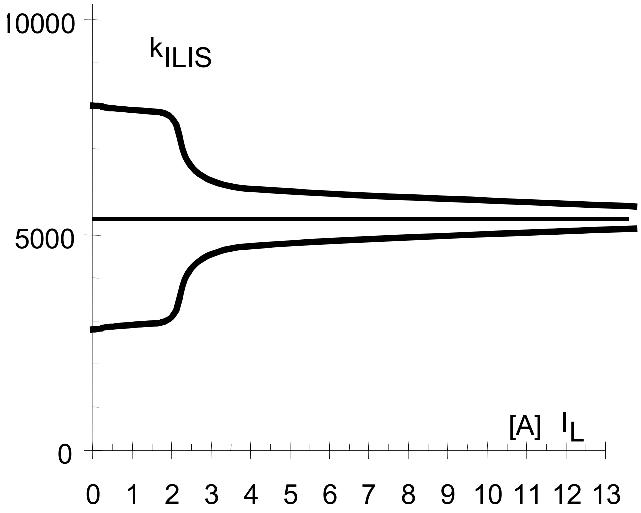


Figure 6b: Current sense ratio[20]:



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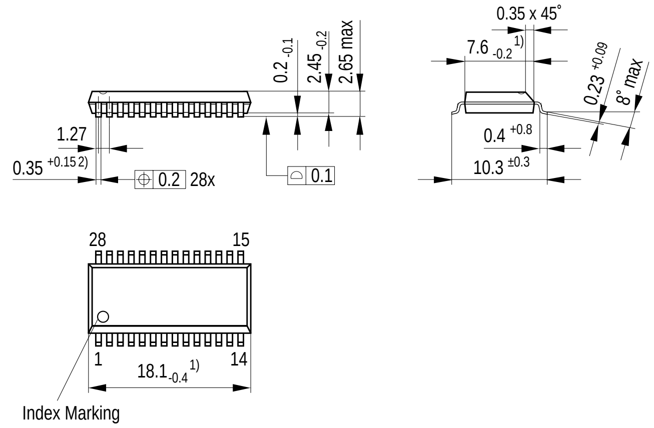
[20] This range for the current sense ratio refers to all devices. The accuracy of the k_{ILIS} can be raised at least by a factor of two by calibrating the value of k_{ILIS} for every single device.

Package and Ordering Code

Standard: P-DSO-28-16

Sales Code	BTS 737 S3
Ordering Code	Q67060-S6133

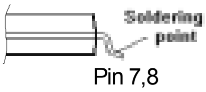


1) Does not include plastic or metal protrusions of 0.15 max rer side

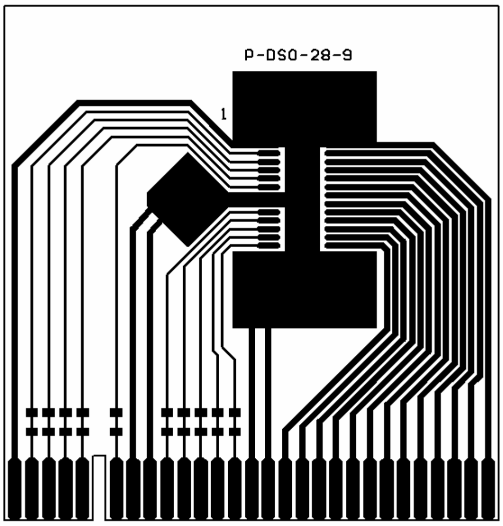
2) Does not include dambar protrusion of 0.05 max per side

All dimensions in millimetres

Definition of soldering point with temperature T_S: upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer 70µm, $6cm^2$ active heatsink area) as a reference for max. power dissipation P_{tot}, nominal load current $I_{L(NOM)}$ and thermal resistance R_{thja}



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