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Data Sheet

TDA21102

High speed Driver with bootstrapping for dual Power MOSFETs



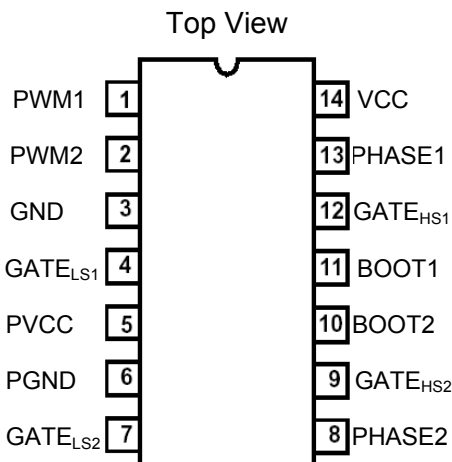
P-DSO-14-3

Features

- Fast rise and fall times for frequencies up to 2 MHz
- Capable of sinking more than 4 A peak current for lowest switching losses
- Charges the High Side and Low Side MOSFET's gate to 5..12 V according to PVCC setting.
- Adjustable High Side and Low Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- High voltage rating on Phase node
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
- Ideal for multi-phase Desktop CPU supplies on motherboards and VRM's

Type	Package	Marking	Ordering Code
TDA21102	P-DSO-14-3	21102	Q67042-S4244

Pinout & Description



Number	Name	Description
1	PWM1	Input for the PWM1 controller signal
2	PWM2	Input for the PWM2 controller signal
3	GND	Ground
4	GATE _{LS1}	Gate drive output for the N-Channel Low Side MOSFET 1.
5	PVCC	Input to adjust the High Side gate drive
6	PGND	Power ground return for the Low Side Drivers
7	GATE _{LS2}	Gate drive output for the N-Channel Low Side MOSFET 2.
8	PHASE2	To be connected to the junction of the High Side and the Low Side MOSFET 2
9	GATE _{HS2}	Gate drive output for the N-Channel High Side MOSFET 2.
10	BOOT2	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 2.
11	BOOT1	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 1.
12	GATE _{HS1}	Gate drive output for the N-Channel High Side MOSFET 1.
13	PHASE1	To be connected to the junction of the High Side and the Low Side MOSFET 1
14	VCC	Supply Voltage



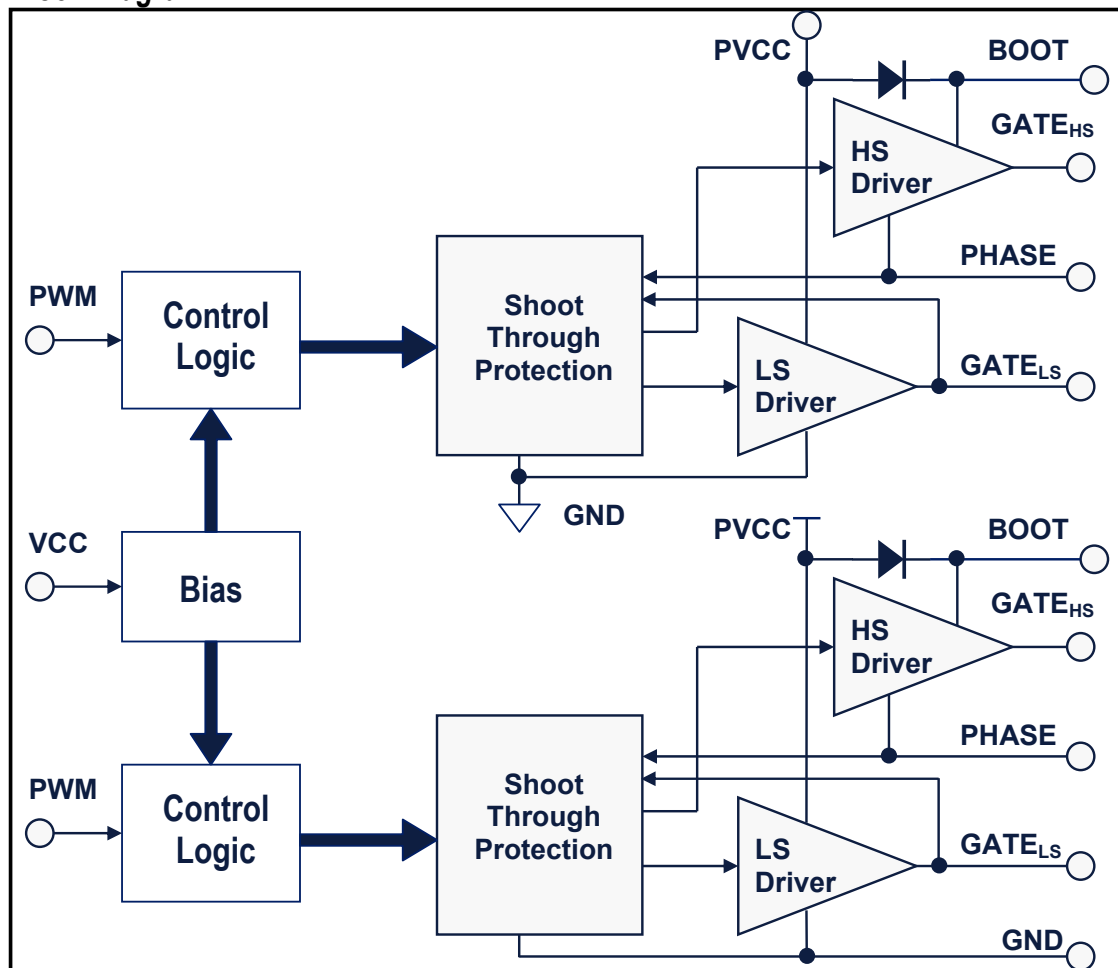
General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration as the HIP6602B. In addition it provides several protection features as well as a shut down mode for efficiency reasons. The high breakdown voltage makes it suitable for mobile applications.

Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver's capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM's but also in motor drive and class-D amplifier type applications.

Block Diagram





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Absolute Maximum Ratings

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin	V _{VCC}	-0.3	25	V
Voltage supplied to 'PVCC' pin	V _{PVCC}	-0.3	25	
Voltage supplied to 'PWM' pin	V _{PWM}	-0.3	5.5	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	V _{BOOT} – V _{PHASE}	-0.3	25	
Voltage rating at 'PHASE' pin, DC	V _{PHASE}	-1	25	
Voltage rating at 'PHASE' pin, t _{pulse_max} =500ns Max Duty Cycle = 2%		-20	30	
Voltage supplied to GATE _{HS} pin referenced to 'PHASE' T _{pulse_max} < 100ns, E < 2µJ	V _{GATEHS}	-3.5	V _{BOOT} +0.3	
Voltage supplied to GATE _{LS} pin referenced to 'GND' T _{pulse_max} < 100ns, E < 2µJ	V _{GATELS}	-5	V _{VCC} +0.3	
Junction temperature	T _J	-25	150	°C
Storage temperature	T _S	-55	150	
ESD Rating; Human Body Model			4	kV
IEC climatic category; DIN EN 60068-1			55/150/56	-

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-solder joint (pin 4)	Rth-JS		40.5		K/W
Thermal resistance, junction-case	Rth-JC		44.7		
Thermal resistance, junction-ambient	Rth-JA		116.2		



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Electrical Characteristic

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
Bias supply current	I _{VCC}	f = 1 MHz, NO LOAD V _{PVCC} = V _{VCC} = 12 V		1.3	1.8	mA
Quiescent current	I _{VCCQ}	1.8 V ≤ V _{PWM} ≤ 3.0 V		3.8	4.9	
Power supply current	I _{PVCC}	f = 1 MHz, NO LOAD V _{PVCC} = V _{VCC} = 12 V		25	33	
Under-voltage lockout		V _{VCC} rising threshold	9.7	10.1	10.5	V
Under-voltage lockout		V _{VCC} falling threshold	7.3	7.6	8.0	V
Input Characteristic						
Current in 'PWM' pin	I _{PWM_L}	V _{PWM} = 0.4 V	-80	115	-150	μA
Current in 'PWM' pin	I _{PWM_H}	V _{PWM} = 4.5 V	120	180	250	
Shut down window	V _{IN_SHUT}	t _{SHUT} > 350 ns	1.7		3.1	V
Shut down hold-off time	t _{SHUT}	1.7 V ≤ V _{PWM} ≤ 3.1 V	100	200	320	ns
PWM pin open	V _{PWM_O}		1.8	2.0	2.2	V
PWM Low level threshold (falling)	V _{PWM_L}				1.4	
PWM High level threshold (rising)	V _{PWM_H}		3.7			
Pulse Width High Side	t _p	= Pulse with on PWM pin	40			ns

At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic						
Turn-on propagation Delay High Side*	t _{d(ON)_HS}	P _{PVCC} = V _{VCC} = 12 V C _{ISS} = 3000 pF		18	35	ns
Turn-off propagation delay High Side	t _{d(OFF)_HS}			18	25	
Rise time High Side	t _{r_HS}			14	28	
Fall time High Side	t _{f_HS}			14	22	
Turn-on propagation Delay Low Side	t _{d(ON)_LS}			17	23	
Turn-off propagation delay Low Side	t _{d(OFF)_LS}			14	20	
Rise time Low Side	t _{r_LS}			22	29	
Fall time Low Side	t _{f_LS}			14	22	



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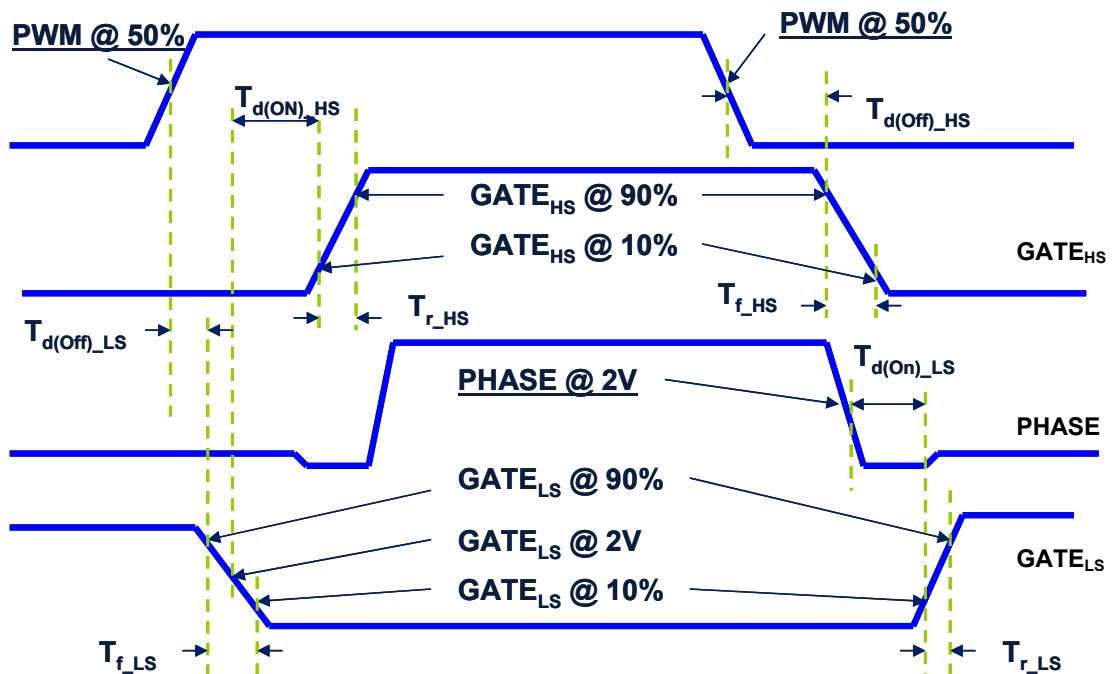
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At $T_j = 125\text{ }^\circ\text{C}$, unless otherwise specified

Dynamic Characteristic					
Turn-on propagation Delay High Side*	$t_{d(ON_HS)}$	$P_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$	22		ns
Turn-off propagation delay High Side	$t_{d(OFF_HS)}$		22		
Rise time High Side	t_{r_HS}		16		
Fall time High Side	t_{f_HS}		16		
Turn-on propagation Delay Low Side	$t_{d(ON_LS)}$		20		
Turn-off propagation delay Low Side	$t_{d(OFF_LS)}$		18		
Rise time Low Side	t_{r_LS}		23		
Fall time Low Side	t_{f_LS}		16		

Measurement Timing diagram





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Operating Conditions

At T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pin	V _{VCC}		10.8		13.2	V
Voltage supplied to 'PVCC' pin	V _{PVCC}		5		13.2	V
Input signal transition frequency	f		0.1		2	MHz
Power dissipation	P _{TOT}	T _A = 25 °C, T _J = 125 °C		0.9		W
Junction temperature	T _J		-25		150	°C

At T_j = 25 °C, unless otherwise specified

Parameter	Conditions	Values			Unit	
		Min.	Typ.	Max.		
Output Characteristic High Side (HS) and Low Side (LS), ensured by design						
Output Resistance	HS; Source	P _{PVCC} = V _{VCC} = 12 V I _{HS_SRC} = 2 A		1 ⁽¹⁾		Ω
	HS; Sink	V _{VCC} = 12 V, P _{PVCC} = 5V		1	1.3	Ω
	HS; Sink	P _{PVCC} = V _{VCC} = 12 V		0.9	1.2	Ω
Output Resistance	LS; Source	P _{PVCC} = V _{VCC} = 12 V I _{HS_SRC} = 2 A		1.4 ⁽²⁾		Ω
	LS; Sink	V _{VCC} = 12 V, P _{PVCC} = 5V		1	1.3	Ω
	LS; Sink	P _{PVCC} = V _{VCC} = 12 V		1	1.25	Ω
Peak output-current	HS; Source	P _{PVCC} = V _{VCC} = 12 V t _{P_HS} / Pulse < 20 ns t _{P_LS} / Pulse < 40 ns D _{HS} < 2%, D _{LS} < 4%	4			A
	HS; Sink		4			
	LS; Source		4			
	LS; Sink		4			

¹ Incremental resistance V_{BOOT}-V_{HS}=4.3V @ I_{SOURCE}=2A

² Incremental resistance V_{VCC} -V_{LS}=4.4V @ I_{SOURCE}=2A

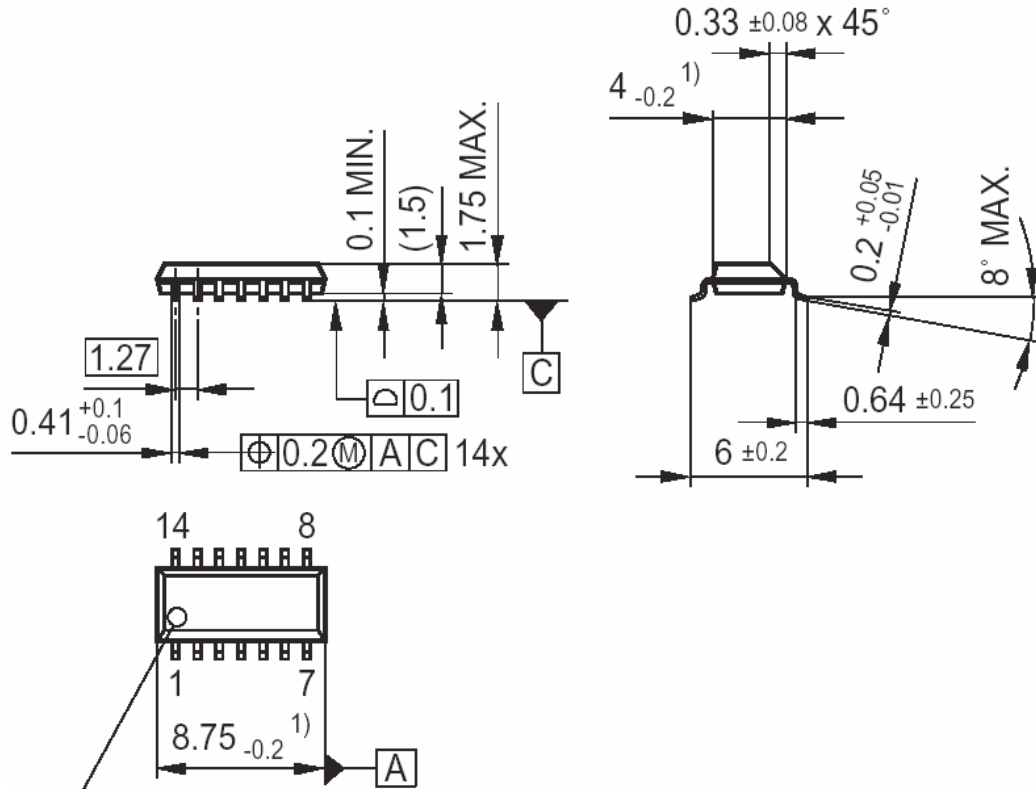


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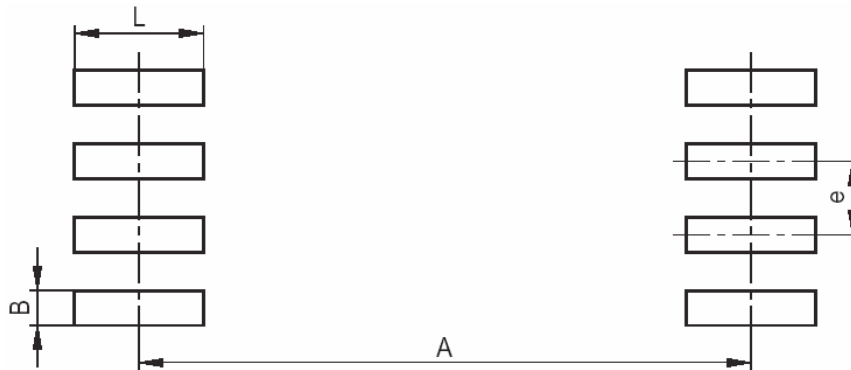
Package Drawing P-DSO-14-3



Index Marking

¹⁾ Does not include plastic or metal protrusion of 0.15 max. per side

Layout Footprints



e	A	L	B
1,27 mm	5,69 mm	1,31 mm	0,65 mm



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Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München
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