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RF3396

GENERAL PURPOSE AMPLIFIER

RoHS Compliant & Pb-Free Product
Package Style: QFN, 12-Pin, 3 x 3

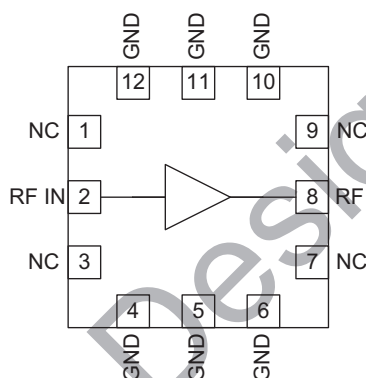


Features

- DC to >6000MHz Operation
- Internally Matched Input and Output
- 22dB Small Signal Gain
- +2.0dB Noise Figure
- +11.5dBm Output P1dB
- Footprint Compatible with Micro-X

Applications

- Basestation Applications
- Broadband, Low-Noise Gain Blocks
- IF or RF Buffer Amplifiers
- Driver Stage for Power Amplifiers
- Final PA for Low-Power Applications
- High Reliability Applications



Functional Block Diagram

Product Description

The RF3396 is a general purpose, low-cost RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as an easily-cascadable 50Ω gain block. Applications include IF and RF amplification in wireless voice and data communication products operating in frequency bands up to 6000MHz. The device is self-contained with 50Ω input and output impedances and requires only two external DC-biasing elements to operate as specified. The device is designed for cost effective high reliability in a plastic package. The 3mmx3mm footprint is compatible with standard ceramic and plastic Micro-X packages.

Ordering Information

| | |
|----------------|----------------------------------|
| RF3396 | General Purpose Amplifier |
| RF3396PCBA-41X | Fully Assembled Evaluation Board |

Optimum Technology Matching® Applied

- | | | | |
|--|--------------------------------------|-------------------------------------|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | |

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RF3396

Absolute Maximum Ratings

| Parameter | Rating | Unit |
|-------------------------------|-------------|------|
| Input RF Power | +3 | dBm |
| Operating Ambient Temperature | -40 to +85 | °C |
| Storage Temperature | -60 to +150 | °C |
| I _{CC} | 40 | mA |



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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| Parameter | Specification | | | Unit | Condition |
|---|---------------|-------------|------|-------|--|
| | Min. | Typ. | Max. | | |
| Overall | | | | | T=25 °C, I _{CC} =35mA (See Note 1.) |
| Frequency Range | | DC to >6000 | | MHz | |
| 3dB Bandwidth | | 2 | | GHz | |
| Gain | 21.0 | 22.7 | | dB | Freq=500MHz |
| | 20.2 | 22.2 | 24.2 | dB | Freq=850MHz |
| | 17.8 | 19.8 | 21.8 | dB | Freq=2000MHz |
| | | 17.4 | | dB | Freq=3000MHz |
| | | 16.0 | | | Freq=4000MHz |
| | | 12.9 | | | Freq=6000MHz |
| Noise Figure | | 2.0 | | dB | Freq=2000MHz |
| Input VSWR | | <1.9:1 | | | In a 50Ω system, DC to 6000MHz |
| Output VSWR | | <1.9:1 | | | In a 50Ω system, DC to 3000MHz |
| | | <1.4:1 | | | In a 50Ω system, 3000MHz to 6000MHz |
| Output IP ₃ | +21.5 | +23.5 | | dBm | Freq=850MHz |
| | +22.0 | +24.0 | | dBm | Freq=2000MHz |
| Output P _{1dB} | +9.5 | +11.5 | | dBm | Freq=850MHz |
| | +9.5 | +11.5 | | dBm | Freq=2000MHz |
| Reverse Isolation | | 22.5 | | dB | Freq=2000MHz |
| Thermal | | | | | I _{CC} =35mA, P _{DISS} =110mW. (See Note 3.) |
| Theta _{JC} | | 335 | | °C/W | |
| Maximum Measured Junction Temperature at DC Bias Conditions | | 122 | | °C | T _{AMB} =+85 °C |
| Mean Time To Failures | | 17,635 | | years | T _{AMB} =+85 °C |
| Power Supply | | | | | With 22Ω bias resistor |
| Device Operating Voltage | 3.3 | 3.4 | 3.5 | V | At pin 8 with I _{CC} =35mA |
| | 3.9 | 4.2 | 4.5 | v | At evaluation board connector, I _{CC} =35mA |
| Operating Current | | 35 | 40 | mA | See Note 2. |

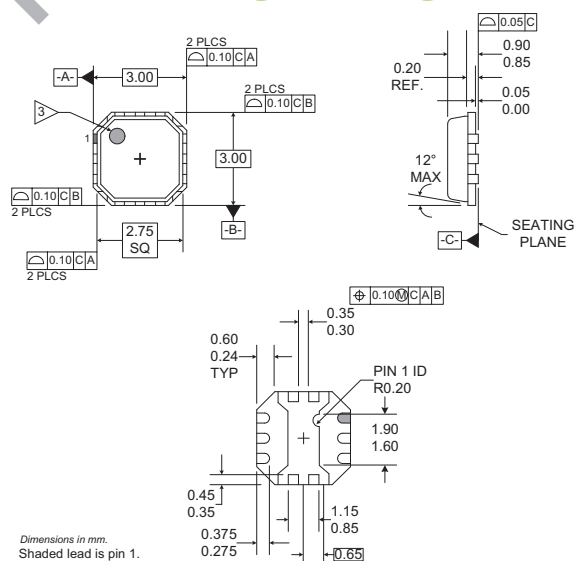
Note 1: All specification and characterization data has been gathered on standard FR-4 evaluation boards. These evaluation boards are not optimized for frequencies above 2.5GHz. Performance above 2.5GHz may improve if a high performance PCB is used.

Note 2: The RF3396 must be operated at or below 40mA in order to achieve the thermal performance listed above. While the RF3396 may be operated at higher bias currents, 35mA is the recommended bias to ensure the highest possible reliability and electrical performance.

Note 3: Because of process variations from part to part, the current resulting from a fixed bias voltage will vary. As a result, caution should be used in designing fixed voltage bias circuits to ensure the worst case bias current does not exceed 40mA over all intended operating conditions.

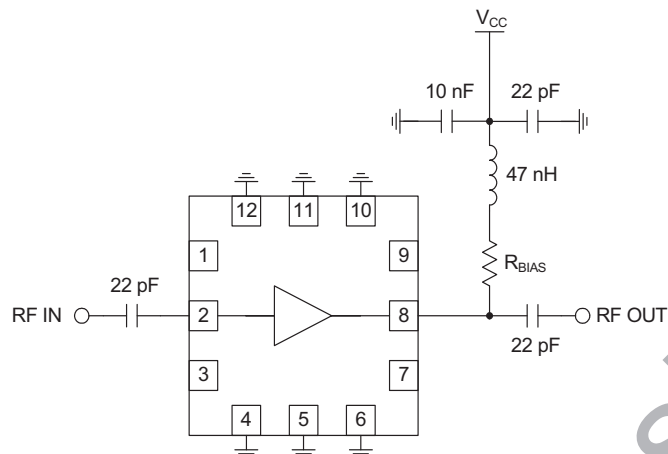
| Pin | Function | Description | Interface Schematic |
|----------|----------|---|---------------------|
| 1 | NC | No internal connections. It is not necessary to ground this pin. | |
| 2 | RF IN | RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability. | |
| 3 | NC | No internal connections. It is not necessary to ground this pin. | |
| 4 | GND | Ground connection. | |
| 5 | GND | Ground connection. | |
| 6 | GND | Ground connection. | |
| 7 | NC | No internal connections. It is not necessary to ground this pin. | |
| 8 | RF OUT | <p>RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation:</p> $R = \frac{(V_{SUPPLY} - V_{DEVICE})}{I_{CC}}$ <p>Care should also be taken in the resistor selection to ensure that the current into the part never exceeds 40mA over the planned operating temperature. This means that a resistor between the supply and this pin is always required, even if a supply near 3.4V is available, to provide DC feedback to prevent thermal runaway. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.</p> | |
| 9 | NC | No internal connections. It is not necessary to ground this pin. | |
| 10 | GND | Ground connection. | |
| 11 | GND | Ground connection. | |
| 12 | GND | Ground connection. | |
| Die Flag | GND | Ground connection. To ensure best performance, avoid placing ground vias directly beneath the part. | |

Package Drawing



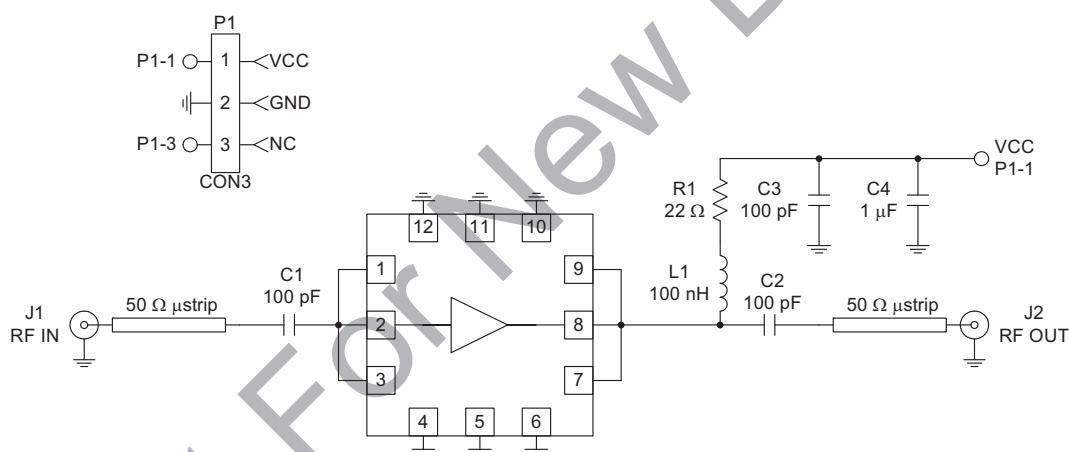
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Application Schematic



Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



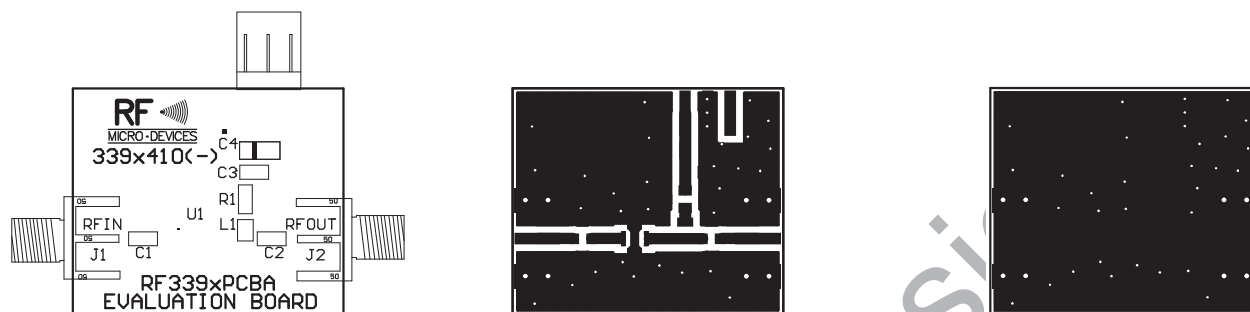
NOTE:

Evaluation board optimized for frequencies above 300 MHz and below 2.5 GHz.
For operation below 300 MHz the value of inductor L1 and capacitors C1 and C2 should be increased.

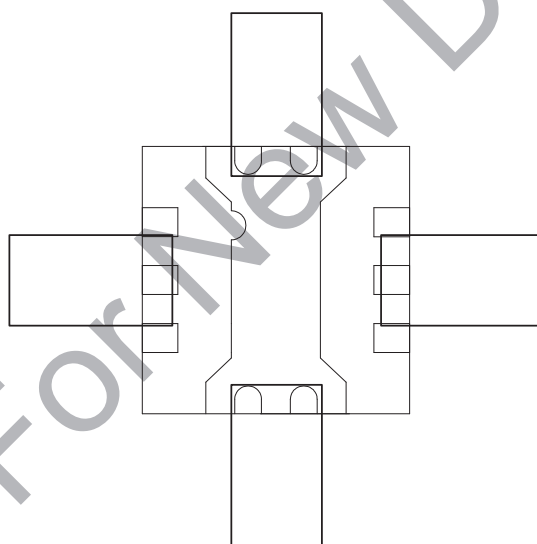
Evaluation Board Layout Board Size 1.195" x 1.000"

Board Thickness 0.033", Board Material FR-4

Note: A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.



Overlay of Suggested Micro-X and 3mmx3mm Layouts Showing Compatibility



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is Electroless Nickel, immersion Gold. Typical thickness is 3µinch to 8µinch Gold over 180µinch Nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Mask Pattern

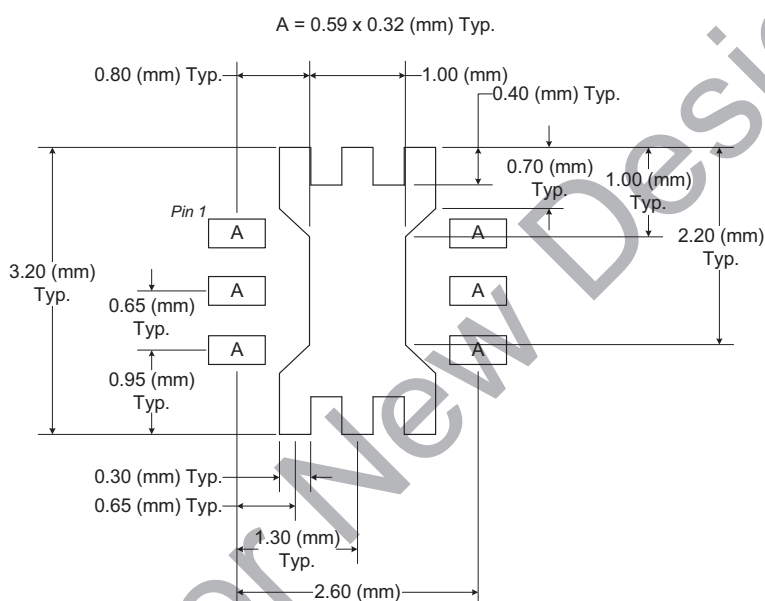
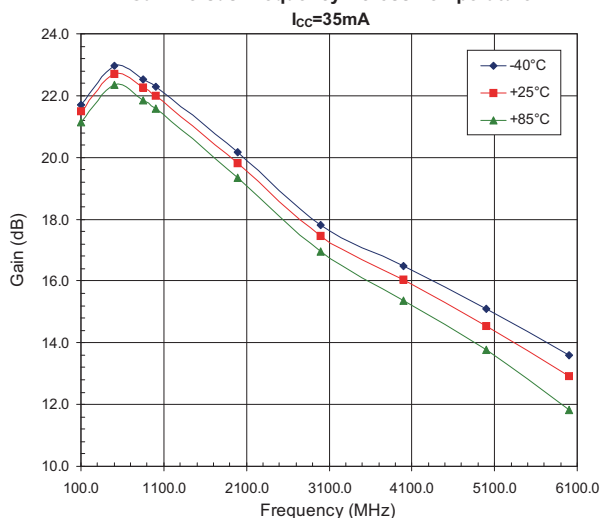
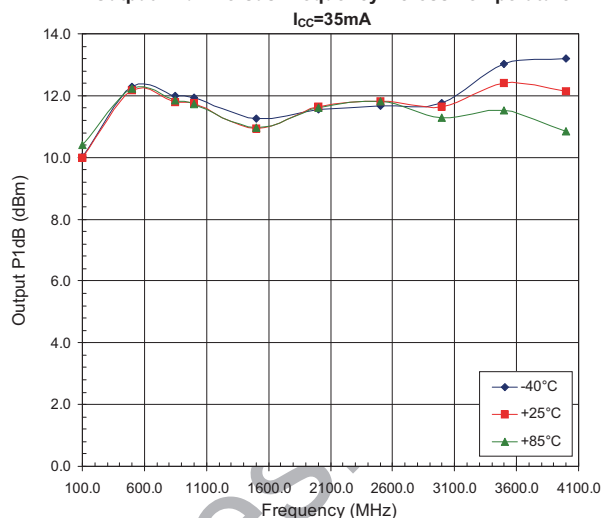


Figure 1. PCB Metal Land Pattern (Top View)

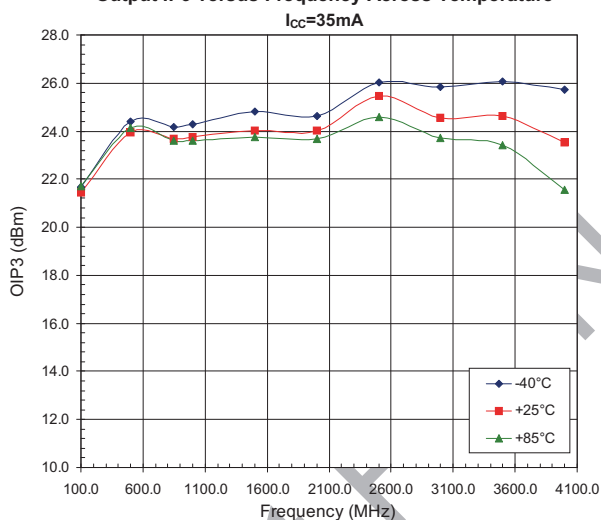
Gain versus Frequency Across Temperature



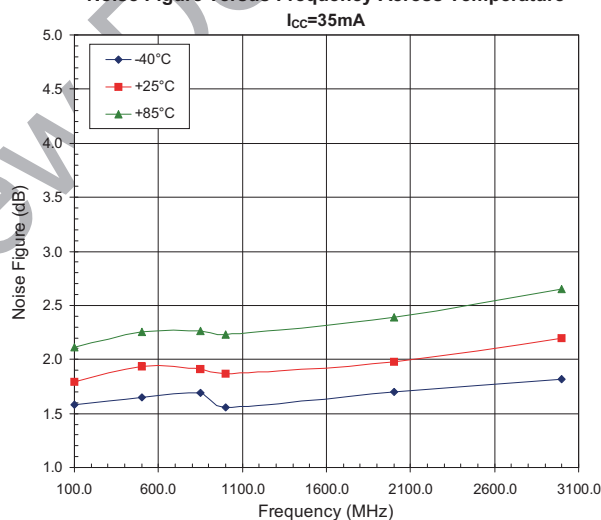
Output P1dB versus Frequency Across Temperature



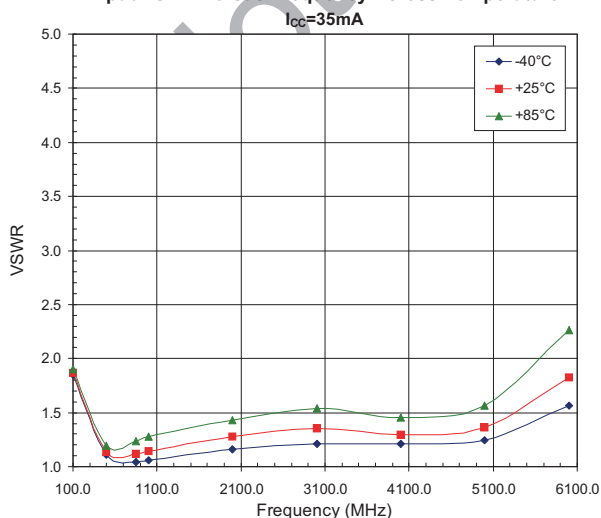
Output IP3 versus Frequency Across Temperature



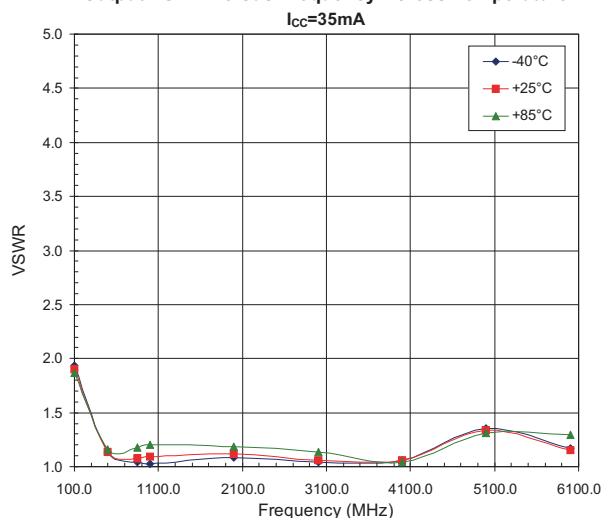
Noise Figure versus Frequency Across Temperature



Input VSWR versus Frequency Across Temperature

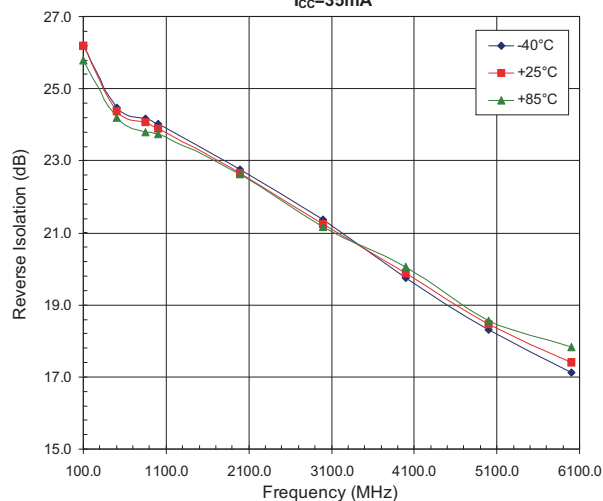


Output VSWR versus Frequency Across Temperature

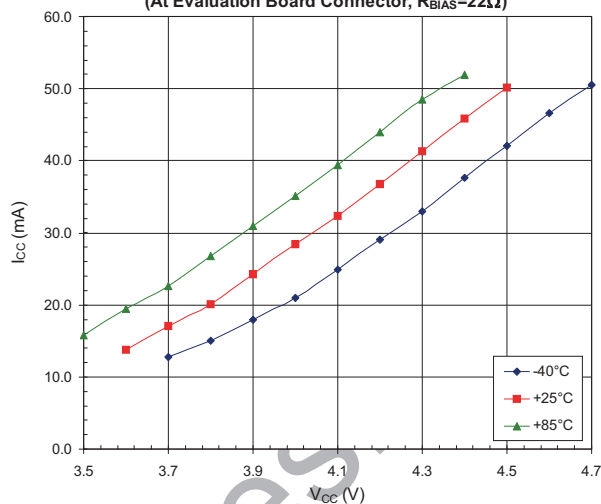


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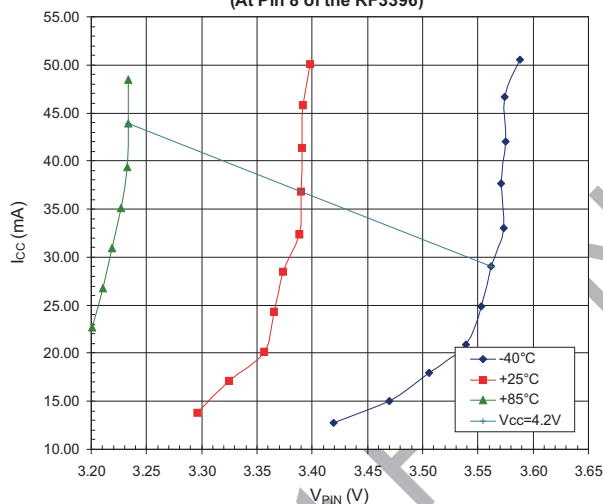
Reverse Isolation versus Frequency Across Temperature
 $I_{CC}=35\text{mA}$



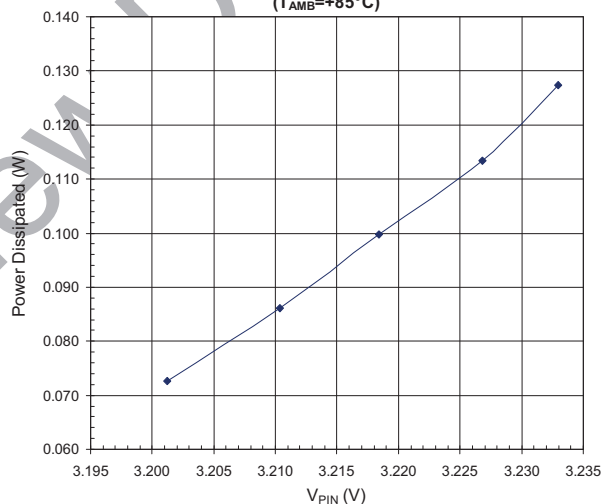
Current versus Voltage
(At Evaluation Board Connector, $R_{BIAS}=22\Omega$)



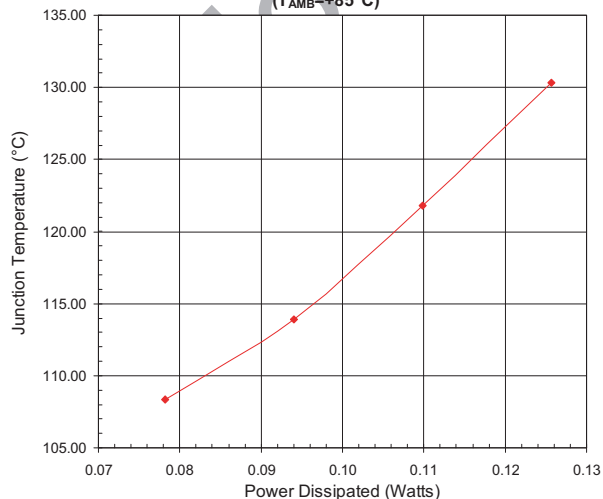
Current versus Voltage
(At Pin 8 of the RF3396)



Power Dissipated versus Voltage at Pin 8
($T_{AMB}=+85^{\circ}\text{C}$)



Junction Temperature versus Power Dissipated
($T_{AMB}=+85^{\circ}\text{C}$)



PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

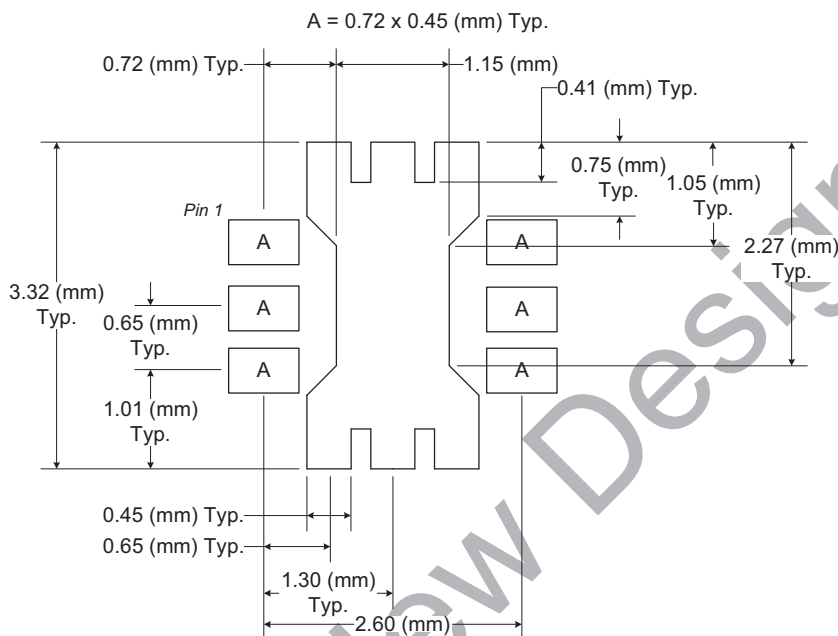


Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

NOTE: A small amount of ground inductance is required to achieve data sheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.

RF3396



Not For New Design