

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)  
[NTLJD4116NT1G](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

# NTLJD4116N

## Power MOSFET

30 V, 4.6 A,  $\mu$ Cool™ Dual N-Channel, 2x2 mm WDFN Package

### Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest  $R_{DS(on)}$  Solution in 2x2 mm Package
- 1.5 V  $R_{DS(on)}$  Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

### Applications

- DC-DC Converters (Buck and Boost Circuits)
- Low Side Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Level Shift for High Side Load Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	3.7	A
		$T_A = 85^\circ\text{C}$		2.7	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$		4.6	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.5	W
		$t \leq 5$ s		2.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	2.5	A
		$T_A = 85^\circ\text{C}$		1.8	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$	0.71	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	20	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 2)		$I_S$	2.0	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

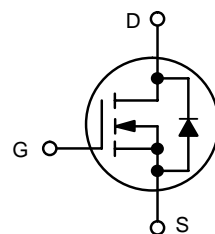
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm<sup>2</sup>, 2 oz Cu.



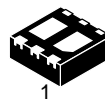
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX (Note 1)
30 V	70 m $\Omega$ @ 4.5 V	4.6 A
	90 m $\Omega$ @ 2.5 V	
	125 m $\Omega$ @ 1.8 V	
	250 m $\Omega$ @ 1.5 V	

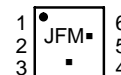


N-CHANNEL MOSFET



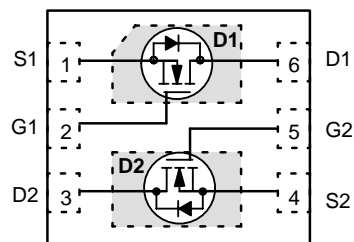
WDFN6  
CASE 506AN

### MARKING DIAGRAM



JF = Specific Device Code  
 M = Date Code  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NTLJD4116NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## NTLJD4116N

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
<b>SINGLE OPERATION (SELF-HEATED)</b>			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	
<b>DUAL OPERATION (EQUALLY HEATED)</b>			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm<sup>2</sup>, 2 oz Cu).

## NTLJD4116N

### MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , Ref to $25^\circ\text{C}$		18.1		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1.0	$\mu\text{A}$
					10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.8		mV/ $^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5, I_D = 2.0\text{ A}$		47	70	m $\Omega$
		$V_{GS} = 2.5, I_D = 2.0\text{ A}$		56	90	
		$V_{GS} = 1.8, I_D = 1.8\text{ A}$		88	125	
		$V_{GS} = 1.5, I_D = 1.5\text{ A}$		133	250	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5.0\text{ V}, I_D = 2.0\text{ A}$		4.5		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		427		pF
Output Capacitance	$C_{OSS}$			51		
Reverse Transfer Capacitance	$C_{RSS}$			32		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 2.0\text{ A}$		5.4	6.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.5		
Gate-to-Source Charge	$Q_{GS}$			0.8		
Gate-to-Drain Charge	$Q_{GD}$			1.24		
Gate Resistance	$R_G$			0.37		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 2.0\text{ A}, R_G = 2.0\ \Omega$		4.8		ns
Rise Time	$t_r$			11.8		
Turn-Off Delay Time	$t_{d(OFF)}$			14.2		
Fall Time	$t_f$			1.7		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$	0.78	1.2	V
			$T_J = 125^\circ\text{C}$	0.62		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, d_{ISD}/d_t = 100\text{ A}/\mu\text{s}, I_S = 2.0\text{ A}$		10.5		ns
Charge Time	$t_a$			7.6		
Discharge Time	$t_b$			2.9		
Reverse Recovery Time	$Q_{RR}$			5.0		

5. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

### NTLJD4116N

#### TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

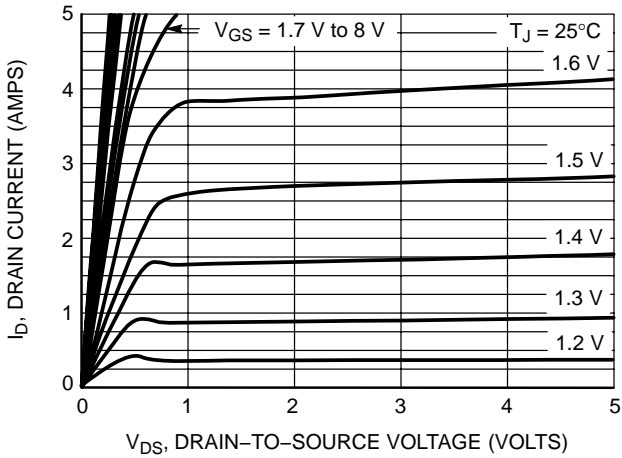


Figure 1. On-Region Characteristics

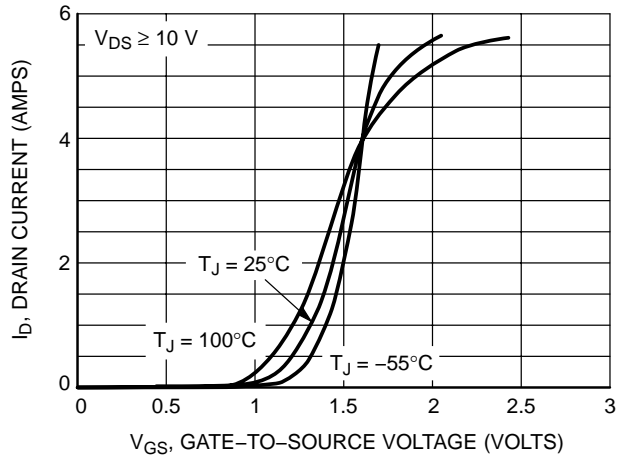


Figure 2. Transfer Characteristics

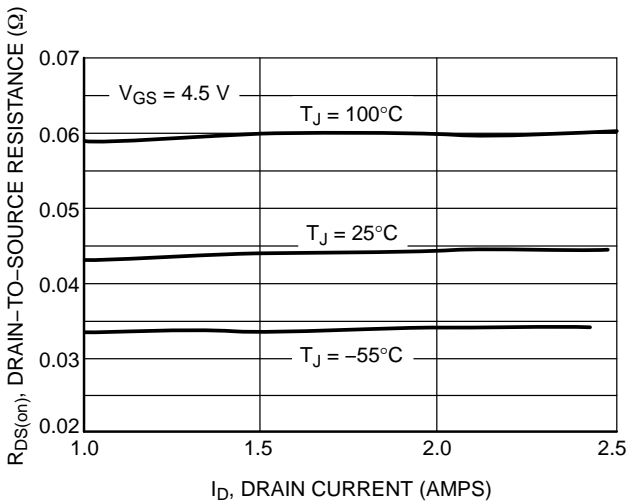


Figure 3. On-Resistance versus Drain Current

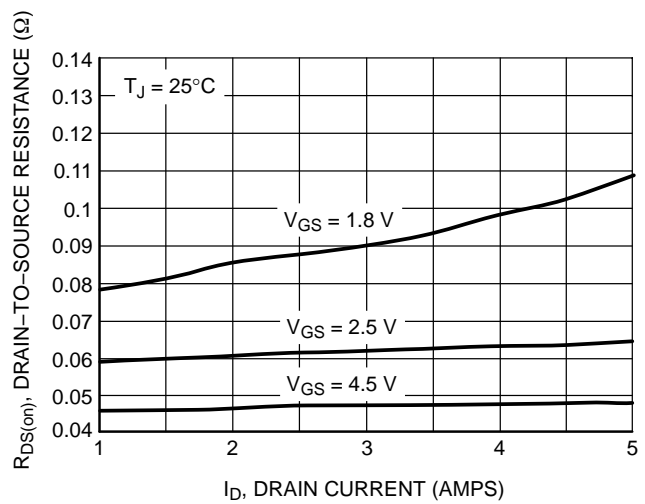


Figure 4. On-Resistance versus Drain Current and Gate Voltage

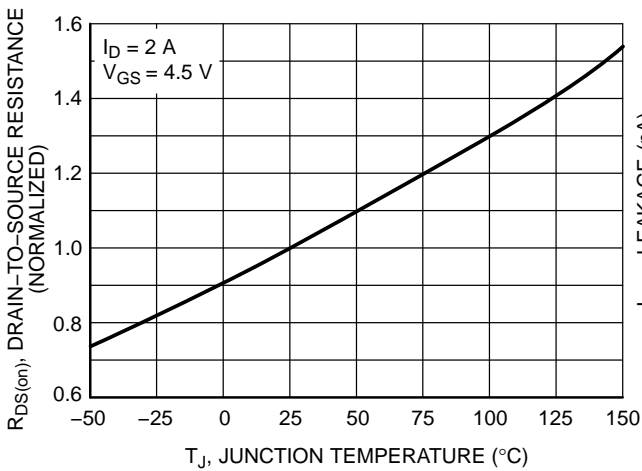


Figure 5. On-Resistance Variation with Temperature

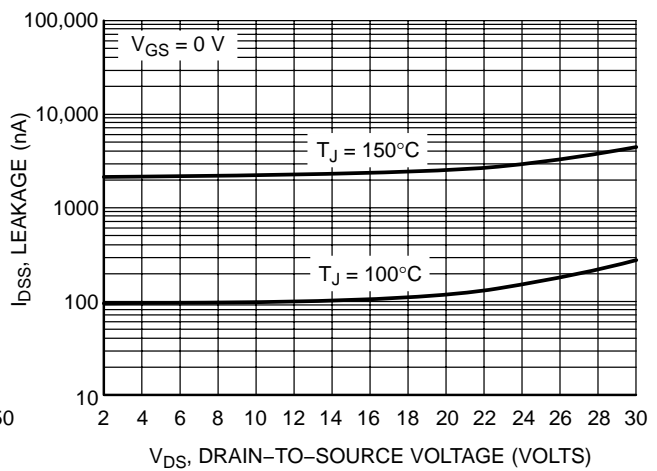
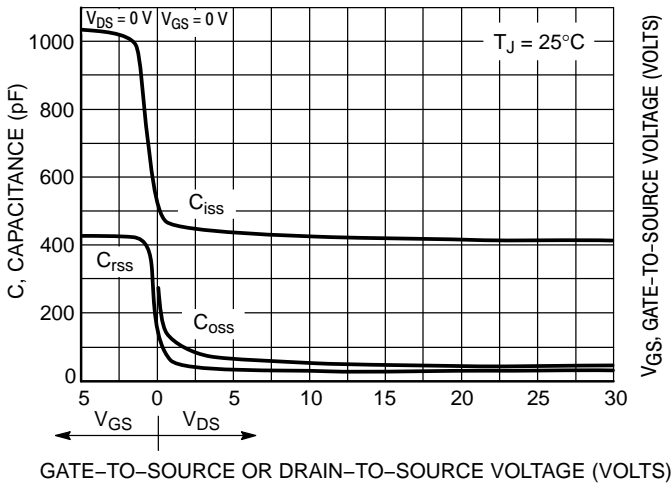


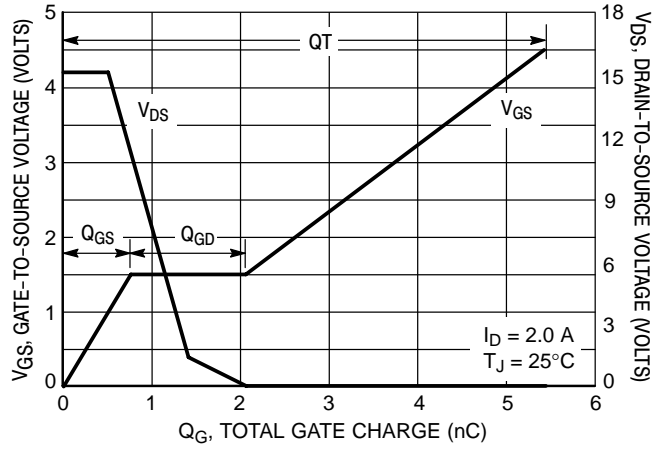
Figure 6. Drain-to-Source Leakage Current versus Voltage

**NTLJD4116N**

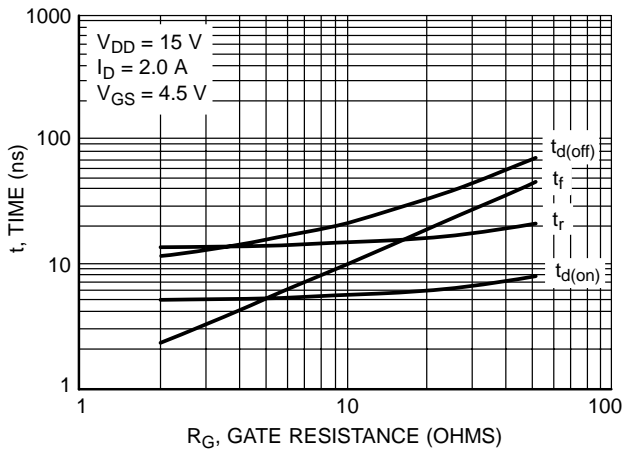
**TYPICAL PERFORMANCE CURVES** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)



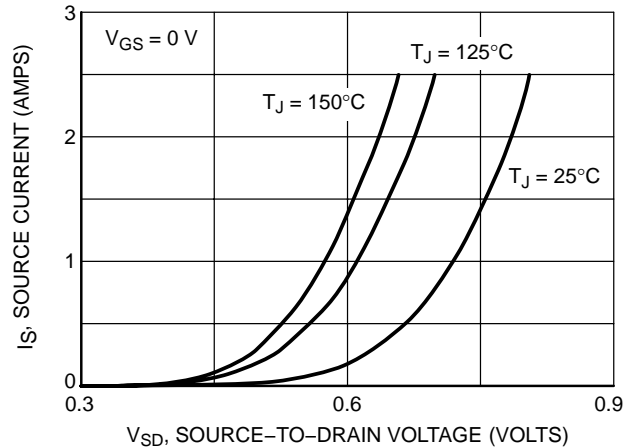
**Figure 7. Capacitance Variation**



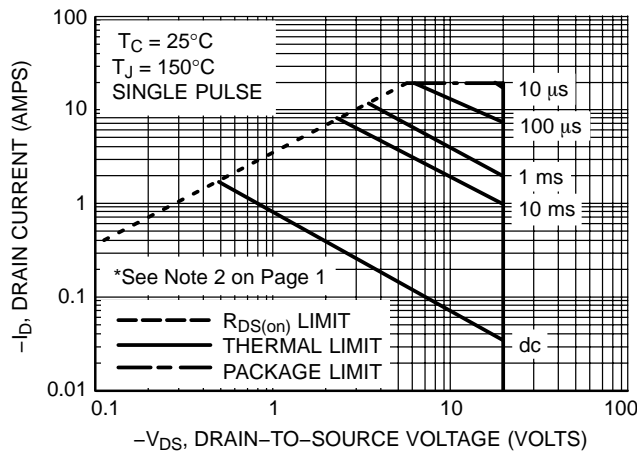
**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



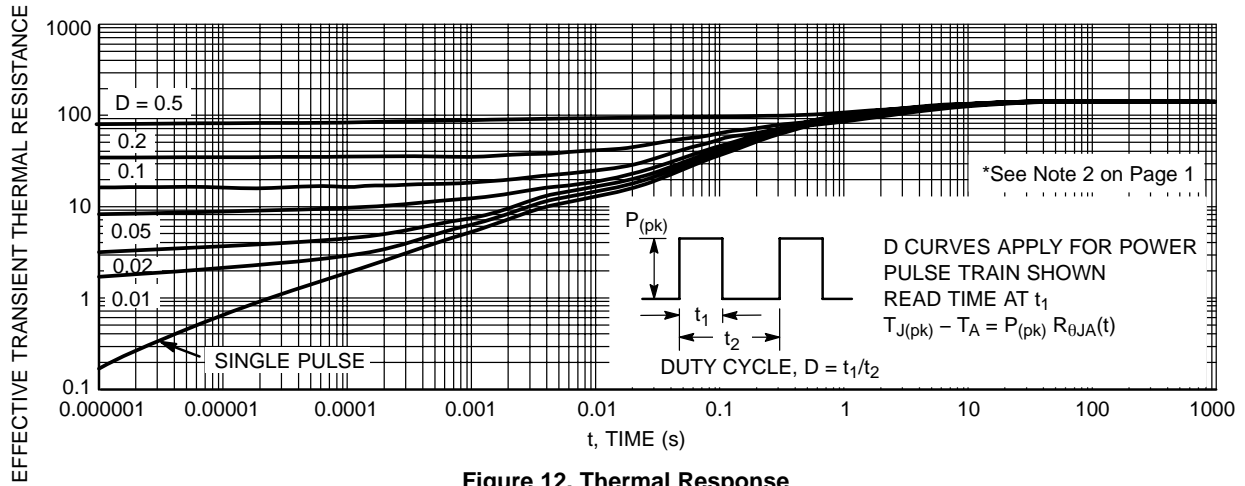
**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

**NTLJD4116N**

**TYPICAL PERFORMANCE CURVES** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

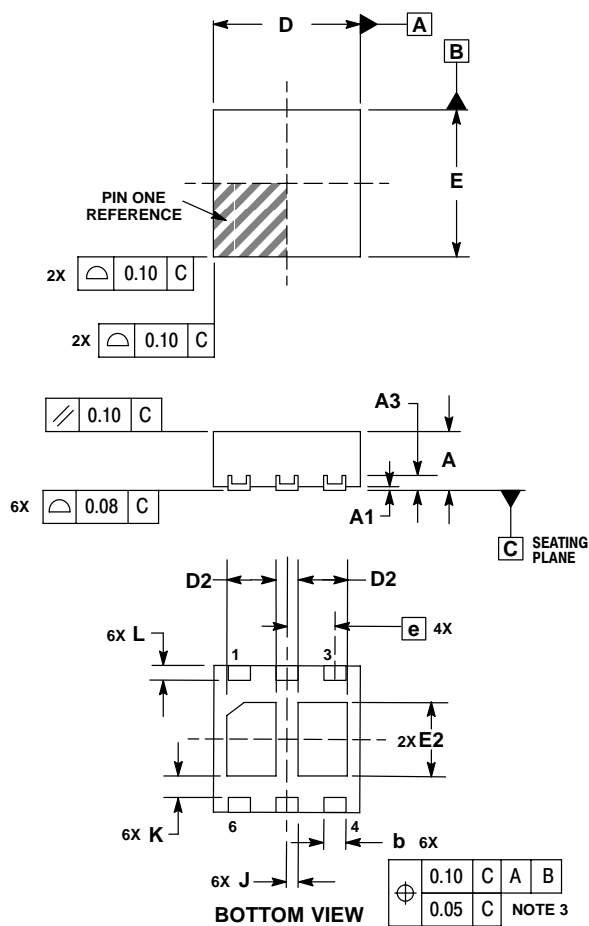


**Figure 12. Thermal Response**

### NTLJD4116N

#### PACKAGE DIMENSIONS

WDFN6, 2x2  
CASE 506AN-01  
ISSUE B

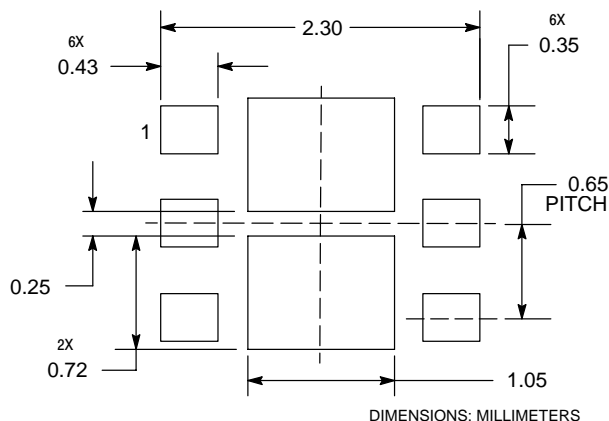


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

#### SOLDERMASK DEFINED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

µCool is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.