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Fairchild Semiconductor DM9368N

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Datasheet of DM9368N - IC DECODER/DRVR/LATCH 7SEG 16DIP

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October 1988 Revised March 2000

DM9368

7-Segment Decoder/Driver/Latch with Constant Current Source Outputs

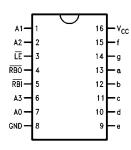
General Description

The DM9368 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

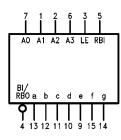
Ordering Code:

Order Number Packag		Package Number	Package Description
	DM9638N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Name	Description					
A0-A3	Address (Data) Inputs					
RBO	Ripple Blanking Output (Active LOW)					
RBI	Ripple Blanking Input (Active LOW)					
a–g	Segment Drivers-Outputs					
LE	Latch Enable Input (Active LOW)					

V_{CC} = Pin 16 GND = PIN 8

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Truth Table

1				0.15							0117	DUT				
ı				INP	UTS						001	PUT:	S			
	BINARY STATE	ΙĒ	RBI	A 3	A 2	A 1	Α0	a	b	С	d	е	f	g	RBO	DISPLAY
	_	Н	*	Х	Х	Х	Х	-		 s	TABL	.E —		-	Н	STABLE
ı	0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
1	0	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	L	H	0
	1	L	Х	L	L	L	Н	L	Н	Н	L	L	L	L	Н	1
	2	L	Х	L	L	Н	L	Н	Н	L	Н	Н	L	Н	н	2
ı	2 3	L	х	L	L	Н	Н	н	Н	Н	Н	L	L	Н	Н	3
ı		L	X	L	Н	L	L	L	Н	Н	L	Ĺ	Н	Н	H	8
	4 5	Ĺ	X	Ĺ	Н	Ĺ	H	H	L	Н	H	Ĺ	Н	Н	H	2335
Į	6	L	x	L	Н	Н	L	lμ	L	Н	Н	Н	Н	Н	Н	S
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ı	10	lī	x	;;	ī	H	ï	l іі	H	Н	Ĺ	H	н	Н	;;	8 3 8 8
ı		-	''		-		-	''							''	
ı	11	L	X	Н	L	Н	Н	L	L	Н	Н	Н	Н	Н	H	8 E E
ı	12	L	Х	H	Н	L	L	Н	L	L	Н	Н	Н	L	H	Ĺ
ı	13	L	Х	Н	Н	L	Н	L	Н	Н	Н	Н	L	Н	Н	ď
ı	14	L	X	Н	Н	Н	L	Н	L	L	Н	Н	Н	Н	H	ε
Į	15	L	Х	Н	Н	Н	Н	Н	L	L	L	Н	Н	Н	H	F
	Х	Χ	χ	Х	Χ	χ	Х	L	L	L	L	L	L	L	L**	BLANK

^{*}The RBI will blank the display only if a binary zero is stored in the latches.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial



Functional Description

The DM9368 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays. The DM9368 drives any common cathode LED display rated at a nominal 20 mA at 1.7V per segment without need for current limiting resistors.

This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" thru "9" and alpha codes "A" through "F" using upper and lower case fonts.

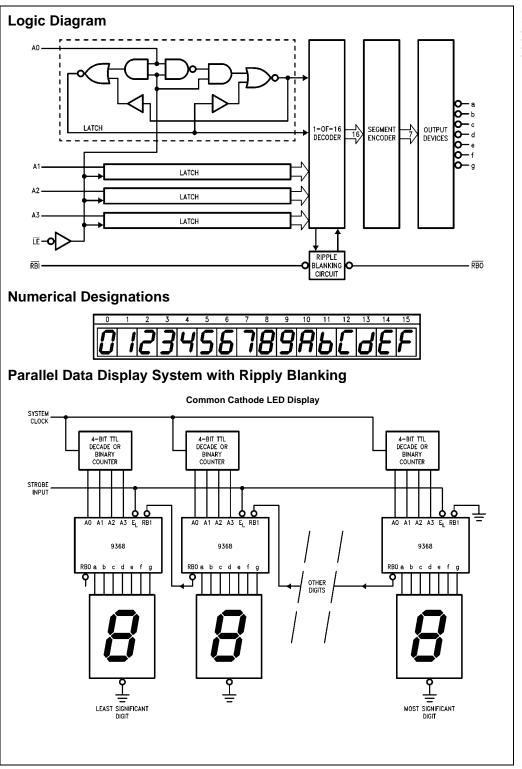
Latches on the four data inputs are controlled by an active LOW latch enable $L\overline{E}$. When the $\overline{L}\overline{E}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{L}\overline{E}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $L\overline{E}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the DM9368 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

Another feature of the DM9368 is that the unit loading on the data inputs is very low (–100 μ A Max) when the latch enable is HIGH. This allows DM9368s to be driven from an

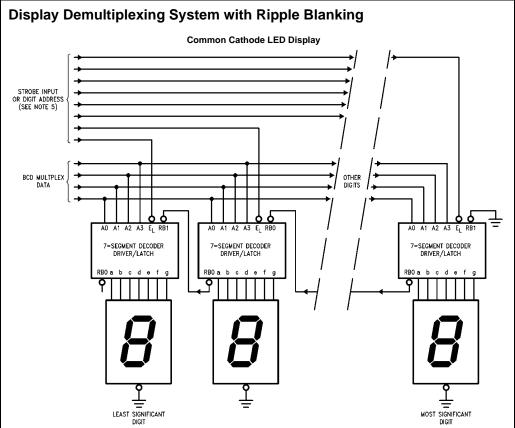
MOS device in multiplex mode without the need for drivers on the data lines.

The DM9368 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output (RBO) of a decoder to the Ripple Blanking Input (RBI) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The RBO terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

^{*}The RBO used as an input overrides all other input conditions







Note: Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.



Absolute Maximum Ratings(Note 1)

Storage Temperature Range

Supply Voltage Input Voltage Operating Free Air Temperature Range -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which 7V the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current		-80		μΑ
I _{OL}	LOW Level Output Current RBO			3.2	mA
T _A	Free Air Operating Temperature	0		70	°C
t _S (H)	Setup Time HIGH A _n to LE	30			ns
t _H (H)	Hold Time HIGH A _n to LE	0			ns
t _S (L)	Setup Time LOW A _n to LE	20			ns
t _H (L)	Hold Time LOW A _n to LE	0			ns
t _W (L)	LE Pulse Width LOW	45			ns
I _{OH}	Segment Output HIGH Current	-16		-22	mA
I _{OL}	Segment Output LOW Current	-250		250	μА

Electrical Characteristics

ver recommended operating free air temperature range (unless otherwise poted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -12 \text{ mA}$			-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max,$ $V_{IL} = Max$	2.4	3.4		V
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max,$ $V_{IH} = Min$		0.2	0.4	V
lį	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$			1	mA
I _{IH}	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.4V$			40	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-1.6	mA
Ios	Short Circuit Output Current	V _{CC} = Max (Note 3)	-18		-57	mA
I _{CC}	Supply Current	V _{CC} = Max, Outputs OPEN, Data & Latch Inputs = 0V			67	mA

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

 $V_{CC} = 5.0V$, $T_A = 25^{\circ}C$

Symbol	Parameter	C _L = 15 pF,	Units				
Gymbol	i arameter	Min	Max	Omis			
t _{PLH}	Propagation Delay		50	50 75 ns			
t _{PHL}	A _n to a–g		75				
t _{PLH}	Propagation Delay		70	ns			
t _{PHL}	LE to a-g		90	115			

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Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.740 - 0.780}{(18.80 - 19.81)}$ 0.090 (2.286) 16 15 14 13 12 11 10 16 15 INDEX AREA $\frac{0.250 \pm 0.010}{(6.350 \pm 0.254)}$ PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 $\frac{0.065}{(1.651)}$ 0.130 ± 0.005 $\frac{0.060}{(1.524)}$ TYP 0.300 - 0.320 4° TYP (3.302 ± 0.127) OPTIONAL (7.620 - 8.128) $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 95° ± 5° $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 90° ± 4° TYP 0.280 (7.112) MIN 0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381) 0.014 = 0.023 (0.356 = 0.584) TYP $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)}$ (0.325 +0.040 -0.015 0.050 ± 0.010 N16E (REV F) (8.255 +1.016) -0.381 (1.270 ± 0.254) TYP

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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