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[Texas Instruments](#)  
[CD74HC40103QM96Q1](#)

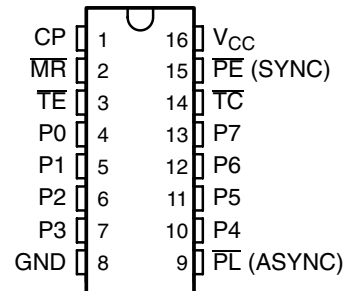
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**CD74HC40103-Q1**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**  
 SCLS547A – OCTOBER 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- $V_{CC}$  Voltage = 2 V to 6 V
- High Noise Immunity  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$ ,  $V_{CC} = 5 V$

M PACKAGE  
(TOP VIEW)



**description/ordering information**

The CD74HC40103 is manufactured with high-speed silicon-gate technology and consists of an 8-stage synchronous down counter with a single output, which is active when the internal count is zero. The device contains a single 8-bit binary counter. Each device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count ( $\overline{TC}$ ) output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock (CP) output. Counting is inhibited when the terminal enable ( $\overline{TE}$ ) input is high.  $\overline{TC}$  goes low when the count reaches zero, if  $\overline{TE}$  is low, and remains low for one full clock period.

When the synchronous preset enable ( $\overline{PE}$ ) input is low, data at the P0–P7 inputs are clocked into the counter on the next positive clock transition, regardless of the state of  $\overline{TE}$ . When the asynchronous preset enable ( $\overline{PL}$ ) input is low, data at the P0–P7 inputs asynchronously are forced into the counter, regardless of the state of the  $\overline{PE}$ ,  $\overline{TE}$ , or CP inputs. Inputs P0–P7 represent a single 8-bit binary word for the CD74HC40103. When the master reset ( $\overline{MR}$ ) input is low, the counter asynchronously is cleared to its maximum count of  $255_{10}$ , regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except  $\overline{TE}$  are high at the time of zero count, the counters jump to the maximum count, giving a counting sequence of  $100_{16}$  or  $256_{10}$  clock pulses long.

**ORDERING INFORMATION<sup>†</sup>**

$T_A$	PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC40103QM96Q1	HC40103Q

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**description/ordering information (continued)**

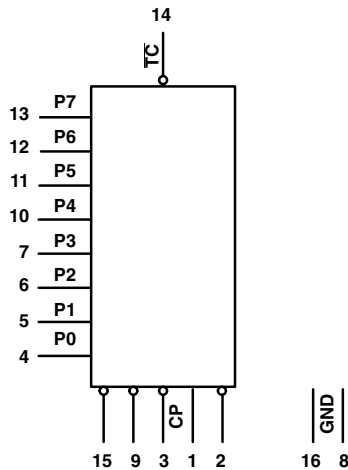
The CD74HC40103 may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either synchronous or ripple mode. These circuits have the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits and can drive up to ten LSTTL loads.

**FUNCTION TABLE**

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	$\overline{TE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	X		Preset on next positive clock transition
H	L	X	X	Asynchronous	Preset asynchronously
L	X	X	X		Clear to maximum count

NOTE: H = high voltage level, L = low voltage level, X = don't care  
 Clock connected to clock input  
 Synchronous operation: changes occur on negative-to-positive clock transitions.  
 Load inputs: MSB = P7, LSB = P0

**logic diagram (positive logic)**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Source or sink current per output pin, $I_O$ ( $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	73°C/W
Maximum junction temperature, $T_J$	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	300°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	6	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V	
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V	
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 6$ V	1.8		
$V_I$	Input voltage	0	$V_{CC}$	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
$T_A$	Operating free-air temperature	–40	125	°C	

NOTES: 3. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
				MIN	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9		1.9	V
			-0.02	4.5 V	4.4		4.4	
			-0.02	6 V	5.9		5.9	
		TTL loads	-4	4.5 V	3.98		3.7	
			-5.2	6 V	5.48		5.2	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V	0.1		0.1	V
			0.02	4.5 V	0.1		0.1	
			0.02	6 V	0.1		0.1	
		TTL loads	4	4.5 V	0.26		0.4	
			5.2	6 V	0.26		0.4	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		6 V	±0.1		±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0	6 V	8		160	μA	
C <sub>IN</sub>	C <sub>L</sub> = 50 pF			10		10	pF	

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t <sub>w</sub>	Pulse duration	CP	2 V	165	250	ns	
			4.5 V	33	50		
			6 V	28	43		
	P <sub>L</sub>	2 V	125	190			
		4.5 V	25	38			
		6 V	21	32			
	M <sub>R</sub>	2 V	125	190			
		4.5 V	25	38			
		6 V	21	32			
f <sub>max</sub>	CP frequency (see Note 4)	2 V	3	2	MHz		
		4.5 V	15	10			
		6 V	18	12			
t <sub>su</sub>	P to CP	2 V	100	150	ns		
		4.5 V	20	30			
		6 V	17	26			
	P <sub>E</sub> to CP	2 V	75	110			
		4.5 V	15	22			
		6 V	13	19			
	T <sub>E</sub> to CP	2 V	150	225			
		4.5 V	30	45			
		6 V	26	38			
	To CP, M <sub>R</sub> inactive	2 V	50	75			
		4.5 V	10	15			
		6 V	9	13			
t <sub>h</sub>	P to CP	2 V	5	5	ns		
		4.5 V	5	5			
		6 V	5	5			
	T <sub>E</sub> to CP	2 V	0	0			
		4.5 V	0	0			
		6 V	0	0			
	P <sub>E</sub> to CP	2 V	2	2			
		4.5 V	2	2			
		6 V	2	2			

NOTE 4: Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables (P<sub>E</sub> or T<sub>E</sub>) to clock setup times, and count enables (P<sub>E</sub> or T<sub>E</sub>) to clock hold times determine maximum clock frequency. For example, with these HC devices:

$$CP f_{max} = \frac{1}{CP \text{ to } \overline{TC} \text{ prop delay} + \overline{TE} \text{ to CP setup time} + \overline{TE} \text{ to CP hold time}} = \frac{1}{60 + 30 + 0} \approx 11 \text{ MHz}$$

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t <sub>pd</sub>	CP	TC̄ (asynchronous preset)	C <sub>L</sub> = 50 pF	2 V		300		450	ns	
				4.5 V		60	90			
			6 V		51	77				
			C <sub>L</sub> = 15 pF	5 V		25				
		TC̄ (synchronous preset)	C <sub>L</sub> = 50 pF	2 V		300		450		
				4.5 V		60	90			
			6 V		51	77				
			C <sub>L</sub> = 15 pF	5 V		25				
	TĒ	TC̄	C <sub>L</sub> = 50 pF	2 V		200		300		
				4.5 V		40	60			
			6 V		34	51				
			C <sub>L</sub> = 15 pF	5 V		17				
	PL	TC̄	C <sub>L</sub> = 50 pF	2 V		275		415		
				4.5 V		55	83			
			6 V		47	71				
			C <sub>L</sub> = 15 pF	5 V		23				
	MR	TC̄	C <sub>L</sub> = 50 pF	2 V		275		415		
				4.5 V		55	83			
			6 V		47	71				
			C <sub>L</sub> = 15 pF	5 V		23				
t <sub>t</sub>			C <sub>L</sub> = 50 pF	2 V		75		110	ns	
				4.5 V		15	22			
				6 V		13	19			
f <sub>max</sub>	CP		C <sub>L</sub> = 15 pF	5 V		25		MHz		

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, input t<sub>r</sub>, t<sub>f</sub> = 6 ns

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance (see Note 5)	25	pF

NOTE 5: C<sub>pd</sub> is used to determine the dynamic power consumption per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency

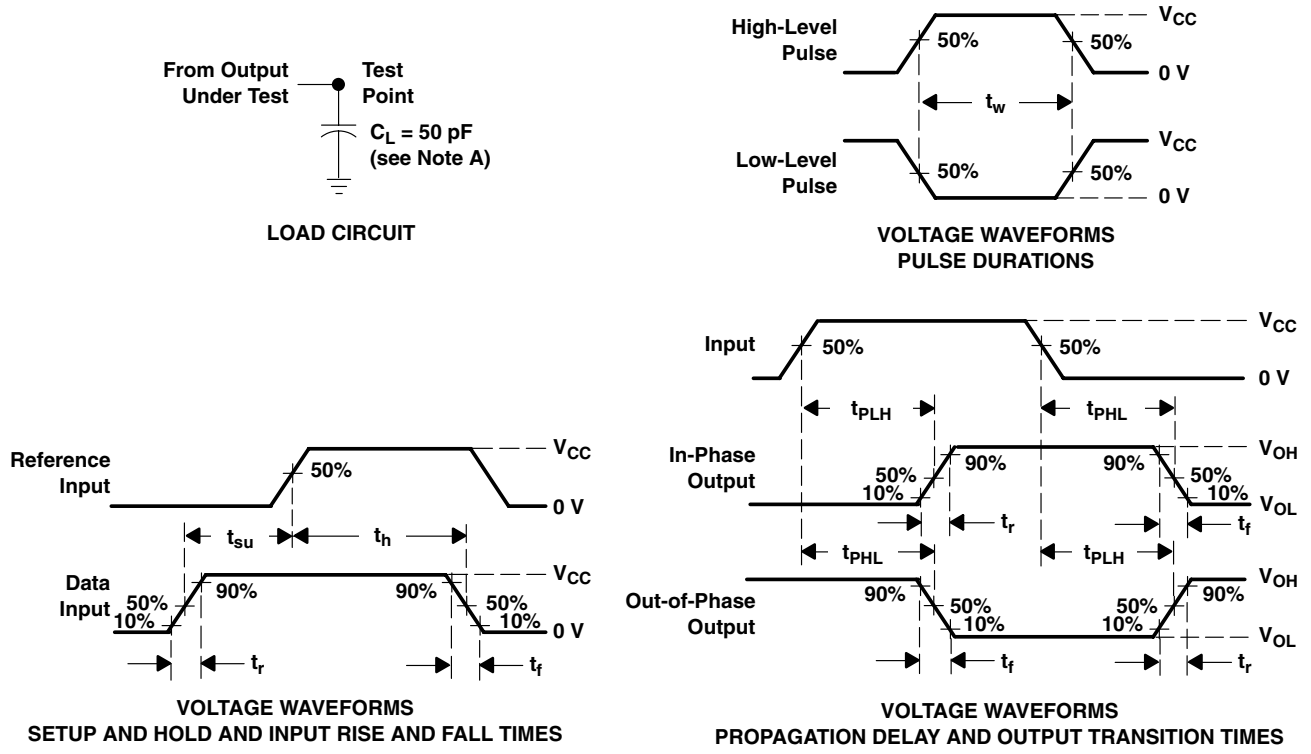
f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**



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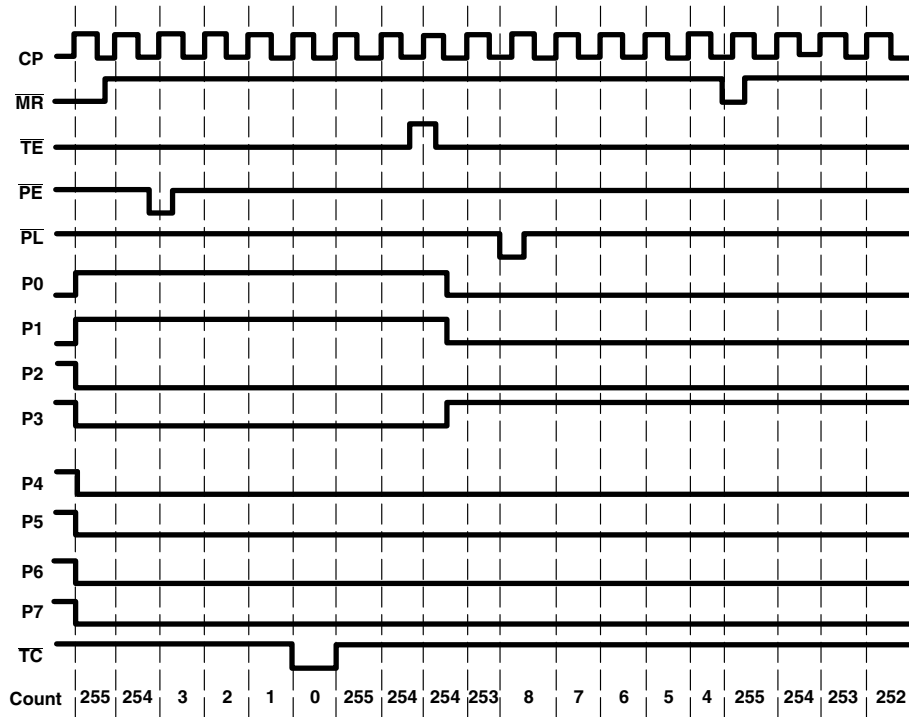


Figure 2. Timing Diagram



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC40103QM96Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Catalog: [CD74HC40103](#)
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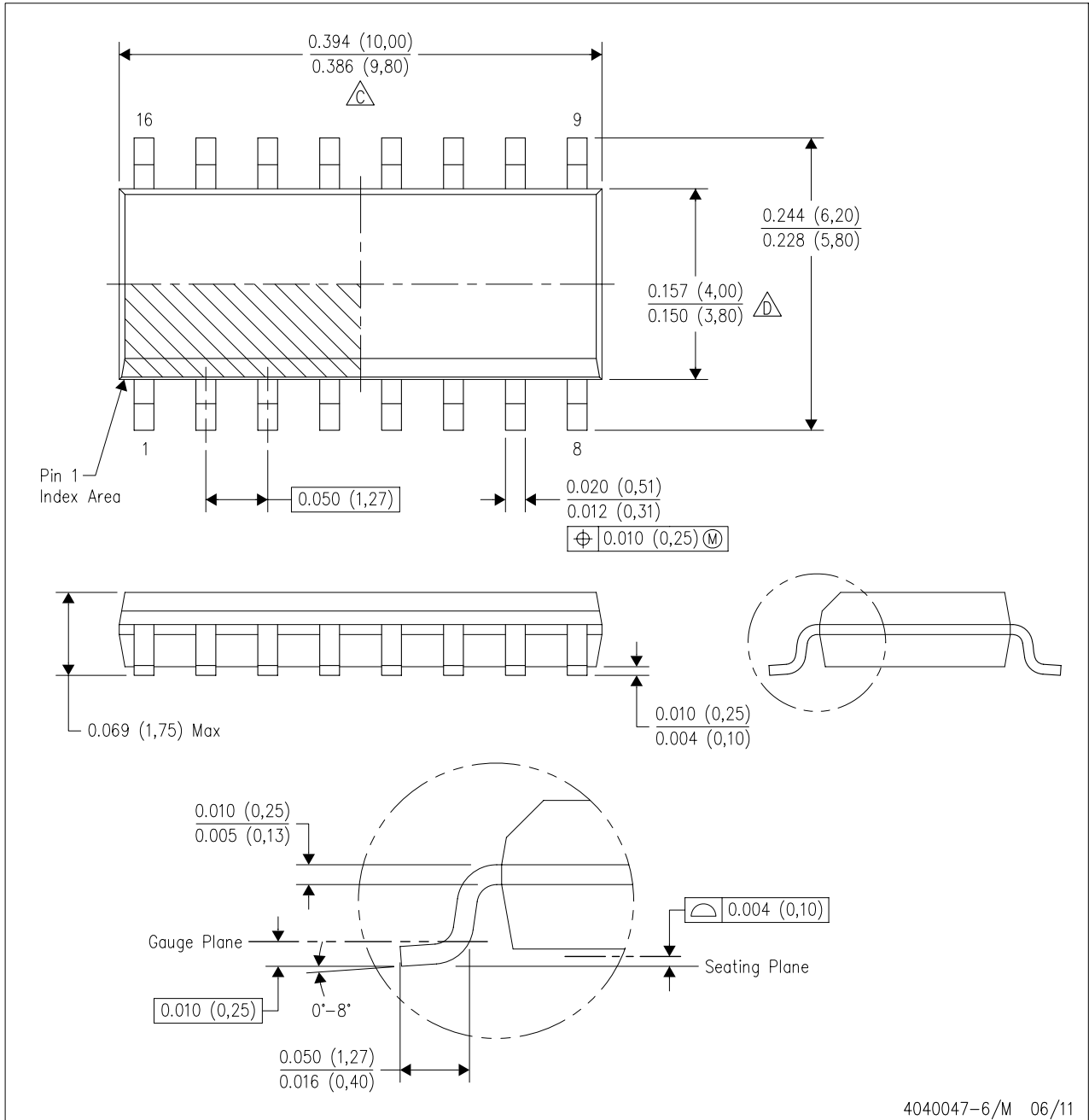
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**MECHANICAL DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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