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Maxim Integrated
MAX19586ETN+D

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19-3758; Rev 0; 8/05

EVALUATION KIT AVAILABLE

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

MAX19586

General Description

The MAX19586 is a 3.3V, high-speed, high-performance analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) and a 16-bit converter core. The MAX19586 is optimized for multichannel, multimode receivers, which require the ADC to meet very stringent dynamic performance requirements. With a -82dBFS noise floor, the MAX19586 allows for the design of receivers with superior sensitivity requirements.

At 80Msps, the MAX19586 achieves a 79.2dB signal-to-noise ratio (SNR) and an 84.3dBc/100dBc single-tone spurious-free dynamic range (SFDR) performance (SFDR1/SFDR2) at f_{IN} = 70MHz. The MAX19586 is not only optimized for excellent dynamic performance in the 2nd Nyquist region, but also for high-IF input frequencies. For instance, at 130MHz, the MAX19586 achieves an 82.5dBc SFDR and its SNR performance stays flat (within 2.5dB) throughout the 4th Nyquist region. This level of performance makes the part ideal for high-performance digital receivers.

The MAX19586 operates from a 3.3V analog supply voltage and a 1.8V digital voltage, features a 2.56V_{P-P} full-scale input range, and allows for a guaranteed sampling speed of up to 80Msps. The input track-and-hold stage operates with a 600MHz full-scale, full-power bandwidth.

The MAX19586 features parallel, low-voltage CMOS-compatible outputs in two's-complement output format.

The MAX19586 is manufactured in an 8mm x 8mm, 56-pin thin QFN package with exposed paddle (EP) for low thermal resistance, and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

Cellular Base-Station Transceiver Systems (BTS)
Wireless Local Loop (WLL)
Multicarrier Receivers
Multistandard Receivers
E911 Location Receivers
High-Performance Instrumentation
Antenna Array Processing

Features

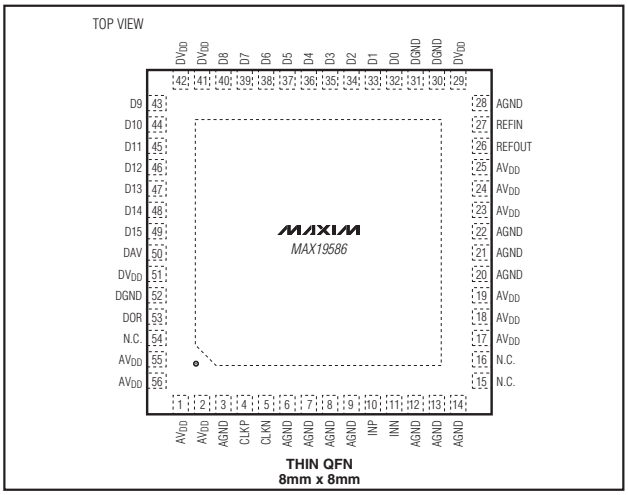
- **80Msps Minimum Sampling Rate**
- **-82dBFS Noise Floor**
- **Excellent Dynamic Performance**
  - **80dB/79.2dB SNR at f_{IN} = 10MHz/70MHz and -2dBFS**
  - **96dBc/102dBc Single-Tone SFDR1/SFDR2 at f_{IN} = 10MHz**
  - **84.3dBc/100dBc Single-Tone SFDR1/SFDR2 at f_{IN} = 70MHz**
- **Less than 0.1ps Sampling Jitter**
- **1.1W Power Dissipation**
- **2.56V_{P-P} Fully Differential Analog Input Voltage Range**
- **CMOS-Compatible Two's-Complement Data Output**
- **Separate Data Valid Clock and Over-Range Outputs**
- **Flexible Input Clock Buffer**
- **3.3V Analog Power Supply; 1.8V Digital Output Supply**
- **Small 8mm x 8mm x 0.8mm 56-Pin Thin QFN Package**
- **EV Kit Available for MAX19586 (Order MAX19586EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX19586ETN	-40°C to +85°C	56 Thin QFN-EP	T5688-2
MAX19586ETN+	-40°C to +85°C	56 Thin QFN-EP	T5688-2

+Denotes lead-free package.

Pin Configuration



High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND ..... -0.3V to +3.6V
DV_{DD} to DGND..... -0.3V to +2.4V
AGND to DGND..... -0.3V to +0.3V
INP, INN, CLKP, CLKN, REFP, REFN,
REFIN, REFOUT to AGND.....-0.3V to (AV_{DD} + 0.3V)
D0–D15, DAV, DOR, DAV to GND.....-0.3V to (DV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN
(derate 47.6mW/°C above +70°C).....3809.5mW

Operating Temperature Range .....-40°C to +85°C
Thermal Resistance θ_{JA} .....21°C/W
Thermal Resistance θ_{JC} .....0.6°C/W
Junction Temperature.....+150°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, AGND = DGND = 0, INP and INN driven differentially, internal reference CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N			16		Bits
Offset Error	VOS		0	10	20	mV
Gain Error	GE		-3.5		+3.5	%FS
ANALOG INPUTS (INP, INN)						
Input Voltage Range	V_{DIFF}	Fully differential input, V_{IN} = V_{INP} - V_{INN}		2.56		V_{P-P}
Common-Mode Voltage	V_{CM}	Internally self-biased		2.2		V
Differential Input Resistance	R_{IN}			10 ±20%		kΩ
Differential Input Capacitance	C_{IN}			7		pF
Full-Power Analog Bandwidth	BW_{-3dB}	-3dB rolloff for FS Input		600		MHz
REFERENCE INPUT/OUTPUT (REFIN, REFOUT)						
Reference Input Voltage Range	REFIN			1.28 ±10%		V
Reference Output Voltage	REFOUT			1.28		V
DYNAMIC SPECIFICATIONS (f_{CLK} = 80Msps)						
Thermal Plus Quantization Noise Floor	NF	A_{IN} < -35dBFS		-82		dBFS
Signal-to-Noise Ratio (First 4 Harmonics Excluded) (Notes 2, 3)	SNR	f_{IN} = 10MHz, A_{IN} = -2dBFS		80		dB
		f_{IN} = 70MHz, A_{IN} = -2dBFS	77.5	79.2		
		f_{IN} = 100MHz, A_{IN} = -2dBFS		78.5		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		77.9		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		77.2		
Signal-to-Noise Plus Distortion (Notes 2, 3)	SINAD	f_{IN} = 10MHz, A_{IN} = -2dBFS		79.6		dB
		f_{IN} = 70MHz, A_{IN} = -2dBFS	75	77.6		
		f_{IN} = 100MHz, A_{IN} = -2dBFS		77.4		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		76.4		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		72.7		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, AGND = DGND = 0, INP and INN driven differentially, internal reference CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range (Worst Harmonic, 2nd and 3rd)	SFDR1	f_{IN} = 10MHz, A_{IN} = -2dBFS		96		dBc
		f_{IN} = 70MHz, A_{IN} = -2dBFS	80	84.3		
		f_{IN} = 100MHz, A_{IN} = -2dBFS		84		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		82.5		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		78		
Spurious-Free Dynamic Range (Worst Harmonic, 4th and Higher) (Note 3)	SFDR2	f_{IN} = 10MHz, A_{IN} = -2dBFS		102		dBc
		f_{IN} = 70MHz, A_{IN} = -2dBFS	90	100		
		f_{IN} = 100MHz, A_{IN} = -2dBFS		92		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		94		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		90		
Second-Order Harmonic Distortion	HD2	f_{IN} = 10MHz, A_{IN} = -2dBFS		-100		dBc
		f_{IN} = 70MHz, A_{IN} = -2dBFS		-95	-84	
		f_{IN} = 100MHz, A_{IN} = -2dBFS		-94		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		-88.8		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		-78		
Third-Order Harmonic Distortion	HD3	f_{IN} = 10MHz, A_{IN} = -2dBFS		-96		dBc
		f_{IN} = 70MHz, A_{IN} = -2dBFS		-84.3	-80	
		f_{IN} = 100MHz, A_{IN} = -2dBFS		-84		
		f_{IN} = 130MHz, A_{IN} = -2dBFS		-82.5		
		f_{IN} = 168MHz, A_{IN} = -2dBFS		-78		
Two-Tone Intermodulation Distortion	TTIMD	f_{IN1} = 65.1MHz, A_{IN} = -8dBFS f_{IN2} = 70.1MHz, A_{IN} = -8dBFS		-85.2		dBc
Two-Tone SFDR	TTSFDR	f_{IN1} = 65.1MHz, f_{IN2} = 70.1MHz -100dBFS < A_{IN} < -10dBFS		99		dBFS
CONVERSION RATE						
Maximum Conversion Rate	f_{CLKMAX}		80			MHz
Minimum Conversion Rate	f_{CLKMIN}				20	MHz
Aperture Jitter	t_J			0.094		ps_{RMS}
CLOCK INPUTS (CLKP, CLKN)						
Differential Input Swing	$V_{DIFFCLK}$	Fully differential inputs		1.0 to 5.0		V_{P-P}
Common-Mode Voltage	V_{CMCLK}	Self-biased		1.6		V
Differential Input Resistance	R_{INCLK}			10		kΩ
Differential Input Capacitance	C_{INCLK}			3		pF
CMOS-COMPATIBLE DIGITAL OUTPUTS (D0–D15, DOR, DAV)						
Digital Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	DV_{DD} - 0.2			V
Digital Output Low Voltage	V_{OL}	I_{SINK} = 200µA			0.2	V

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, AGND = DGND = 0, INP and INN driven differentially, internal reference CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING SPECIFICATION (Figures 4, 5), C_L = 5pF (D0–D15, DOR); C_L = 15pF (DAV)						
CLKP - CLKN High	t_{CLKP}	(Note 2)	5			ns
CLKP - CLKN Low	t_{CLKN}	(Note 2)	5			ns
Effective Aperture Delay	t_{AD}			-300		ps
Output Data Delay	t_{DAT}			3.3		ns
Data Valid Delay	t_{DAV}	(Note 2)	2.8	3.8	5.0	ns
Pipeline Latency	t_P			7		Clock Cycles
CLKP Rising Edge to DATA Not Valid	t_{DNV}	(Note 2)	1.2			ns
CLKP Rising Edge to DATA Guaranteed Valid	t_{DGV}	(Note 2)			6.5	ns
DATA Setup Time Before Rising DAV	t_S	Clock duty cycle = 50% (Note 2)	3			ns
DATA Hold Time After Rising DAV	t_H	Clock duty cycle = 50% (Note 2)	3			ns
POWER SUPPLIES						
Analog Power-Supply Voltage	AV_{DD}		3.13	3.3	3.46	V
Digital Output Power-Supply Voltage	DV_{DD}		1.7	1.8	1.9	V
Analog Power-Supply Current	I_{AVDD}			320	382	mA
Digital Output Power-Supply Current	I_{DVDD}			28	35	mA
Power Dissipation	P_{DISS}			1105	1325	mW

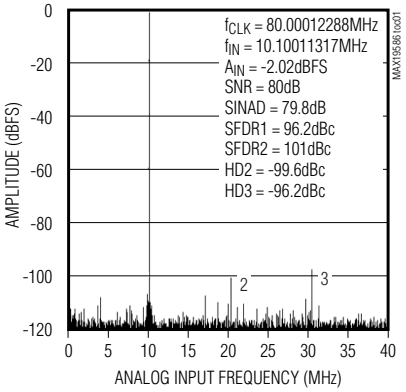
Note 1: ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.
Note 2: Parameter guaranteed by design and characterization.
Note 3: AC parameter measured in a 32,768-point FFT record, where the first 2 bins of the FFT and 2 bins on either side of the carrier are excluded.

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

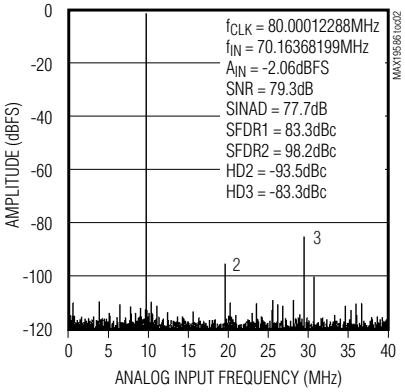
Typical Operating Characteristics

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, INP and INN driven differentially, internal reference, CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = +25°C. Unless otherwise noted, all AC data based on 32k-point FFT records and under coherent sampling conditions.)

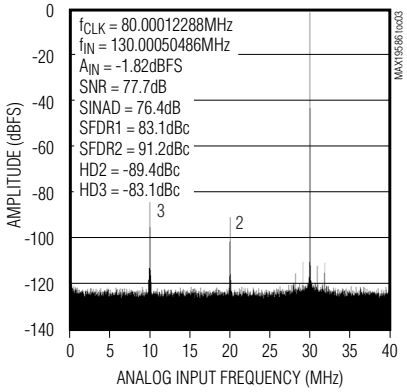
FFT PLOT (32,768-POINT RECORD)



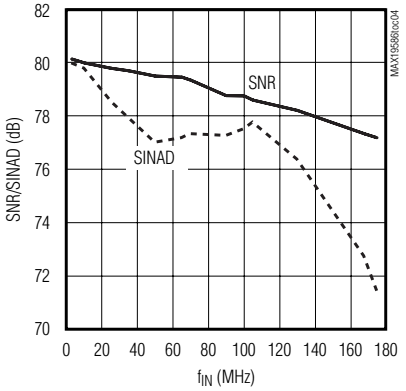
FFT PLOT (32,768-POINT RECORD)



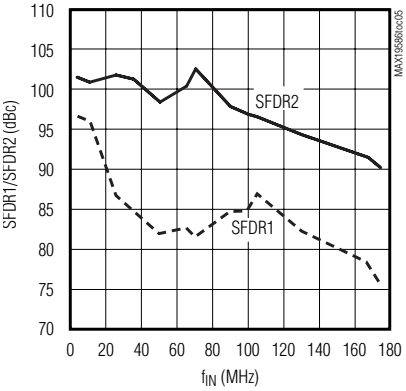
FFT PLOT (261,244-POINT DATA RECORD)



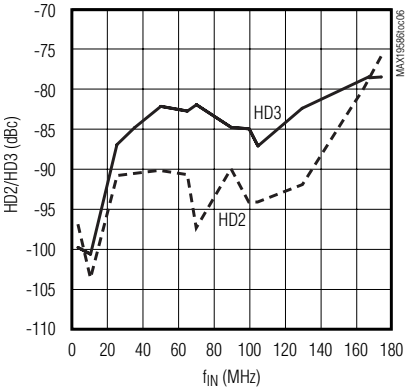
SNR/SINAD vs. ANALOG INPUT FREQUENCY (f_{CLK} = 80MHz, A_{IN} = -2dBFS)



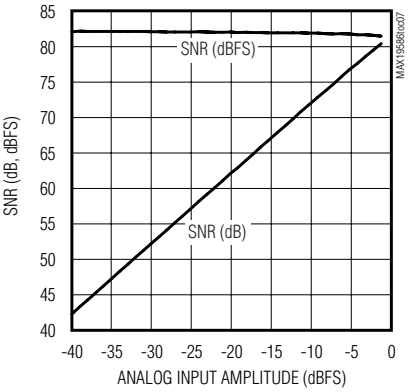
SFDR1/SFDR2 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 80MHz, A_{IN} = -2dBFS)



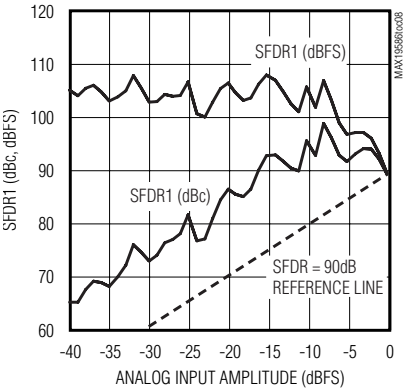
HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 80MHz, A_{IN} = -2dBFS)



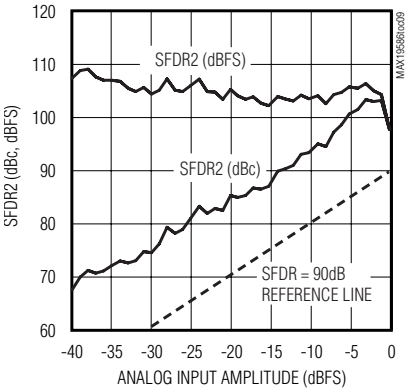
SNR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz)



SFDR1 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz)



SFDR2 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz)

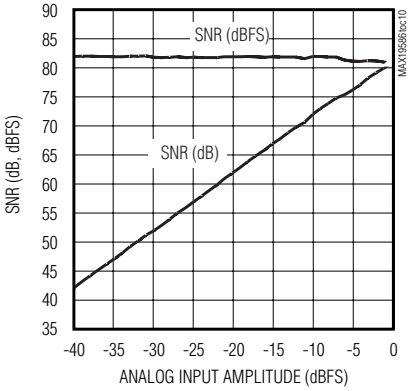


High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

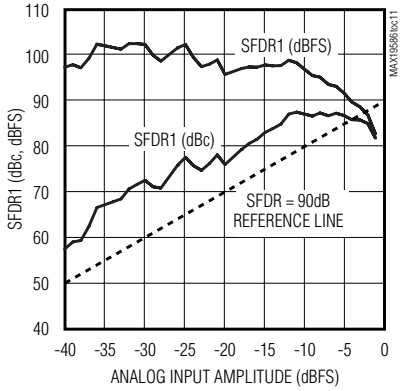
Typical Operating Characteristics (continued)

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, INP and INN driven differentially, internal reference, CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = +25°C. Unless otherwise noted, all AC data based on 32k-point FFT records and under coherent sampling conditions.)

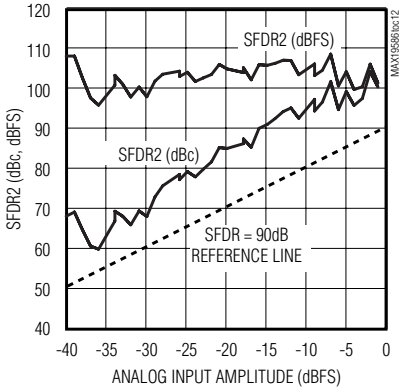
SNR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz)



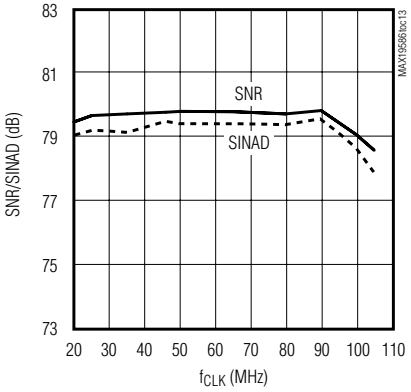
SFDR1 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz)



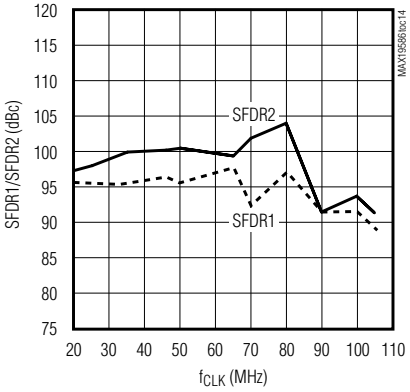
SFDR2 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz)



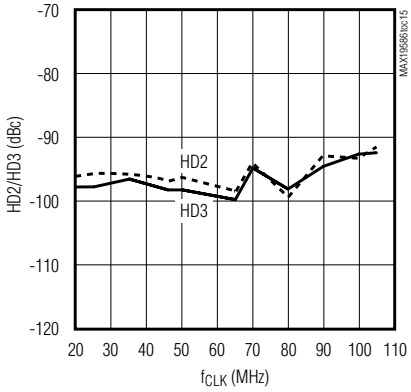
SNR/SINAD vs. SAMPLING FREQUENCY (f_{IN} = 9.9757395MHz, A_{IN} = -2dBFS)



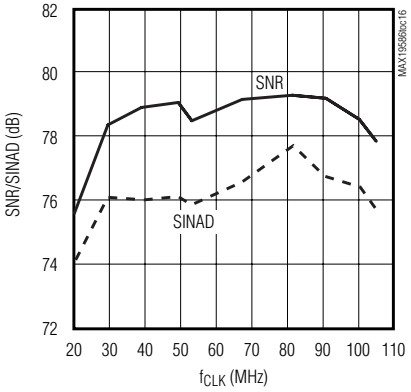
SFDR/SFDR2 vs. SAMPLING FREQUENCY (f_{IN} = 10.10011MHz, A_{IN} = -2dBFS)



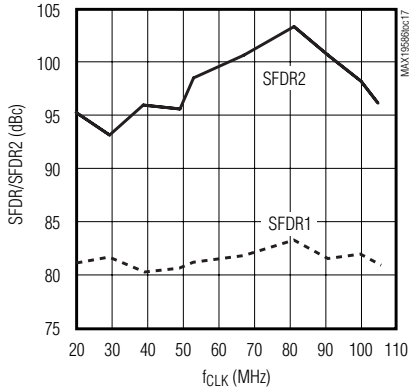
HD2/HD3 vs. SAMPLING FREQUENCY (f_{IN} = 10.10011MHz, A_{IN} = -2dBFS)



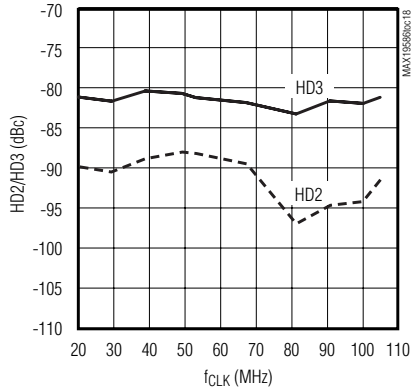
SNR/SINAD vs. SAMPLING FREQUENCY (f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)



SFDR1/SFDR2 vs. SAMPLING FREQUENCY (f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)



HD2/HD3 vs. SAMPLING FREQUENCY (f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)

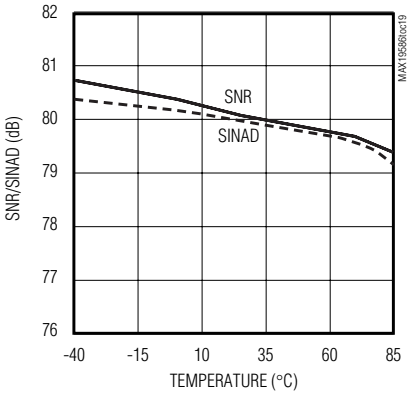


High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

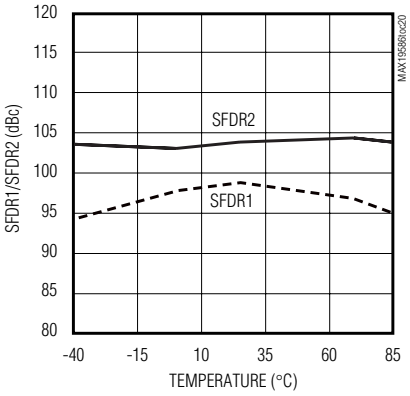
Typical Operating Characteristics (continued)

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, INP and INN driven differentially, internal reference, CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = +25°C. Unless otherwise noted, all AC data based on 32k-point FFT records and under coherent sampling conditions.)

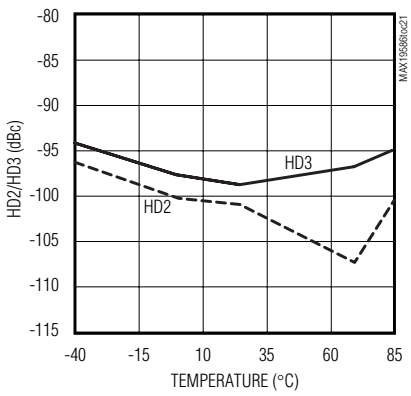
SNR/SINAD vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz, A_{IN} = -2dBFS)



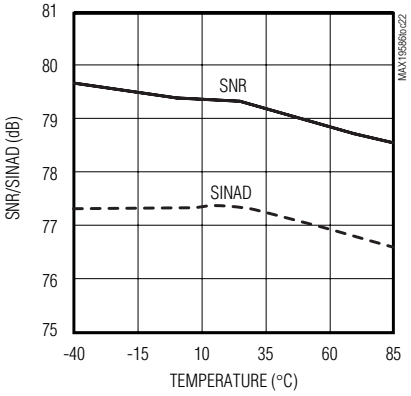
SFDR1/SFDR2 vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz, A_{IN} = -2dBFS)



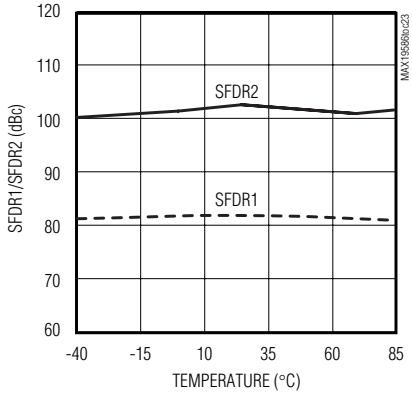
HD2/HD3 vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 10.10011MHz, A_{IN} = -2dBFS)



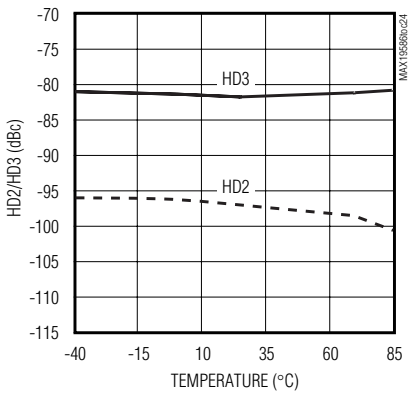
SNR/SINAD vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)



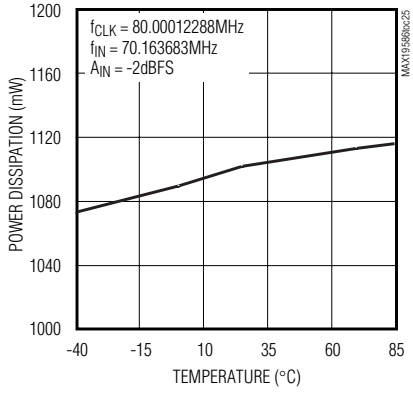
SFDR1/SFDR2 vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)



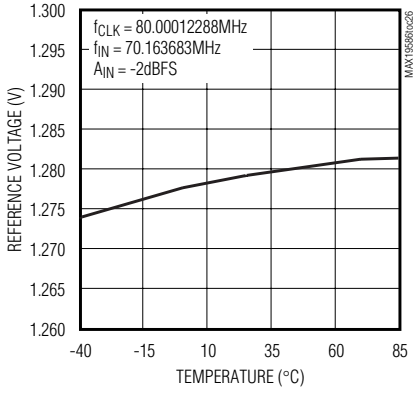
HD2/HD3 vs. TEMPERATURE (f_{CLK} = 80MHz, f_{IN} = 70.163683MHz, A_{IN} = -2dBFS)



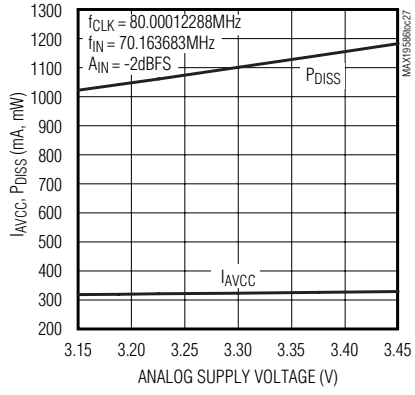
POWER DISSIPATION vs. TEMPERTURE



REFERENCE VOLTAGE vs. TEMPERTURE



POWER DISSIPATION vs. ANALOG SUPPLY VOLTAGE

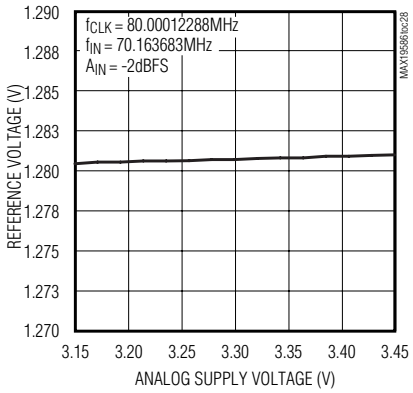


High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

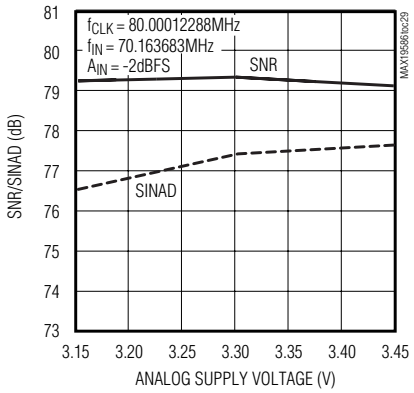
Typical Operating Characteristics (continued)

(AV_{DD} = 3.3V, DV_{DD} = 1.8V, INP and INN driven differentially, internal reference, CLKP and CLKN driven differentially, C_L = 5pF at digital outputs, f_{CLK} = 80MHz, T_A = +25°C. Unless otherwise noted, all AC data based on 32k-point FFT records and under coherent sampling conditions.)

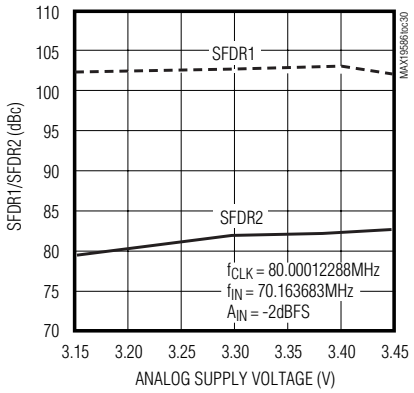
REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



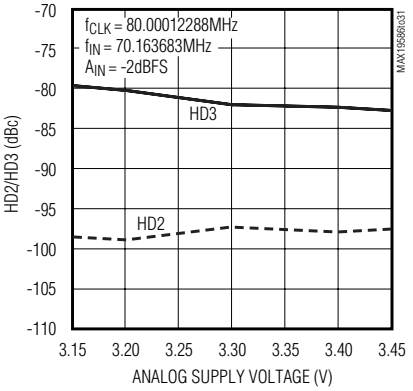
SNR/SINAD vs. ANALOG SUPPLY VOLTAGE



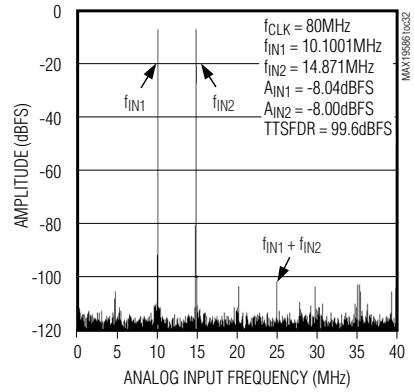
SFDR1/SFDR2 vs. ANALOG SUPPLY VOLTAGE



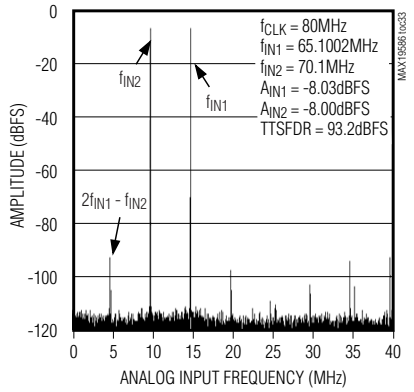
HD2/HD3 vs. ANALOG SUPPLY VOLTAGE



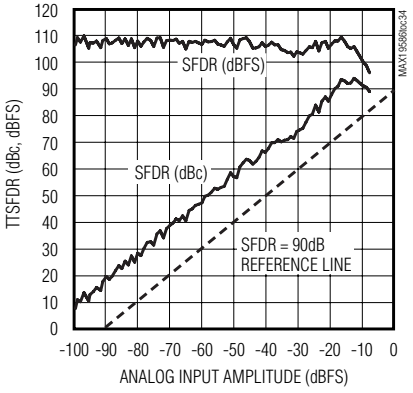
TWO-TONE SFDR PLOT (32,768-POINT DATA RECORD)



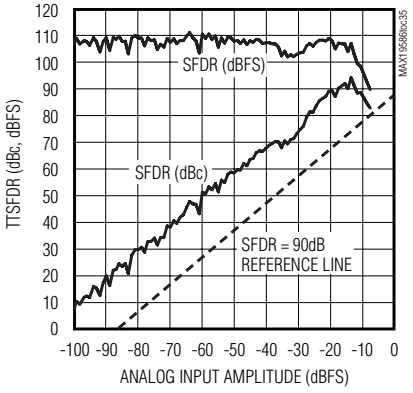
TWO-TONE SFDR PLOT (32,768-POINT DATA RECORD)



TWO-TONE SFDR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN1} = 10.1MHz, f_{IN2} = 14.87MHz)



TWO-TONE SFDR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 80MHz, f_{IN1} = 65.1MHz, f_{IN2} = 70.1MHz)



High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

Pin Description

PIN	NAME	FUNCTION
1, 2, 17, 18, 19, 23, 24, 25, 55, 56	AV_{DD}	Analog Supply Voltage. Provide local bypassing to ground with 0.01µF and 0.1µF capacitors.
3, 6–9, 12, 13, 14, 20, 21, 22, 28	AGND	Converter Ground. Analog, digital, and output-driver grounds are internally connected to the same potential. Connect the converter's exposed paddle (EP) to GND.
4	CLKP	Differential Clock, Positive Input Terminal
5	CLKN	Differential Clock, Negative Input Terminal
10	INP	Differential Analog Input, Positive Terminal
11	INN	Differential Analog Input, Negative/Complementary Terminal
15, 16, 54	N.C.	No Connection. **Do not connect to this pin.**
26	REFOUT	Internal Bandgap Reference Output
27	REFIN	Reference Voltage Input
29, 41, 42, 51	DV_{DD}	Digital Supply Voltage. Provide local bypassing to ground with 0.01µF and 0.1µF capacitors.
30, 31, 52	DGND	Converter Ground. Digital output-driver ground.
32	D0	Digital CMOS Output Bit 0 (LSB)
33	D1	Digital CMOS Output Bit 1
34	D2	Digital CMOS Output Bit 2
35	D3	Digital CMOS Output Bit 3
36	D4	Digital CMOS Output Bit 4
37	D5	Digital CMOS Output Bit 5
38	D6	Digital CMOS Output Bit 6
39	D7	Digital CMOS Output Bit 7
40	D8	Digital CMOS Output Bit 8
43	D9	Digital CMOS Output Bit 9
44	D10	Digital CMOS Output Bit 10
45	D11	Digital CMOS Output Bit 11
46	D12	Digital CMOS Output Bit 12
47	D13	Digital CMOS Output Bit 13
48	D14	Digital CMOS Output Bit 14
49	D15	Digital CMOS Output Bit 15 (MSB)
50	DAV	Data Valid Output. This output can be used as a clock control line to drive an external buffer or data-acquisition system. The typical delay time between the falling edge of the converter clock and the rising edge of DAV is 3.8ns.
53	DOR	Data Over-Range Bit. This control line flags an over-/under-range condition in the ADC. If DOR transitions high, an over-/under-range condition was detected. If DOR remains low, the ADC operates within the allowable full-scale range.
—	EP	Exposed Paddle. **Must be connected to AGND.**

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

Detailed Description

Figure 1 provides an overview of the MAX19586 architecture. The MAX19586 employs an input track-and-hold (T/H) amplifier, which has been optimized for low thermal noise and low distortion. The high-impedance differential inputs to the T/H amplifier (INP and INN) are self-biased at 2.2V, and support a full-scale 2.56V_{P-P} differential input voltage. The output of the T/H amplifier is applied to a multistage pipelined ADC core, which is designed to achieve a very low thermal noise floor and low distortion.

A clock buffer receives a differential input clock waveform and generates a low-jitter clock signal for the input T/H. The signal at the analog inputs is sampled at the rising edge of the differential clock waveform. The differential clock inputs (CLKP and CLKN) are high-impedance inputs, are self-biased at 1.6V, and support differential clock waveforms from 1V_{P-P} to 5V_{P-P}.

The outputs from the multistage pipelined ADC core are delivered to error correction and formatting logic, which deliver the 16-bit output code in two's-complement format to digital output drivers. The output drivers provide 1.8V CMOS-compatible outputs.

Analog Inputs (INP, INN)

The signal inputs to the MAX19586 (INP and INN) are balanced differential inputs. This differential configuration provides immunity to common-mode noise coupling and rejection of even-order harmonic terms. The differential signal inputs to the MAX19586 should be AC-coupled and carefully balanced to achieve the best dynamic performance (see *Differential, AC-Coupled Analog Inputs* in the *Applications Information* section for more details). AC-coupling of the input signal is required because the MAX19586 inputs are self-biasing as shown in Figure 2. Although the track-and-hold inputs are high impedance, the actual differential input impedance is nominally 10kΩ because of the two 5kΩ resistors connected to the common-mode bias circuitry.

Avoid injecting any DC leakage currents into these analog inputs. Exceeding a DC leakage current of 10µA shifts the self-biased common-mode level, adversely affecting the converter's performance.

On-Chip Reference Circuit

The MAX19586 incorporates an on-chip 1.28V, low-drift bandgap reference. This reference potential establishes the full-scale range for the converter, which is nominally 2.56V_{P-P} differential (Figure 3). The internal reference voltage can be monitored by REFOUT. **To use the internal reference voltage the reference input (REFIN) must be connected to REFOUT through a 10kΩ resistor.** Bypass both pins with separate 1µF capacitors to AGND.

The MAX19586 also allows an external reference source to be connected to REFIN, enabling the user to overdrive the internal bandgap reference. REFIN accepts a 1.28V ±10% input voltage range.

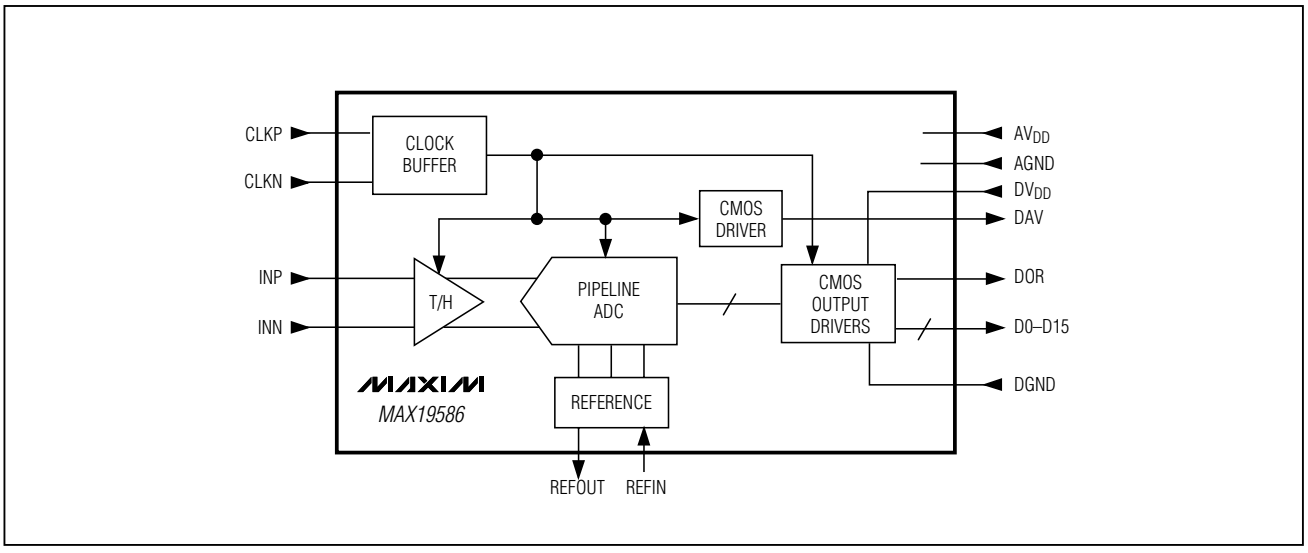


Figure 1. Block Diagram

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

Clock Inputs (CLKP, CLKN)

The differential clock buffer for the MAX19586 has been designed to accept an AC-coupled clock waveform. Like the signal inputs, the clock inputs are self-biasing. In this case, the self-biased potential is 1.6V and each input is connected to the reference potential with a 5kΩ resistor. Consequently, the differential input resistance associated with the clock inputs is 10kΩ. While differential clock signals as low as $0.5V_{P-P}$ can be used to drive the clock inputs, best dynamic performance is achieved with $1V_{P-P}$ to $5V_{P-P}$ clock input voltage levels.

Jitter on the clock signal translates directly to jitter (noise) on the sampled signal. Therefore, the clock source must be a very low-jitter (low-phase-noise) source. Additionally, extremely low phase-noise oscillators and bandpass filters should be used to obtain the true AC performance of this converter. See the *Differential, AC-Coupled Clock Inputs* and *Testing the MAX19586* topics in the *Applications Information* section for additional details on the subject of driving the clock inputs.

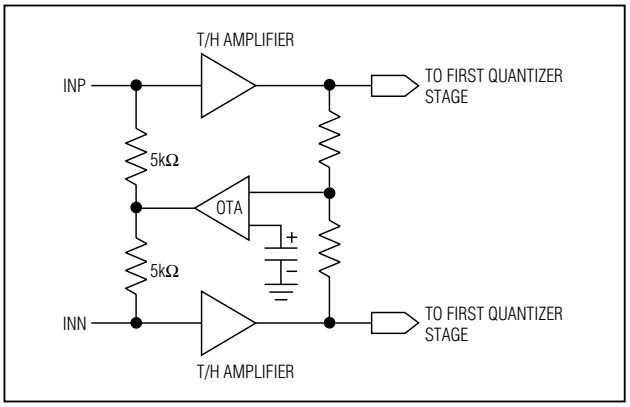


Figure 2. Simplified Analog Input Architecture

System Timing Requirements

Figure 4 depicts the general timing relationships for the signal input, clock input, data output, and DAV output. Figure 5 shows the detailed timing specifications and signal relationships, as defined in the *Electrical Characteristics* table.

The MAX19586 samples the input signal on the rising edge of the input clock. Output data is valid on the rising edge of the DAV signal, with a 7 clock-cycle data latency. Note that the clock duty cycle should typically be 50% ±10% for proper operation.

Digital Outputs (D0–D15, DAV, DOR)

Although designed for low-voltage 1.8V logic systems, the logic-high level of the low-voltage CMOS-compatible digital outputs (D0–D15, DAV, and DOR) offer some flexibility, as it allows the user to select the digital voltage within the 1.7V to 1.9V range.

For best performance, the capacitive loading on the digital outputs of the MAX19586 should be kept as low as possible (< 10pF). Due to the current-limited data-output driver of the MAX19586, large capacitive loads increase the rise and fall time of the data and can make it more difficult to register the data into the next IC. The loading capacitance can be kept low by keeping the output traces short and by driving a single CMOS buffer or latch input (as opposed to multiple CMOS inputs). The output data is in two's-complement format, as illustrated in Table 1.

Data is valid at the rising edge of DAV (Figures 4, 5). DAV may be used as a clock signal to latch the output data. Note that the DAV output driver is not current limited, hence it allows for higher capacitive loading.

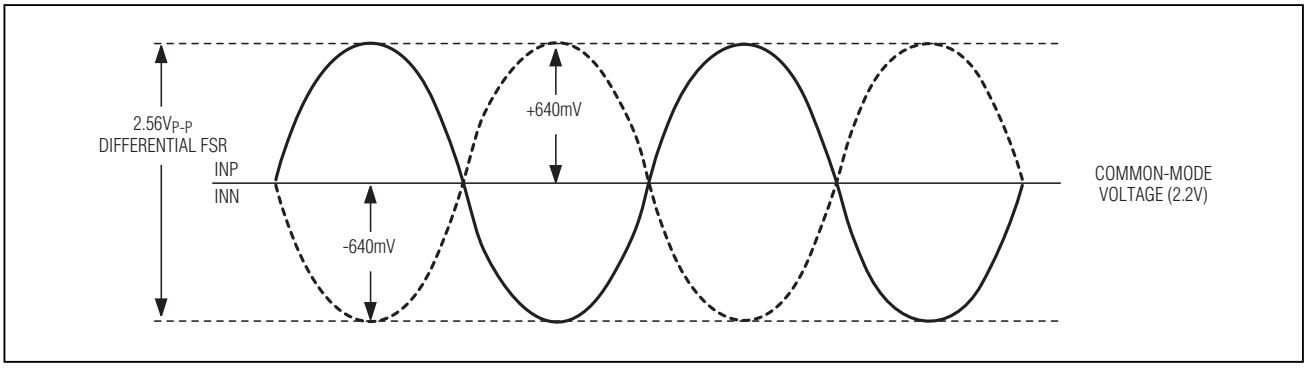


Figure 3. Full-Scale Voltage Range

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

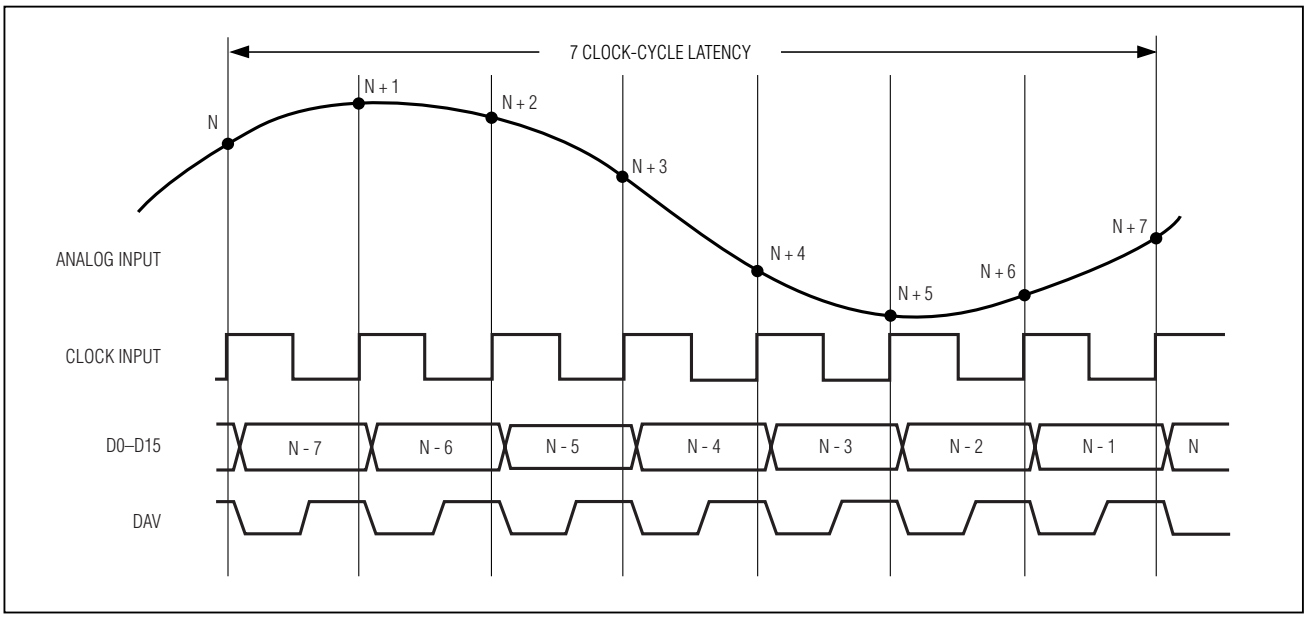
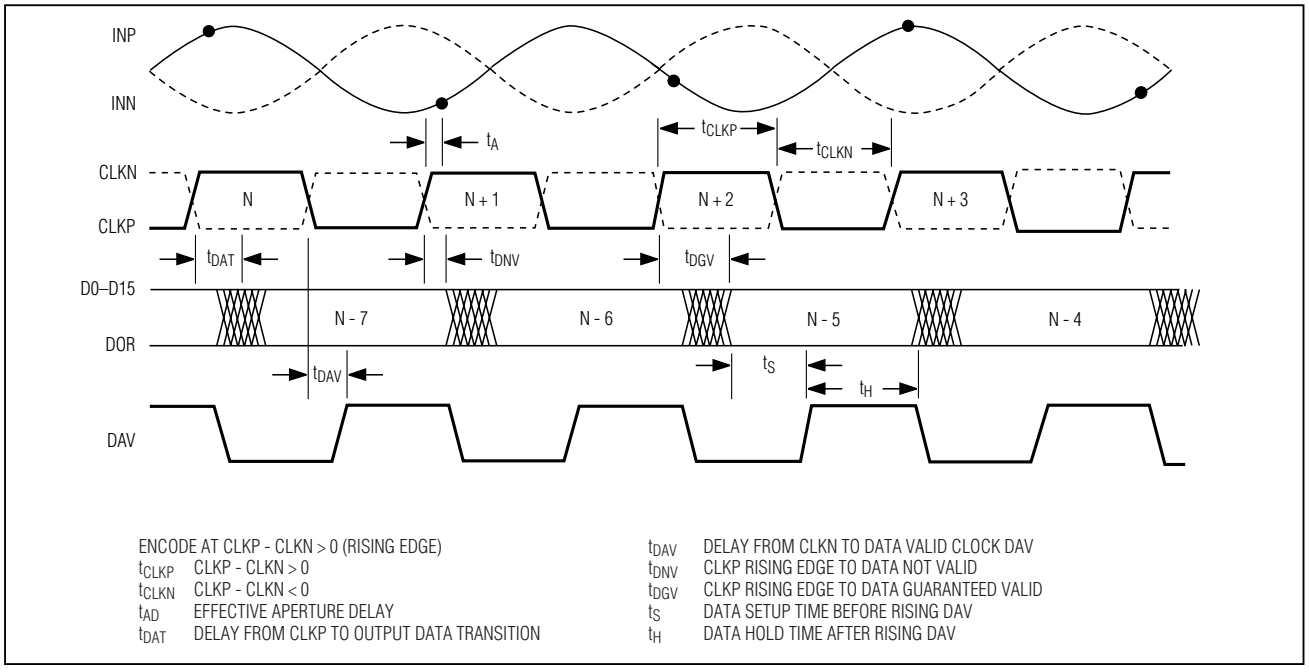


Figure 4. General System and Output Timing Diagram



ENCODE AT CLKP - CLKN > 0 (RISING EDGE)

t_{CLKP}	CLKP - CLKN > 0	t_{DAV}	DELAY FROM CLKN TO DATA VALID CLOCK DAV
t_{CLKN}	CLKP - CLKN < 0	t_{DNV}	CLKP RISING EDGE TO DATA NOT VALID
t_{AD}	EFFECTIVE APERTURE DELAY	t_{DGV}	CLKP RISING EDGE TO DATA GUARANTEED VALID
t_{DAT}	DELAY FROM CLKP TO OUTPUT DATA TRANSITION	t_S	DATA SETUP TIME BEFORE RISING DAV
		t_H	DATA HOLD TIME AFTER RISING DAV

Figure 5. Detailed Timing Information for Clock Operation

Table 1. MAX19586 Digital Output Coding

INP ANALOG VOLTAGE LEVEL	INN ANALOG VOLTAGE LEVEL	D15–D0 TWO'S-COMPLEMENT CODE
V_{CM} + 0.64V	V_{CM} - 0.64V	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 (positive full-scale)
V_{CM}	V_{CM}	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 (midscale + δ) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 (midscale - δ)
V_{CM} - 0.64V	V_{CM} + 0.64V	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 (negative full-scale)

The converter's DOR output signal is used to identify over- and under-range conditions. If the input signal exceeds the positive or negative full-scale range for the MAX19586 then DOR will be asserted high. The timing for DOR is identical to the timing for the data outputs, and DOR therefore provides an over-range indication on a sample-by-sample basis.

Applications Information

Differential, AC-Coupled Clock Inputs

The clock inputs to the MAX19586 are driven with an AC-coupled differential signal, and best performance is achieved under these conditions. However, it is often the case that the available clock source is single-ended. Figure 6 demonstrates one method for converting a single-ended clock signal into a differential signal with a transformer. In this example, the transformer turns ratio from the primary to secondary side is 1:1.414. The impedance ratio from primary to secondary is the square of the turns ratio, or 1:2. So terminating the secondary side with a 100Ω differential resistance results in a 50Ω load looking into the primary side of the transformer. The termination resistor in this example is comprised of the series combination of two 50Ω resistors with their common node AC-coupled to ground.

Figure 6 illustrates the secondary side of the transformer to be coupled directly to the clock inputs. Since the clock inputs are self-biasing, the center tap of the transformer must be AC-coupled to ground or left floating. If the center tap of the transformer's secondary side is DC-coupled to ground, it is necessary to add blocking capacitors in series with the clock inputs.

Clock jitter is generally improved if the clock signal has a high slew rate at the time of its zero-crossing. Therefore, if a sinusoidal source is used to drive the clock inputs the clock amplitude should be as large as possible to maximize the zero-crossing slew rate. The back-to-back Schottky diodes shown in Figure 6 are not required as long as the input signal is held to a differential voltage potential of $3V_{P-P}$ or less. If a larger amplitude signal is provided (to maximize the zero-crossing slew rate), then the diodes serve to limit the differential signal swing at the clock inputs. Note that all AC specifications for the MAX19586 are measured within this configuration and with an input clock amplitude of approximately 12dBm.

Any differential mode noise coupled to the clock inputs translates to clock jitter and degrades the SNR performance of the MAX19586. Any differential mode coupling of the analog input signal into the clock inputs results in harmonic distortion. Consequently, it is important that the clock lines be well isolated from the analog signal input and from the digital outputs. See the *Signal Routing* section for more discussion on the subject of noise coupling.

Differential, AC-Coupled Analog Inputs

The analog inputs INP and INN are driven with a differential AC-coupled signal. It is important that these inputs be accurately balanced. Any common-mode signal applied to these inputs degrades even-order distortion terms. Therefore, any attempt at driving these inputs in a single-ended fashion will result in significant even-order distortion terms.

Figure 7 presents one method for converting a single-ended signal to a balanced differential signal using a transformer. The primary-to-secondary turns ratio in this example is 1:1.414. The impedance ratio is the square of the turns ratio, so in this example the impedance ratio is 1:2. To achieve a 50Ω input impedance at the primary side of the transformer, the secondary side is terminated with a 100Ω differential load. This load, in shunt with the differential input resistance of the MAX19586, results in a 100Ω differential load on the secondary side. It is rea-

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

sonable to use a larger transformer turns ratio to achieve a larger signal step-up, and this may be desirable to relax the drive requirements for the circuitry driving the MAX19586. However, the larger the turns ratio, the larger the effect of the differential input impedance of the MAX19586 on the primary-referred input impedance.

As stated previously, the signal inputs to the MAX19586 must be accurately balanced to achieve the best even-order distortion performance.

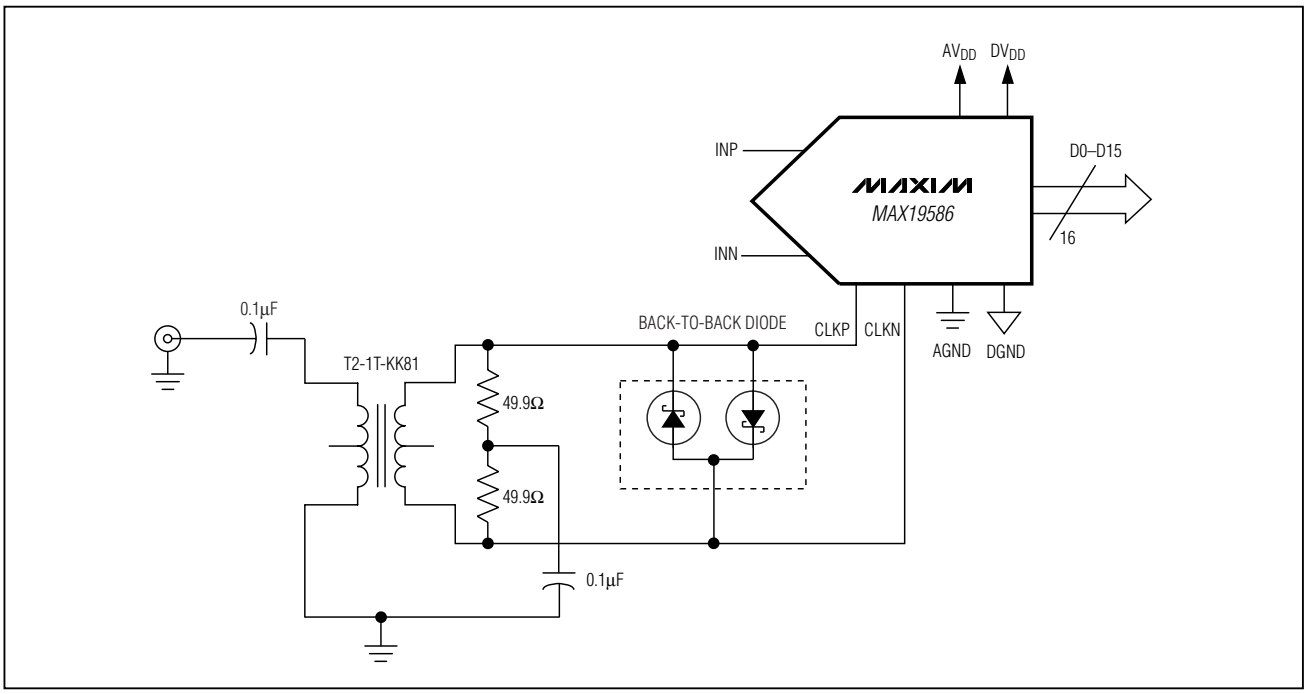


Figure 6. Transformer-Coupled Clock Input Configuration

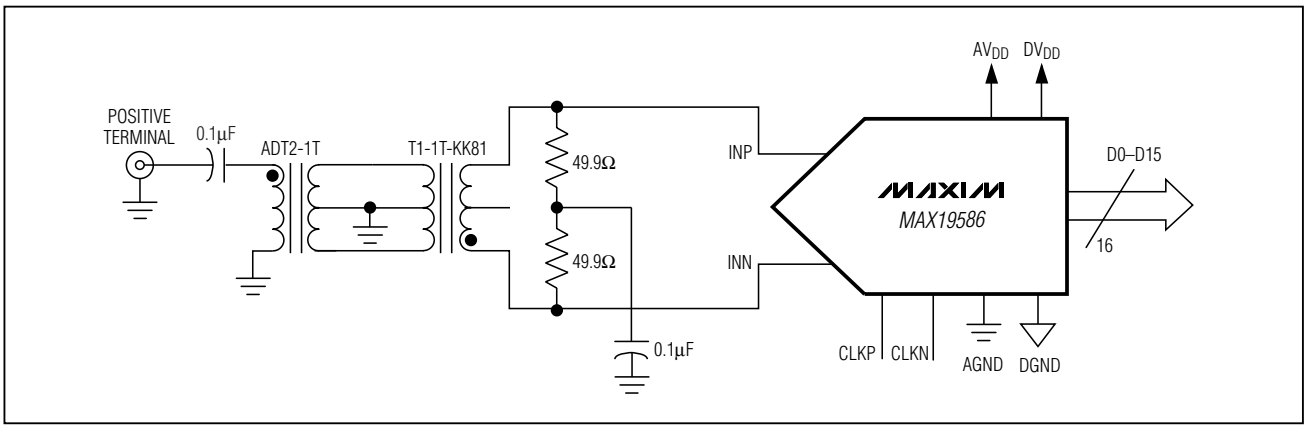


Figure 7. Transformer-Coupled Analog Input Configuration with Primary-Side Balun Transformer

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

One note of caution in relation to transformers is important. Any DC current passed through the primary or secondary windings of a transformer may magnetically bias the transformer core. When this happens the transformer is no longer accurately balanced and a degradation in the distortion of the MAX19586 may be observed. The core must be demagnetized to return to balanced operation.

Testing the MAX19586

The MAX19586 has a very low thermal noise floor (-82dBFS) and very low jitter (< 100fs). As a consequence, test system limitations can easily obscure the performance of the ADC. Figure 8a is a block diagram of a conventional high-speed ADC test system. The input signal and the clock source are generated by low-phase-noise synthesizers (e.g., Agilent 8644B). Bandpass filters in both the signal and the clock paths then attenuate noise and harmonic components.

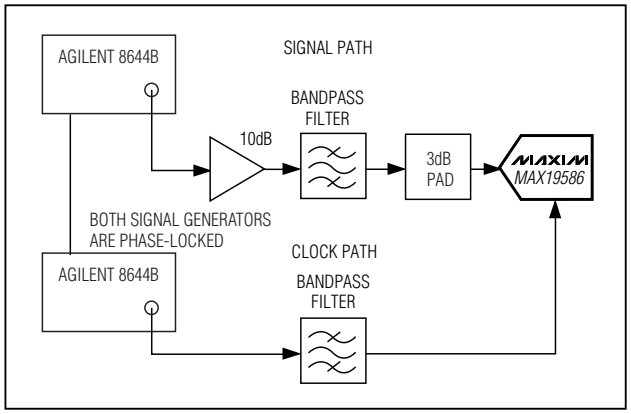


Figure 8a. Standard High-Speed ADC Test Setup (Simplified Block Diagram)

Figure 8b shows the resulting power spectrum, which results from this setup for a 70MHz input tone and an 80Msps clock. Note the substantial lift in the noise floor near the carrier. The bandwidth of this particular noise-floor lift near the carrier corresponds to the bandwidth of the filter in the input signal path.

Figure 8c illustrates the impact on the spectrum if the input frequency is shifted away from the center frequency of the input signal filter. Note that the fundamental tone has moved, but the noise-floor lift remains in the same location. This is evidence of the validity of the claim that the lift in the noise floor is due to the test system and not the ADC. In this figure, the magnitude of the lift in the noise floor increased relative to the previous figure because the signal is located on the skirt of the filter and the signal amplitude had to be increased to obtain a signal near full scale.

To truly reveal the performance of the MAX19586, the test system performance must be improved substantially. Figure 8d depicts such an improved test system. In this system, the synthesizers provide reference inputs to two dedicated low-noise phase-locked loops (PLLs), one centered at approximately 80MHz (for the clock path) and the other centered at 70MHz (for the signal path). The oscillators in these PLLs are very low-noise oscillators, and the

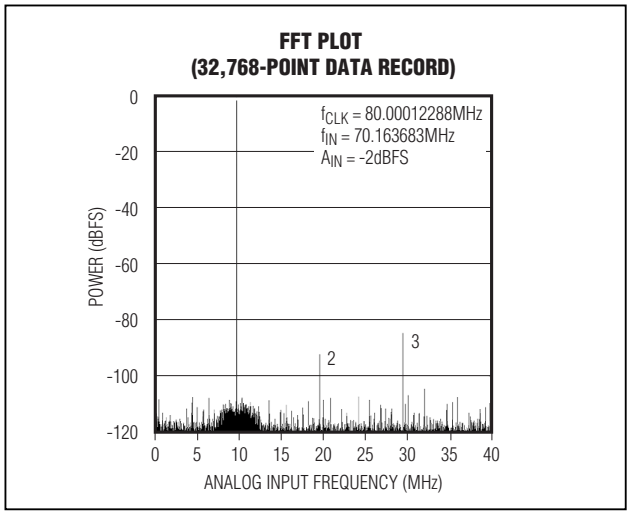


Figure 8b. 70MHz FFT with Standard High-Speed ADC Test Setup

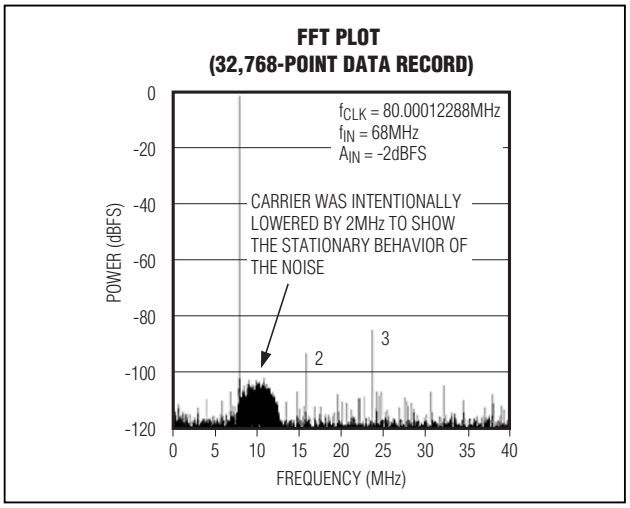


Figure 8c. 68MHz FFT with Standard High-Speed ADC Test Setup

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

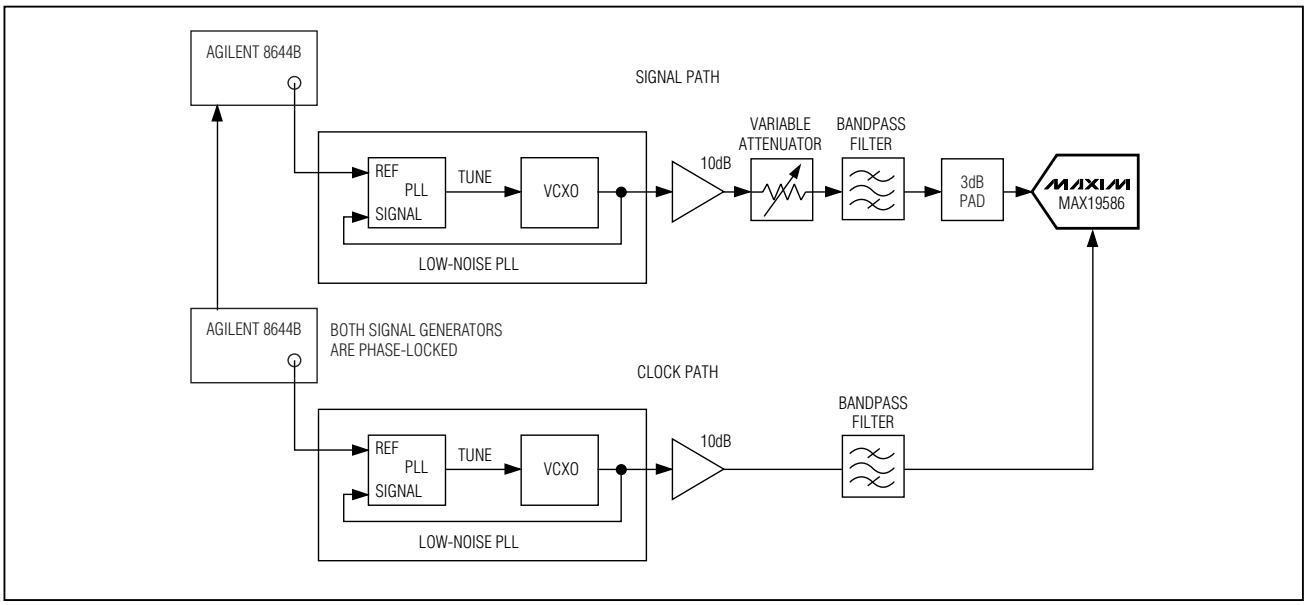


Figure 8d. Improved Test System Employing Narrowband PLLs (Simplified Block Diagram)

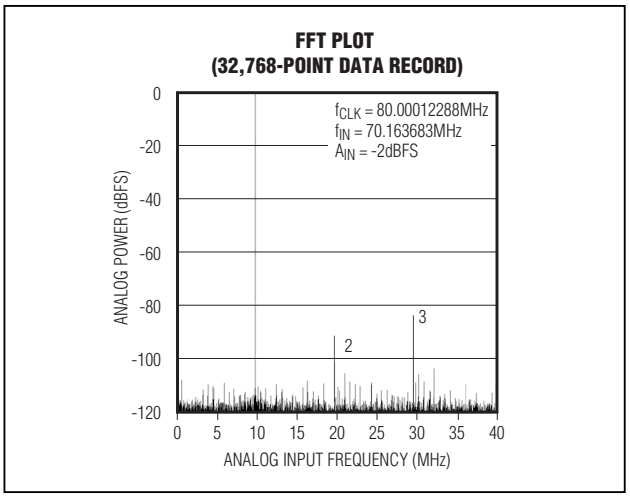


Figure 8e. 70MHz FFT with Improved High-Speed ADC Test Setup

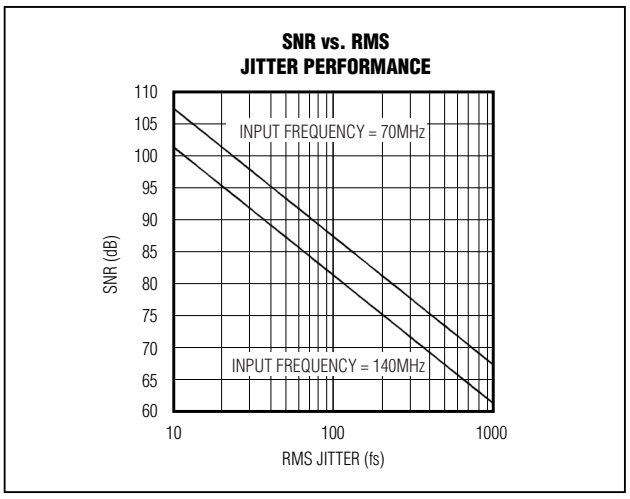


Figure 8f. SNR vs. System Jitter Performance Graph

PLLs act as extremely narrow bandwidth filters (on the order of 20Hz) to attenuate the noise of the synthesizers. The system provides a total system jitter on the order of 20fs. Note that while the low-noise oscillators could be used by themselves without being locked to their respective signal sources, this would result in FFTs that are not coherent and which would require windowing.

Figure 8e is an FFT plot of the spectrum obtained when the improved test system is employed. The noise-floor lift in the vicinity of the carrier is now almost completely eliminated. The SNR associated with this FFT is about 79.1dB, whereas the SNR obtained using the standard test system is on the order of 77.6dB.

Figure 8f demonstrates the impact of test system jitter on measured SNR. The figure plots SNR due to test system jitter only, neglecting all other sources of noise, for two different input frequencies. For example, note that for a 70MHz input frequency a test system jitter number of 100fs results in an SNR (due to the test system alone) of about 87.1dB. In the case of the MAX19586, which has a -82dBFS noise floor, this is not an inconsequential amount of additional noise.

In conclusion, careful attention must be paid to both the input signal source and the clock signal source, if the true performance of the MAX19586 is to be properly characterized. Dedicated PLLs with low-noise VCOs, such as those used in Figure 8d, are capable of providing signals with the required low jitter performance.

Layer Assignments

The MAX19586 EV kit is a 6-layer board, and the assignment of layers is discussed in this context. It is recommended that the ground plane be on a layer between the signal routing layer and the supply routing layer(s). This prevents coupling from the supply lines into the signal lines. The MAX19586 EV kit PC board places the signal lines on the top (component) layer and the ground plane on layer 2. Any region on the top layer not devoted to signal routing is filled with the ground plane with vias to layer 2. Layers 3 and 4 are devoted to supply routing, layer 5 is another ground plane, and layer 6 is used for the placement of additional components and for additional signal routing.

A four-layer implementation is also feasible using layer 1 for signal lines, layer 2 as a ground plane, layer 3 for supply routing, and layer 4 for additional signal routing. However, care must be taken to ensure that the clock and signal lines are isolated from each other and from the supply lines.

Signal Routing

To preserve good even-order distortion, the signal lines (those traces feeding the INP and INN inputs) must be carefully balanced. To accomplish this, the signal traces should be made as symmetric as possible, meaning that each of the two signal traces should be the same length and should see the same parasitic environment. As mentioned previously, the signal lines must be isolated from the supply lines to prevent coupling from the supplies to the inputs. This is accomplished by making the necessary layer assignments as described in the previous section. Additionally, it is crucial that the clock lines be isolated from the signal lines. On the MAX19586 EV kit this is done by routing the clock lines on the bottom layer (layer 6). The clock lines then connect to the ADC through vias placed in close proximity to the device. The clock lines are isolated from the supply lines as well by virtue of the ground plane on layer 5.

As with all high-speed designs, digital output traces should be kept as short as possible to minimize capacitive loading. The ground plane on layer 2 beneath these traces should not be removed so that the digital ground return currents have an uninterrupted path back to the bypass capacitors.

Grounding

The practice of providing a split ground plane in an attempt to confine digital ground-return currents has often been recommended in ADC application literature. However, for converters such as the MAX19586 it is strongly recommended to employ a single, uninterrupted ground plane. The MAX19586 EV kit achieves excellent dynamic performance with such a ground plane.

The exposed paddle of the MAX19586 should be soldered directly to a ground pad on layer 1 with vias to the ground plane on layer 2. This provides excellent electrical and thermal connections to the PC board.

Supply Bypassing

The MAX19586 EV kit uses 220µF capacitors (and smaller values such as 47µF and 2µF) on power-supply lines AV_{DD} and DV_{DD} to provide low-frequency bypassing. The loss (series resistance) associated with these capacitors is beneficial in eliminating high-Q supply resonances. Ferrite beads are also used on each of the power-supply lines to enhance supply bypassing (Figure 9).

Combinations of small value (0.01µF and 0.1µF), low-inductance surface-mount capacitors should be placed at each supply pin or each grouping of supply pins to attenuate high-frequency supply noise. Place these capacitors on the top side of the board and as close to the converter as possible with short connections to the ground plane.

Parameter Definitions

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Ideally, the midscale MAX19586 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

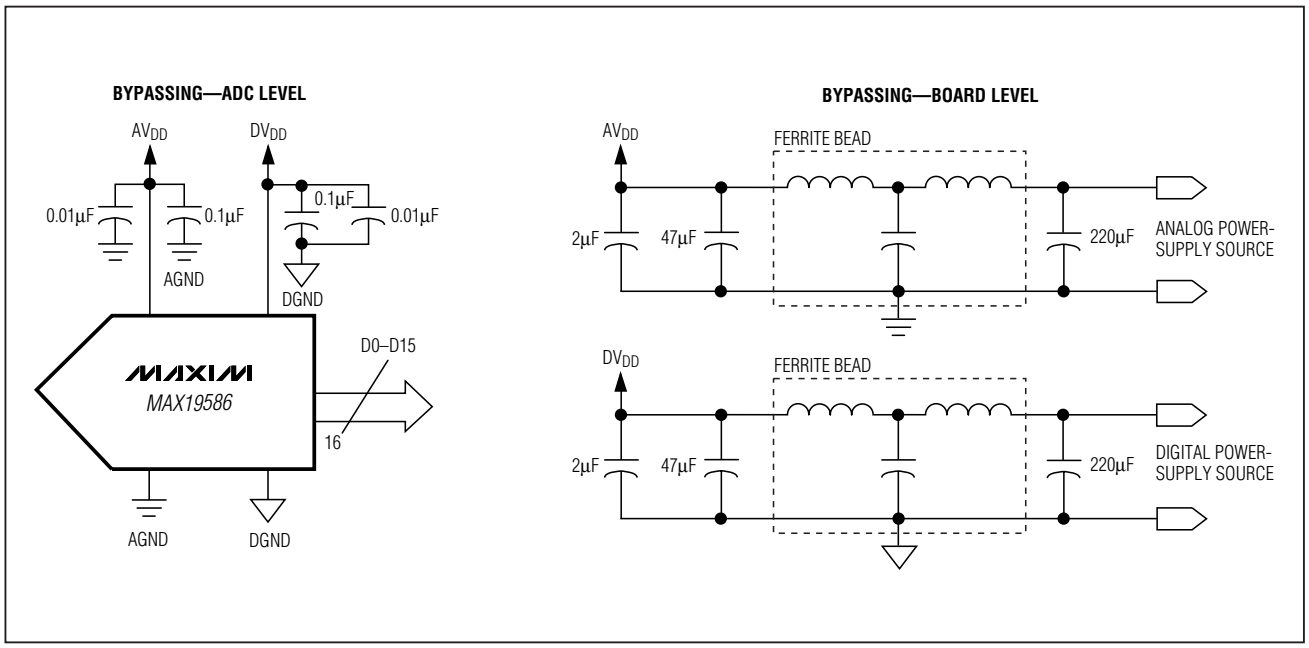


Figure 9. Grounding, Bypassing, and Decoupling Recommendations for the MAX19586

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The slope of the actual transfer function is measured between two data points: positive full scale and negative full scale. Ideally, the positive full-scale MAX19586 transition occurs at 1.5 LSBs below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

Small-Signal Noise Floor (SSNF)

Small-signal noise floor is the integrated noise and distortion power in the Nyquist band for small-signal inputs. The DC offset is excluded from this noise calculation. For this converter, a small signal is defined as a single tone with an amplitude of less than -35dBFS. This parameter captures the thermal and quantization noise characteristics of the data converter and can be used to help calculate the overall noise figure of a digital receiver signal path.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR[max] = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first four harmonics (HD2 through HD5), and the DC offset.

$$SNR = 20 \times \log (SIGNAL_{RMS} / NOISE_{RMS})$$

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

Spurious-Free Dynamic Range (SFDR1 and SFDR2)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR1 reflects the MAX19586 spurious performance based on worst 2nd- or 3rd-order harmonic distortion. SFDR2 is defined by the worst spurious component excluding 2nd- and 3rd-order harmonic spurs and DC offset.

Two-Tone Spurious-Free Dynamic Range (TTSFDR)

Two-tone SFDR is the ratio of the full scale of the converter to the RMS value of the peak spurious component. The peak spurious component can be related to the intermodulation distortion components, but does not have to be. Two-tone SFDR for the MAX19586 is expressed in dBFS.

Two-Tone Intermodulation Distortion (TTIMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -8dBFS. The intermodulation products are as follows:

Second-Order Intermodulation Products (IM2):
$f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$

Third-Order Intermodulation Products (IM3):
$2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$

Fourth-Order Intermodulation Products (IM4):
$3 \times f_{IN1} - f_{IN2}$, $3 \times f_{IN2} - f_{IN1}$, $3 \times f_{IN1} + f_{IN2}$, $3 \times f_{IN2} + f_{IN1}$, $2 \times f_{IN1} - 2 \times f_{IN2}$

Fifth-Order Intermodulation Products (IM5):
$3 \times f_{IN1} - 2 \times f_{IN2}$, $3 \times f_{IN2} - 2 \times f_{IN1}$, $3 \times f_{IN1} + 2 \times f_{IN2}$, $3 \times f_{IN2} + 2 \times f_{IN1}$, $4 \times f_{IN1} - f_{IN2}$

Note that the two-tone intermodulation distortion is measured with respect to a single-carrier amplitude and not the peak-to-average input power of both input tones.

Aperture Jitter

Aperture jitter (t_{AJ}) represents the sample-to-sample variation in the aperture delay specification.

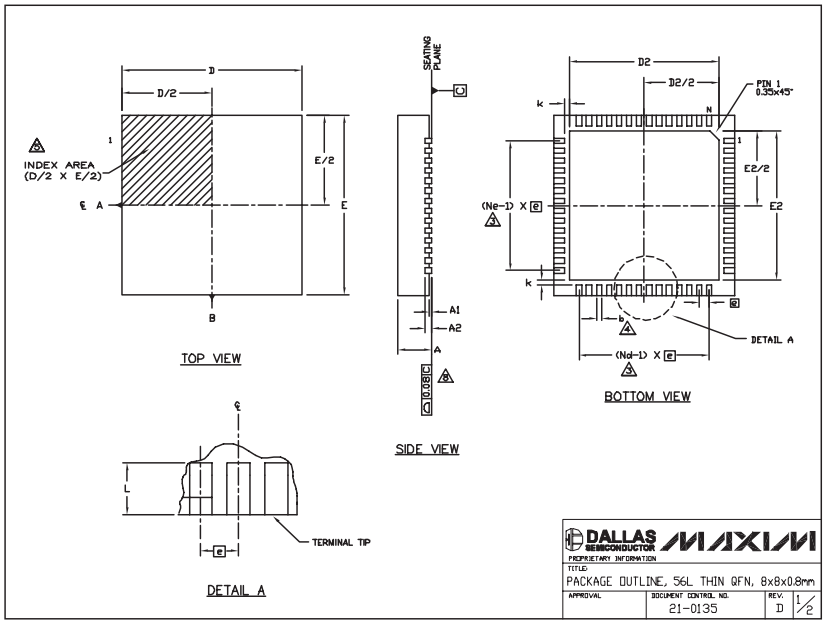
Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 5).

High-Dynamic-Range, 16-Bit, 80Msps ADC with -82dBFS Noise Floor

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.008 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN MATCHED AREA AS SHOWN.
   EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS.
   EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC	DOWN BONDS ALLOWED
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0135 | REV. D | 2/2