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19-0644; Rev 2; 2/09

# 4-Channel I²C Switches/Multiplexer



## General Description

The MAX7367/MAX7368/MAX7369 bidirectional, four-channel I²C switches/multiplexer expand the main I²C bus up to four extended buses. The MAX7369 1:4 multiplexer connects the main I²C bus to one channel at a time. The MAX7367/MAX7368 four-channel switches connect the main I²C bus to one or more channels at a time.

These devices isolate bus loading by extending the I²C bus onto different channels. The MAX7367/MAX7368/MAX7369 allow more devices to be interconnected to a master controller and multiple devices with the same I²C address to communicate to a master. The channels are selected through the main I²C bus by writing to the internal control register of the device.

Any device connected to an I²C bus can transmit and receive signals. The MAX7367/MAX7368/MAX7369 are transparent to signals sent and received at each channel, allowing multiple masters. These devices are compatible with the I²C protocol of clock stretch, synchronization, and arbitration in case multiple masters address the bus at the same time.

All devices are set to the default state during initial power-up. The MAX7367/MAX7368 have a $\overline{\text{RESET}}$ input allowing external circuitry to set the MAX7367/MAX7368 to its default state anytime after the device has powered up. The MAX7367/MAX7369 have interrupt inputs, allowing devices on the extended bus to send an interrupt signal to the master on the main bus.

The MAX7367/MAX7369 are available in 20-pin TSSOP packages, and the MAX7368 is available in a 16-pin TSSOP package. All devices operate over the -40°C to +85°C extended temperature range.

## Applications

Servers
RAID
Cellular Phones
Base Stations
PCs
Multimedia Electronics
SAN/NAS

## Features

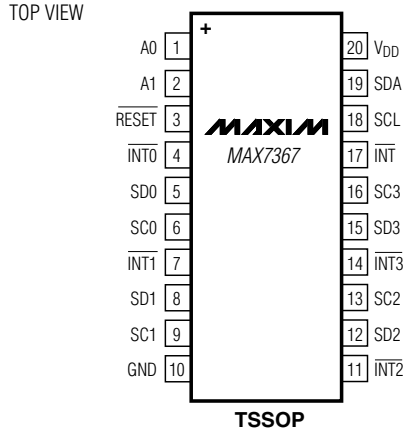
- **Four-Channel, Bidirectional Bus Expansion**
- **Voltage-Level Translation**
- **Low 6µA (typ) Supply Current, 0.1µA (typ) Standby Current**
- **Low 16Ω (typ) On-Resistance**
- **Channel Selection Through I²C**
- **I²C-Compatible Normal or Fast Mode**
- **Device Address Selection**
  **Up to Four Addresses (MAX7367)**
  **Up to Eight Addresses (MAX7368/MAX7369)**
- **Bus-Loading Isolation**
- **Support Clock Stretch, Synchronization, and Arbitration**
- **Hot Insertion**
- **2.3V to 5.5V Supply Voltage Range**
- **5V-Tolerant Inputs**
- **Interrupt from Extended Buses (MAX7367/MAX7369)**
- **Hardware Reset (MAX7367/MAX7368)**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX7367**EUP+ | -40°C to +85°C | 20 TSSOP |
| **MAX7368**EUE+ | -40°C to +85°C | 16 TSSOP |
| **MAX7369**EUP+ | -40°C to +85°C | 20 TSSOP |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Pin Configurations




*Pin Configurations continued at end of data sheet.*

# 4-Channel I²C Switches/Multiplexer

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....-0.3V to +6.0V
All Other Pins to GND .....-0.3V to +6.0V
Input Currents
  $V_{DD}$ .....100mA
  GND .....100mA
  All Input Pins .....±20mA
Output Current .....25mA

Continuous Power Dissipation ($T_A$ = +70°C)
  20-Pin TSSOP (derate 11.0mW/°C
  above $T_A$ = +70°C) ..... 879.1mW
  16-Pin TSSOP (derate 9.4mW/°C
  above $T_A$ = +70°C) ..... 754.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS (3.3V SUPPLY)

($V_{DD}$ = 2.3V to 3.6V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = 3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Voltage | $V_{DD}$ | | 2.3 | | 3.6 | V |
| Standby Current | $I_{STB}$ | No load, all inputs = $V_{DD}$ or GND, $V_{DD}$ = 3.6V, all channels disabled | | 0.1 | 1 | µA |
| Supply Current | $I_{DD}$ | No load, all inputs = $V_{DD}$ or GND, $f_{SCL}$ = 100kHz, $V_{DD}$ = 3.6V, all channels disabled | | 6 | 30 | µA |
| Power-On-Reset (POR) Voltage | $V_{POR}$ | $V_{DD}$ rising | | 1.4 | 2.1 | V |
| Power-On-Reset Hysteresis | $V_{HYST}$ | | | 0.4 | | V |
| **INPUT SCL, INPUT/OUTPUT SDA** | | | | | | |
| Low-Level Input Voltage | $V_{IL}$ | (Note 2) | -0.2 | | +0.3 x $V_{DD}$ | V |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | | 5.5 | V |
| Low-Level Output Current | $I_{OL}$ | $V_{OL}$ = 0.4V | 3 | 30 | | mA |
| | | $V_{OL}$ = 0.6V | 6 | 50 | | |
| Input Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input Capacitance | $C_I$ | All inputs = GND | | 15 | | pF |
| **SELECT INPUTS A2, A1, A0, $\overline{INT0}$–$\overline{INT3}$, $\overline{RESET}$** | | | | | | |
| Low-Level Input Voltage | $V_{IL}$ | (Note 2) | -0.2 | | +0.3 x $V_{DD}$ | V |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | | 5.5 | V |
| Input Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input Capacitance | $C_I$ | All inputs = GND | | 5 | | pF |

## ELECRTICAL CHARACTERISTICS (3.3V SUPPLY) (continued)

($V_{DD}$ = 2.3V to 3.6V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = 3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PASS GATE** | | | | | | |
| Switch On-Resistance | $R_{ON}$ | $V_{DD}$ = 3V to 3.6V, $I_O$ = 15mA, $V_O$ = 0.4V | 5 | 16 | 30 | Ω |
| | | $V_{DD}$ = 2.3V to 2.7V, $I_O$ = 10mA, $V_O$ = 0.4V | 7 | 23 | 55 | |
| Switch Output Voltage | $V_{PASS}$ | $V_{I(SW)}$ = $V_{DD}$ = 3.0V to 3.6V, $I_O$ = -100µA | 1.6 | 1.9 | 2.8 | V |
| | | $V_{I(SW)}$ = $V_{DD}$ = 2.3V to 2.7V, $I_O$ = -100µA | 1.1 | | 2.0 | |
| | | $V_{I(SW)}$ = $V_{DD}$ = 2.5V, $I_O$ = -100µA | | 1.5 | | |
| Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input/Output Capacitance | $C_{IO}$ | All inputs = GND | | 6 | | pF |
| **$\overline{INT}$ OUTPUT** | | | | | | |
| Low-Level Output Current | $I_{OL}$ | $V_{OL}$ = 0.4V | 3 | | | mA |
| High-Level Output Current | $I_{OH}$ | | | | 1 | µA |

## ELECRTICAL CHARACTERISTICS (5V SUPPLY)

($V_{DD}$ = 4.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = 5V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Voltage | $V_{DD}$ | | 4.5 | | 5.5 | V |
| Standby Current | $I_{STB}$ | No load, all inputs = $V_{DD}$ or GND, $V_{DD}$ = 5.5V, all channels disabled | | 0.3 | 1 | µA |
| Supply Current | $I_{DD}$ | No load, all inputs = $V_{DD}$ or GND, $f_{SCL}$ = 100kHz, $V_{DD}$ = 5.5V, all channels disabled | | 12 | 50 | µA |
| Power-On-Reset Voltage | $V_{POR}$ | $V_{DD}$ rising | | 1.4 | 2.1 | V |
| POR Hysteresis | $V_{HYST}$ | | | 0.4 | | V |
| **INPUT SCL, INPUT/OUTPUT SDA** | | | | | | |
| Low-Level Input Voltage | $V_{IL}$ | (Note 2) | -0.2 | | +0.3 x $V_{DD}$ | V |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | | 5.5 | V |
| Low-Level Output Current | $I_{OL}$ | $V_{OL}$ = 0.4V | 3 | 30 | | mA |
| | | $V_{OL}$ = 0.6V | 6 | 50 | | |
| Input Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input Capacitance | $C_I$ | All inputs = GND | | 15 | | pF |
| **SELECT INPUTS A2, A1, A0, $\overline{INT0}$–$\overline{INT3}$, $\overline{RESET}$** | | | | | | |
| Low-Level Input Voltage | $V_{IL}$ | (Note 2) | -0.2 | | +0.3 x $V_{DD}$ | V |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{DD}$ | | 5.5 | V |

# 4-Channel I²C Switches/Multiplexer

## ELECRTICAL CHARACTERISTICS (5V SUPPLY) (continued)

($V_{DD}$ = 4.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{DD}$ = 5V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input Capacitance | $C_I$ | All inputs = GND | | 5 | | pF |
| **PASS GATE** | | | | | | |
| Switch On-Resistance | $R_{ON}$ | $V_{DD}$ = 4.5V to 5.5V, $I_O$ = 15 mA, $V_O$ = 0.4V | 4 | 12 | 24 | Ω |
| Switch Output Voltage | $V_{PASS}$ | $V_{I(SW)} = V_{DD}$, $I_O$ = -100µA | 2.6 | 3.6 | 4.5 | V |
| Leakage Current | $I_L$ | | -1 | | +1 | µA |
| Input/Output Capacitance | $C_{IO}$ | All inputs = GND | | 6 | | pF |
| **$\overline{INT}$ OUTPUT** | | | | | | |
| Low-Level Output Current | $I_{OL}$ | $V_{OL}$ = 0.4V | 3 | | | mA |
| High-Level Output Current | $I_{OH}$ | | | | 1 | µA |

## TIMING CHARACTERISTICS (Figure 1)

($V_{DD}$ = 2.3V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Propagation Delay from SDA To SD_ or SCL to SC_ | $t_{pd}$ | (Note 3) | | | 0.3 | ns |
| SCL Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | $f_{SCL}$ = 100kHz | 4.7 | | | µs |
| | | $f_{SCL}$ = 400kHz | 1.3 | | | |
| Hold Time (Repeated) START Condition (after this period, the first clock pulse is generated) | $t_{HD;STA}$ | $f_{SCL}$ = 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ = 400kHz | 0.6 | | | |
| Low Period of the SCL Clock | $t_{LOW}$ | $f_{SCL}$ = 100kHz | 4.7 | | | µs |
| | | $f_{SCL}$ = 400kHz | 1.3 | | | |
| High Period of the SCL Clock | $t_{HIGH}$ | $f_{SCL}$ = 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ = 400kHz | 0.6 | | | |
| Setup Time for a Repeated START Condition | $t_{SU;STA}$ | $f_{SCL}$ = 100kHz | 4.7 | | | µs |
| | | $f_{SCL}$ = 400kHz | 0.6 | | | |
| Setup Time for STOP Condition | $t_{SU;STO}$ | $f_{SCL}$ = 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ = 400kHz | 0.6 | | | |
| Data Hold Time (Note 4) | $t_{HD;DAT}$ | $f_{SCL}$ = 100kHz | 0 | | 3.45 | µs |
| | | $f_{SCL}$ = 400kHz | 0 | | 0.9 | |
| Data Setup Time | $t_{SU;DAT}$ | $f_{SCL}$ = 100kHz | 250 | | | ns |
| | | $f_{SCL}$ = 400kHz | 100 | | | |
| Rise Time of Both SDA and SCL Signals | $t_r$ | $f_{SCL}$ = 100kHz | | | 1000 | ns |
| | | $f_{SCL}$ = 400kHz (Note 5) | 20 + 0.1$C_b$ | | 300 | |

## TIMING CHARACTERISTICS (Figure 1) (continued)

($V_{DD}$ = 2.3V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Fall Time of Both SDA and SCL Signals | $t_f$ | $f_{SCL}$ = 100kHz | | | 300 | ns |
| | | $f_{SCL}$ = 400kHz (Note 5) | 20 + 0.1$C_b$ | | 300 | |
| Capacitive Load for Each Bus Line | $C_b$ | (Note 6) | | | 400 | pF |
| Pulse Width of Spikes Suppressed | $t_{SP}$ | | | | 50 | ns |
| Data Valid Time from High to Low | $t_{VD;DATL}$ | (Note 7) | | | 1 | µs |
| Data Valid Time from Low to High | $t_{VD;DATH}$ | (Note 7) | | | 0.6 | µs |
| Data Valid Acknowledge | $t_{VD;ACK}$ | | | | 1 | µs |
| **$\overline{INT}$ (Figure 2)** | | | | | | |
| $\overline{INT\_}$ to $\overline{INT}$ Active Valid Time | $t_{IV}$ | | | | 4 | µs |
| $\overline{INT\_}$ to $\overline{INT}$ Inactive Delay Time | $t_{IR}$ | | | | 2 | µs |
| Low-Level, Pulse-Width Rejection or $\overline{INT\_}$ Inputs | $t_{W(REJ)L}$ | | 1 | | | µs |
| High-Level, Pulse-Width Rejection or $\overline{INT\_}$ Inputs | $t_{W(REJ)H}$ | | 0.5 | | | µs |
| **$\overline{RESET}$ (Figure 3)** | | | | | | |
| Pulse-Width Low Reset | $t_{WL(RST)}$ | | | 4 | | ns |
| Reset Time (SDA Clear) | $t_{RST}$ | | 500 | | | ns |
| Recovery to Start | $t_{REC;STA}$ | | 0 | | | ns |

**Note 1:** All parameters are production tested at $T_A$ = +25°C and guaranteed by design over the specified temperature range.
**Note 2:** Minimum value is not production tested. Guaranteed by design.
**Note 3:** Pass gate propagation delay is calculated from 20Ω (typ) $R_{ON}$ and the 15pF load capacitance. Not production tested.
**Note 4:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IL}$ of the SCL) in order to bridge the undefined region of SCL's falling edge.
**Note 5:** $C_b$ = total capacitance of one bus line in pF.
**Note 6:** Guaranteed by design.
**Note 7:** Measurements taken with a 1kΩ pullup resistor and 50pF load.

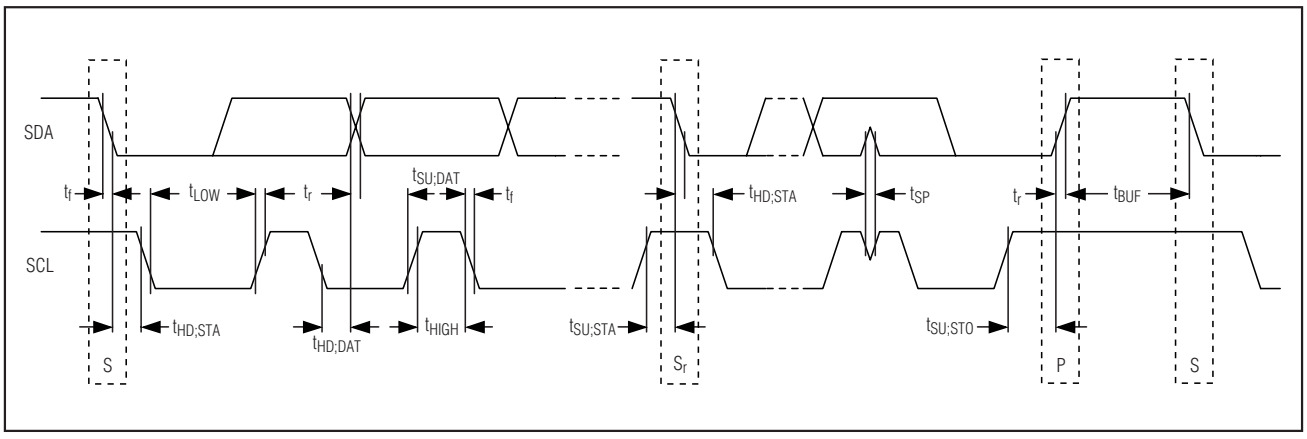



*Figure 1. 2-Wire Serial-Interface Timing Diagram*

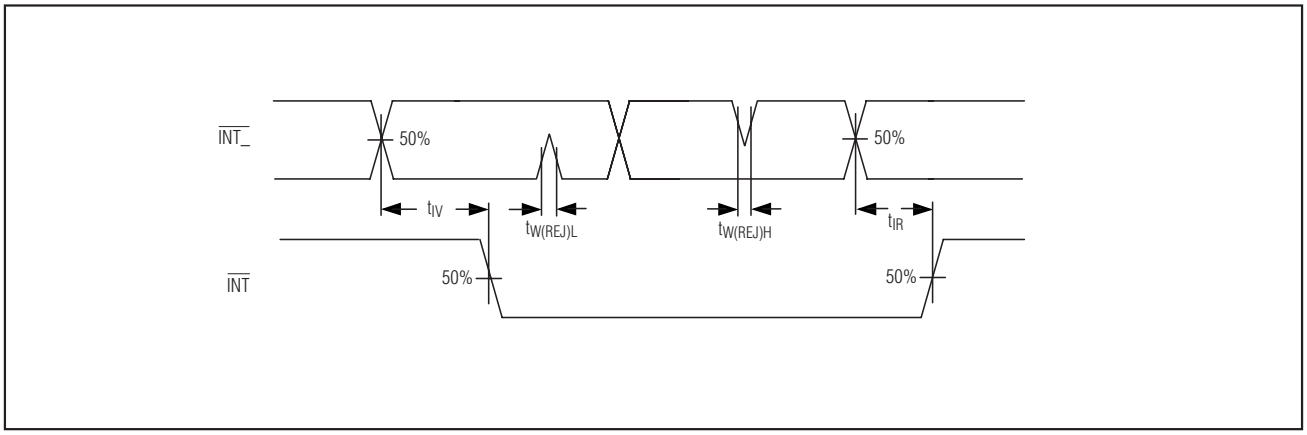



*Figure 2. $\overline{INT}$ Timing Diagram*

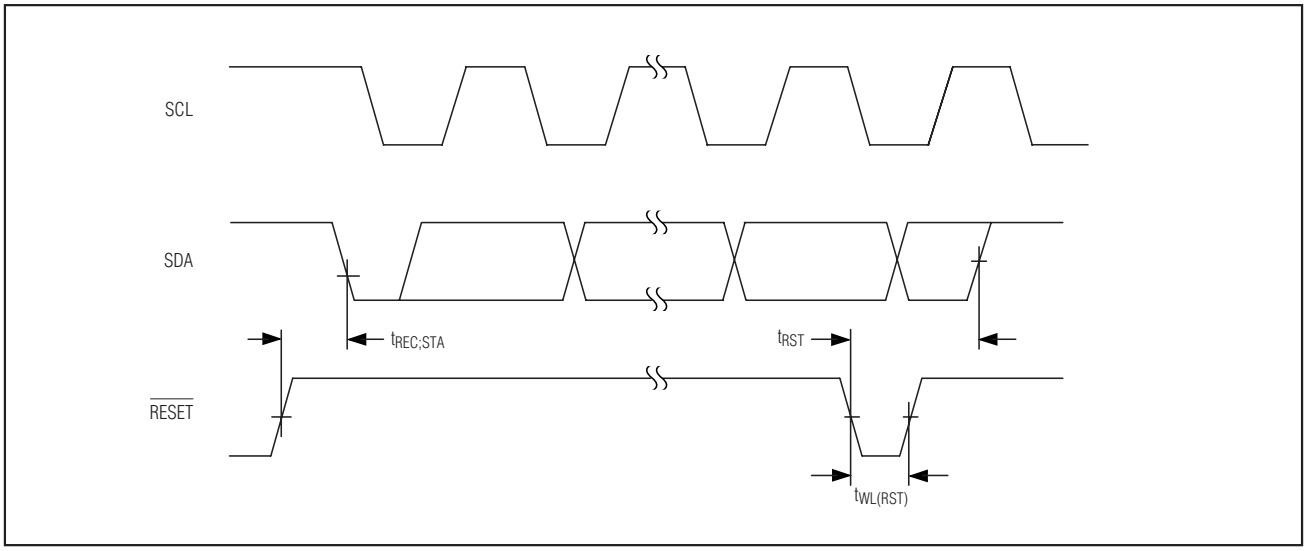


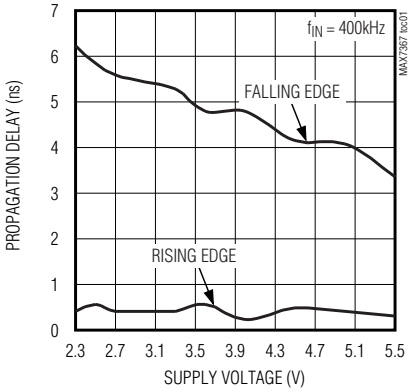

*Figure 3. $\overline{RESET}$ Timing Diagram*

# 4-Channel I²C Switches/Multiplexer

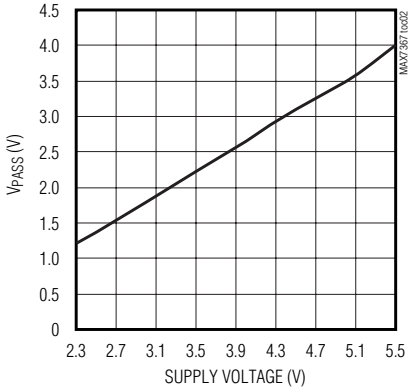
## Typical Operating Characteristics

($V_{DD}$ = +5V, $T_A$ = +25°C, unless otherwise noted.)

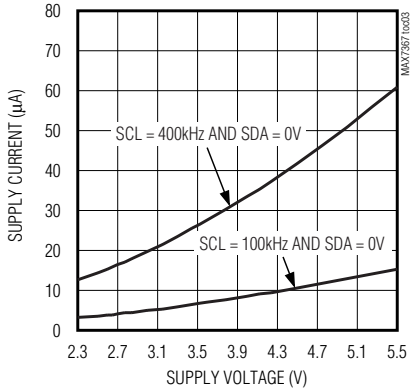
**PROPAGATION DELAY vs. SUPPLY VOLTAGE**



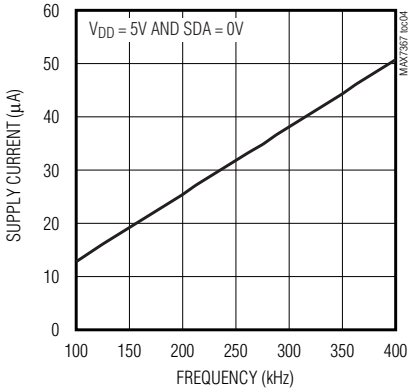

**VPASS VOLTAGE vs. SUPPLY VOLTAGE**




**SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**SUPPLY CURRENT vs. SCL FREQUENCY**



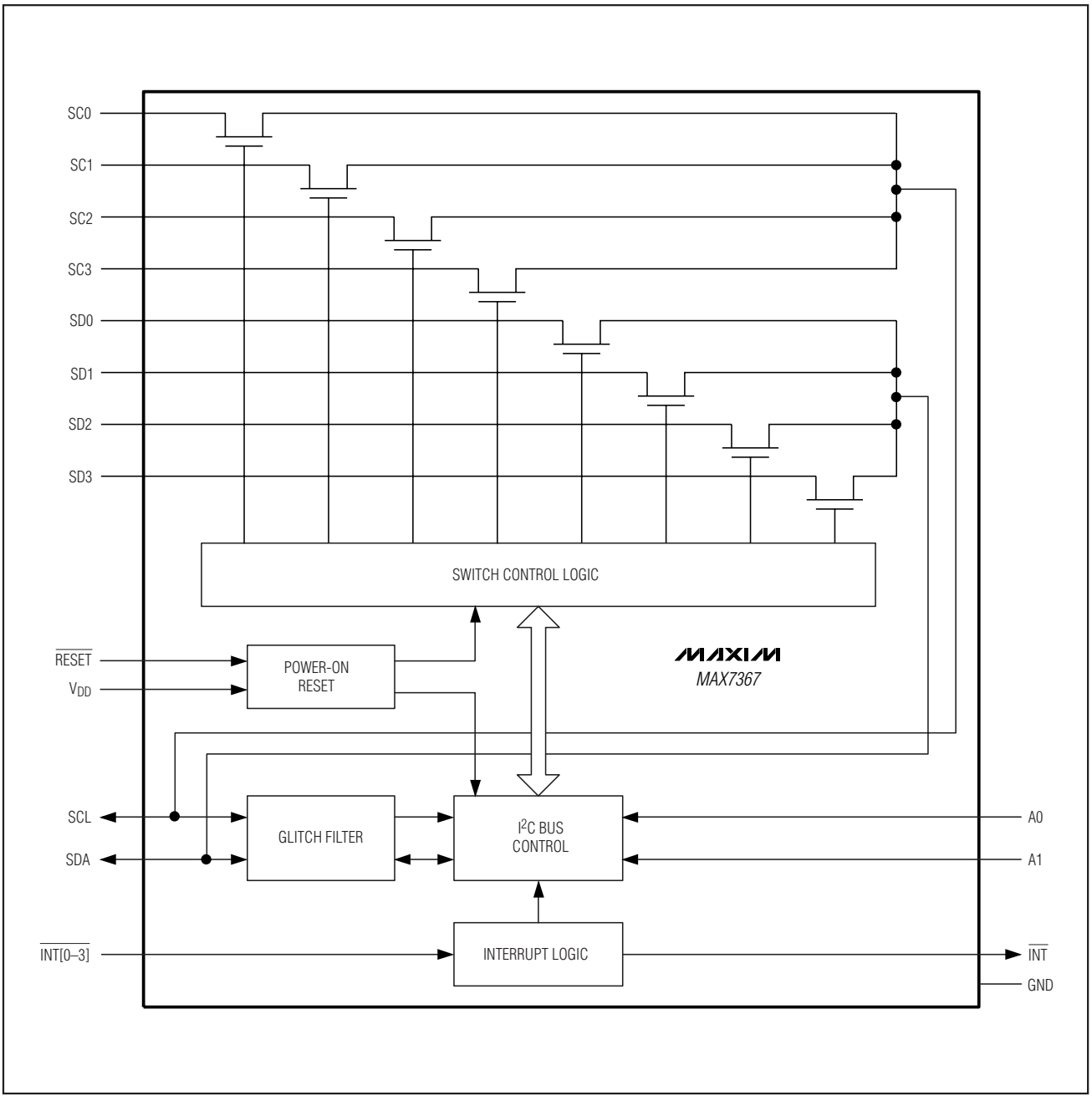
# 4-Channel I²C Switches/Multiplexer

## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX7367 | MAX7368 | MAX7369 | | |
| 1 | 1 | 1 | A0 | Device Address Bit 0 (LSB) |
| 2 | 2 | 2 | A1 | Device Address Bit 1 |
| 3 | 3 | — | $\overline{\text{RESET}}$ | Active-Low Reset Input |
| 4 | — | 4 | $\overline{\text{INT0}}$ | Channel 0 Active-Low Interrupt Input. A logic-low $\overline{\text{INT0}}$ asserts $\overline{\text{INT}}$. If not used, pull up $\overline{\text{INT0}}$ through a resistor to $V_{DD}$. |
| 5 | 4 | 5 | SD0 | Channel 0 Serial Data |
| 6 | 5 | 6 | SC0 | Channel 0 Serial Clock |
| 7 | — | 7 | $\overline{\text{INT1}}$ | Channel 1 Active-Low Interrupt Input. A logic-low $\overline{\text{INT1}}$ asserts $\overline{\text{INT}}$. If not used, pull up $\overline{\text{INT1}}$ through a resistor to $V_{DD}$. |
| 8 | 6 | 8 | SD1 | Channel 1 Serial Data |
| 9 | 7 | 9 | SC1 | Channel 1 Serial Clock |
| 10 | 8 | 10 | GND | Ground |
| 11 | — | 11 | $\overline{\text{INT2}}$ | Channel 2 Active-Low Interrupt Input. A logic-low $\overline{\text{INT2}}$ asserts $\overline{\text{INT}}$. If not used, pull up $\overline{\text{INT2}}$ through a resistor to $V_{DD}$. |
| 12 | 9 | 12 | SD2 | Channel 2 Serial Data |
| 13 | 10 | 13 | SC2 | Channel 2 Serial Clock |
| 14 | — | 14 | $\overline{\text{INT3}}$ | Channel 3 Active-Low Interrupt Input. A logic-low $\overline{\text{INT3}}$ asserts $\overline{\text{INT}}$. If not used, pull up $\overline{\text{INT3}}$ through a resistor to $V_{DD}$. |
| 15 | 11 | 15 | SD3 | Channel 3 Serial Data |
| 16 | 12 | 16 | SC3 | Channel 3 Serial Clock |
| — | 13 | 3 | A2 | Device Address Bit 2 |
| 17 | — | 17 | $\overline{\text{INT}}$ | Active-Low, Open-Drain Interrupt Output. Connect a pullup resistor to $V_{DD}$. |
| 18 | 14 | 18 | SCL | Main Serial Clock |
| 19 | 15 | 19 | SDA | Main Serial Data |
| 20 | 16 | 20 | $V_{DD}$ | Power Supply. Bypass to GND with 0.1µF capacitor. |

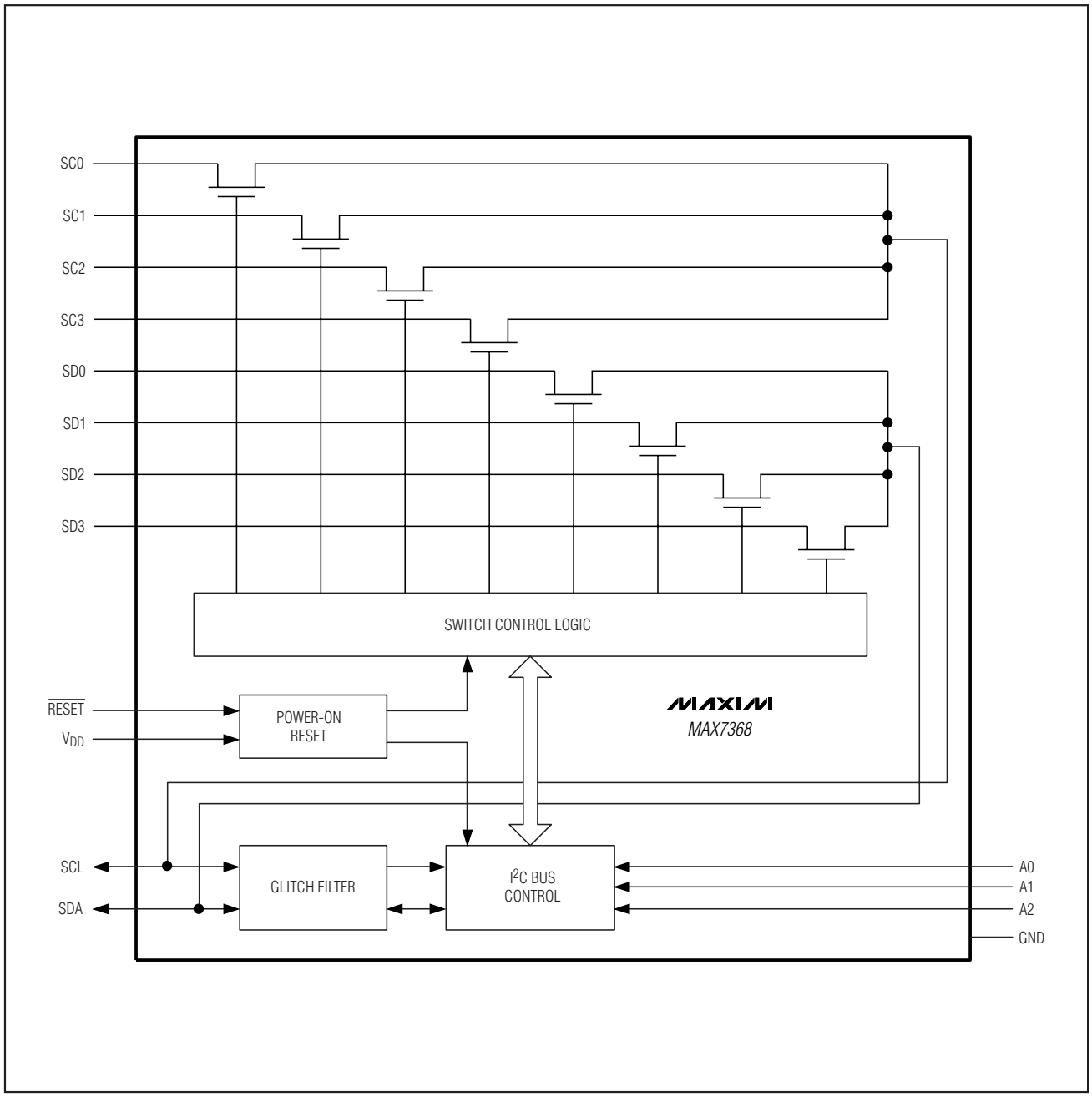
# 4-Channel I²C Switches/Multiplexer

## MAX7367 Functional Diagram



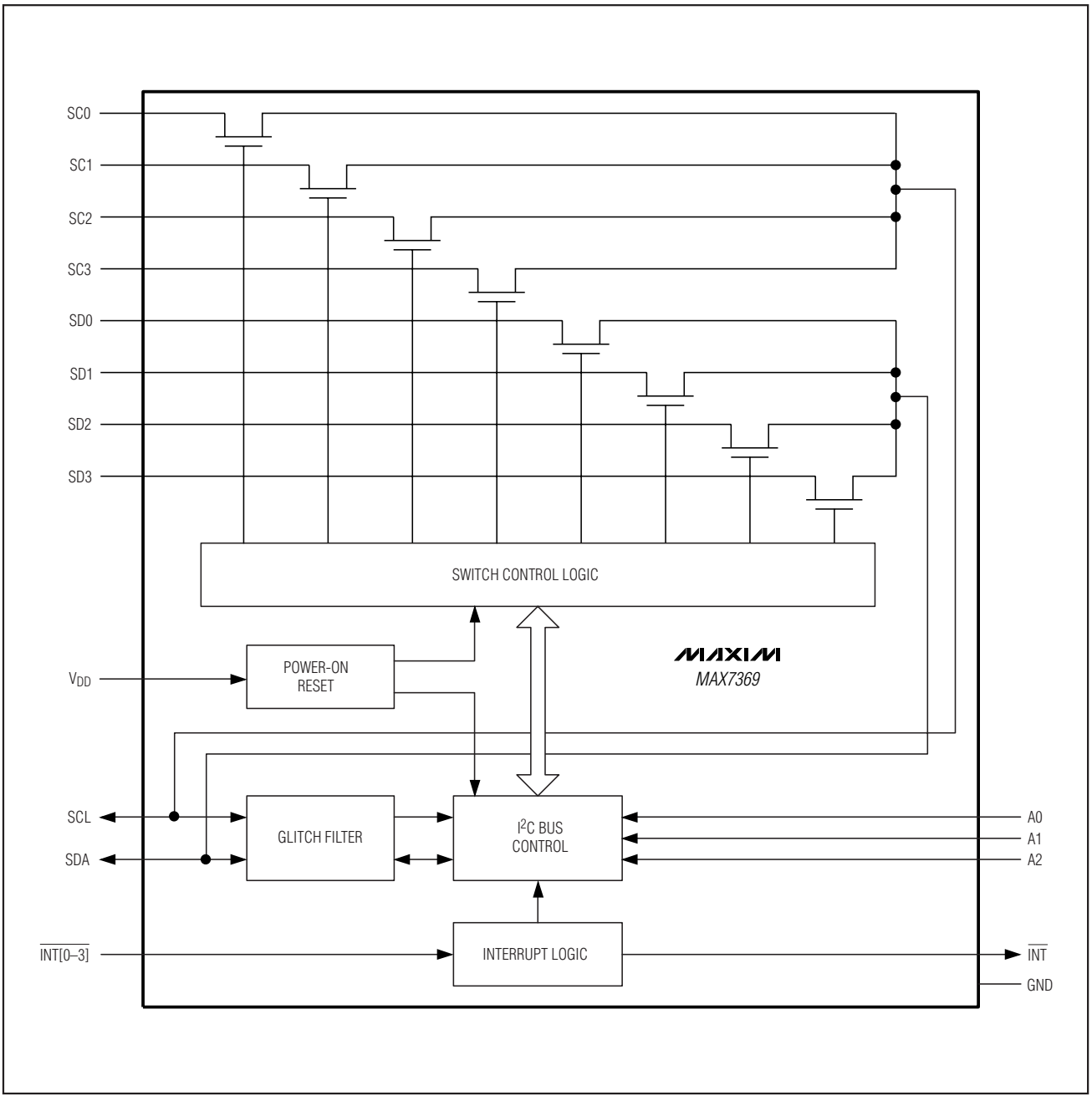
# 4-Channel I²C Switches/Multiplexer

## MAX7368 Functional Diagram



# 4-Channel I²C Switches/Multiplexer

## MAX7369 Functional Diagram



# 4-Channel I²C Switches/Multiplexer

## Detailed Description

The MAX7367/MAX7368/MAX7369 bidirectional, four-channel I²C switches/multiplexer expand the main I²C bus up to four extended buses. The MAX7369 is a 1:4 multiplexer that connects the main I²C bus to one channel at a time. The MAX7367/MAX7368 are four-channel switches that can connect the main I²C bus to one or more channels at a time. These devices isolate bus loading by separating available I²C devices into groups on the channels. The total loading capacitance of the main bus plus those of the connected channel must not exceed 400pF. The extended buses are connected or disconnected through the main I²C bus by writing to the control register of the MAX7367/MAX7368/MAX7369.

Any device connected to an I²C bus can transmit and receive signals. The MAX7367/MAX7368/MAX7369 are transparent to signals sent and received at each channel, allowing multiple masters on the buses. These devices are compatible with the I²C protocol of clock stretch, synchronization, and arbitration in case of multiple masters addressing the bus at the same time. The MAX7367/MAX7368 have a $\overline{\text{RESET}}$ input that allows external circuitry to set the MAX7367/MAX7368 to its default state anytime after the device has powered up. The MAX7367/MAX7369 have interrupt inputs, allowing devices on the extended bus to send an interrupt signal to the master on the main bus.

### Device Address

The MAX7367/MAX7368/MAX7369 have selectable device addresses through external inputs. The MAX7367 slave address consists of 5 fixed bits (A6–A2, set to 11100), followed by 2 pin-programmable bits (A1 and A0), as shown in Figure 4. The MAX7368/MAX7369 slave address consists of 4 fixed bits (A6–A3, set to 1110), followed by 3 pin-programmable bits (A2, A1 and A0), as shown in Figure 5. The most significant address bit (A6) is transmitted first, followed by the remaining bits. The addresses A2 (for MAX7368/MAX7369), A1, and A0 can also be driven dynamically if required, but the values must be stable when they are expected in the address sequence.

### Control/Interrupt Register

There is a control/interrupt register inside the MAX7367/MAX7369 (Figures 6 and 8). There is a control (only) register inside the MAX7368 (Figure 7). Use the main I²C bus to write or read from this register. Following the successful acknowledgement of the slave address, the master bus sends a byte or the master bus receives a byte from/to the MAX7367/MAX7368/MAX7369. The last 3 bits (for the MAX7369) or 4 bits (for the MAX7367/MAX7368) of the byte are stored in the control/interrupt register (B0 to B2 or B0 to B3) for channel selection. If multiple bytes are received, only the last byte received is saved. The first four bits of the register represent the interrupt condition (for the MAX7367/MAX7369 only).

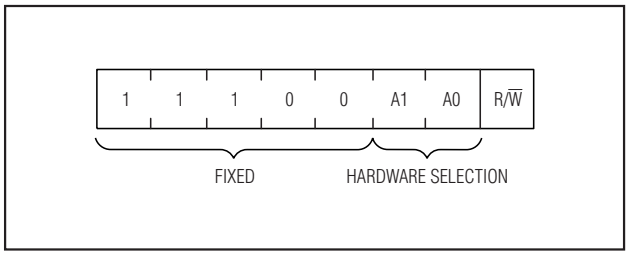



*Figure 4. MAX7367 Slave Address*

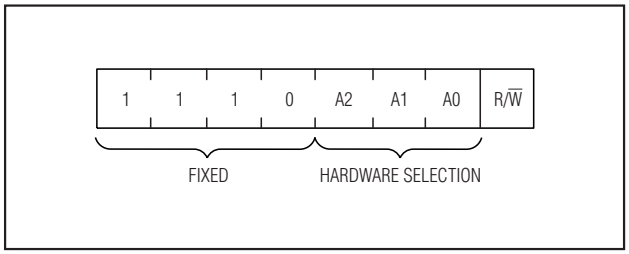



*Figure 5. MAX7368/MAX7369 Slave Address*

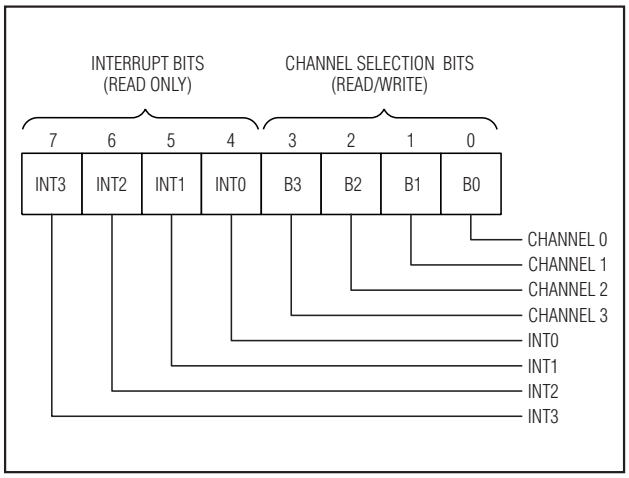



*Figure 6. MAX7367 Control/Interrupt Register*

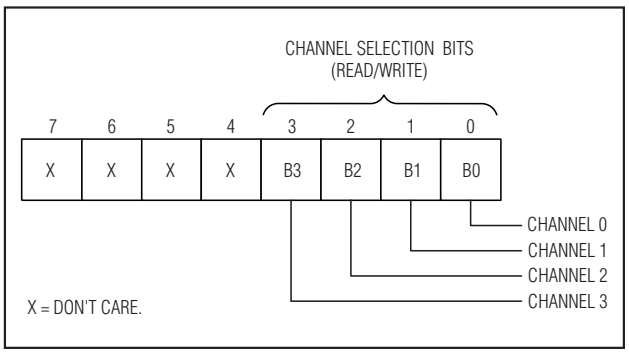



*Figure 7. MAX7368 Control Register*

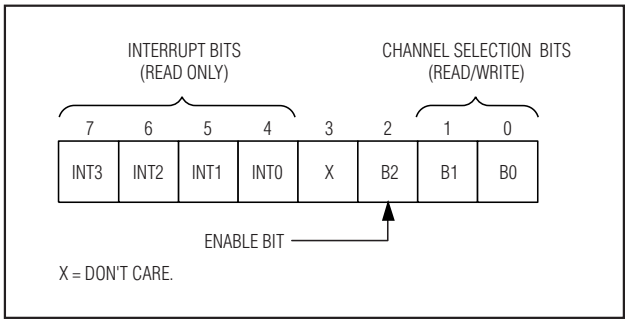



*Figure 8. MAX7369 Control/Interrupt Register*

### *Channel Selection*

Each channel selected contains an SD_ and SC_ pair. Select a channel by writing a control byte after a successful acknowledge of the slave address. The last 4 bits of the control byte determine which channel(s) is selected for the MAX7367/MAX7368 as shown in Table 1. The last 3 bits of the control byte determine which channel is selected for the MAX7369 as shown in Table 2. The selected channels are activated after the stop condition. When a channel is selected, the respective SD_/SC_ pair is logic-high, ensuring no false conditions occur on the bus.

### *Interrupt Logic (MAX7367/MAX7369)*

The MAX7367/MAX7369 have four interrupt inputs, one for each channel, and one $\overline{INT}$ output. The $\overline{INT}$ output is an open-drain output that requires a pullup resistor. The $\overline{INT}$ output is asserted by a low-logic signal on any of the $\overline{INT\_}$ inputs, and it is deasserted only when all the $\overline{INT\_}$ inputs are logic-high. Bits 4–7 of the MAX7367/MAX7369 control/interrupt register store the state of the $\overline{INT\_}$ for each channel as shown in Table 3 and Figures 6 and 8. The logic level of $\overline{INT\_}$ is not latched. Drive the respective $\overline{INT\_}$ input high to remove the interrupt condition for the channel. An interrupt can occur on any channel, regardless of whether it is selected or not selected.

After a device generates an interrupt on one of the channels, the interrupt input is loaded into the control/interrupt register when a read is performed. To determine which device is generating the interrupt, read the contents of the control/interrupt register to determine which channel is issuing the interrupt, then write the appropriate command to the control/interrupt register to select the interrupted channel. Read from all devices on the interrupted channel to determine the exact source of the interrupt.

## Table 1. MAX7367/MAX7368 Control Bits for Channel Selection

| CONTROL BIT | COMMAND |
|---|---|
| B0 | 0 = Channel 0 disabled (default)<br>1 = Channel 0 enabled |
| B1 | 0 = Channel 1 disabled (default)<br>1 = Channel 1 enabled |
| B2 | 0 = Channel 2 disabled (default)<br>1 = Channel 2 enabled |
| B3 | 0 = Channel 3 disabled (default)<br>1 = Channel 3 enabled |

## Table 2. MAX7369 Control Bits for Channel Selection

| B2 | B1 | B0 | COMMAND |
|---|---|---|---|
| 0 | 0 | 0 | No channel selected (default) |
| 0 | X | X | No channel selected |
| 1 | 0 | 0 | Channel 0 selected |
| 1 | 0 | 1 | Channel 1 selected |
| 1 | 1 | 0 | Channel 2 selected |
| 1 | 1 | 1 | Channel 3 selected |

## Table 3. MAX7367/MAX7369 Interrupt Indicator Bits

| INTERRUPT BIT | STATE |
|---|---|
| INT0 | 0 = No channel 0 interrupt (default)<br>1 = Channel 0 interrupt |
| INT1 | 0 = No channel 1 interrupt (default)<br>1 = Channel 1 interrupt |
| INT2 | 0 = No channel 2 interrupt (default)<br>1 = Channel 2 interrupt |
| INT3 | 0 = No channel 3 interrupt (default)<br>1 = Channel 3 interrupt |

# 4-Channel I²C Switches/Multiplexer

### $\overline{\text{RESET}}$ Input (MAX7367/MAX7368)

The MAX7367/MAX7368 feature an active-low $\overline{\text{RESET}}$ input. When $\overline{\text{RESET}}$ is driven low for more than 4ns, the MAX7367/MAX7368 reset the internal register and I²C state machine to their default states, allowing a master to recover from a bus fault condition.

### Power-On Reset (POR)

When power is applied to $V_{DD}$, internal POR circuitry holds the MAX7367/MAX7368/MAX7369 in a reset state until $V_{DD}$ has reached the $V_{POR}$ threshold. At this point, the reset condition is released, and the MAX7367/MAX7368/MAX7369 register and I²C state machine are initialized to their default states (all zeroes), causing all the channels to be deselected.

### Voltage Translation

The MAX7367/MAX7368/MAX7369 can be used as a voltage translator from the main bus to the extended buses. The output voltage ($V_{PASS}$) is limited by the supply voltage ($V_{DD}$) (see the *Typical Operation Characteristics*). For the MAX7367/MAX7368/MAX7369 to be used as a voltage translator, the $V_{PASS}$ voltage should be lower than or equal to the lowest bus voltage.

### I²C Interface

The MAX7367/MAX7368/MAX7369 feature an I²C-compatible, 2-wire serial interface consisting of a bidirectional serial-data line (SDA) and a serial-clock line (SCL). The master (typically a microcontroller) initiates data transfer on the bus and generates the SCL.

### Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 9).

### Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 10).

### Acknowledge Bit

Successful data transfers are acknowledged with an acknowledge bit (A) or a not-acknowledge bit (NA). Both the master and the MAX7367/MAX7368/MAX7369 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 11). In the case of an unsuccessful data transfer, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

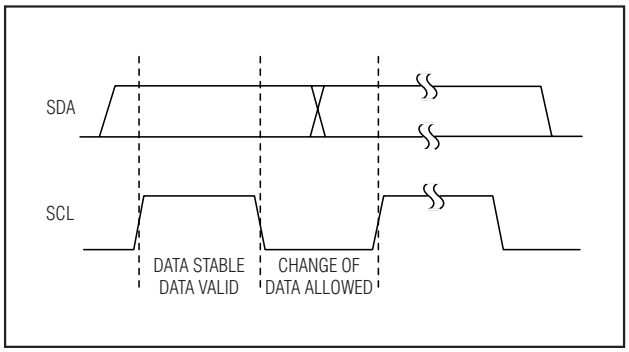



*Figure 9. Bit Transfer*

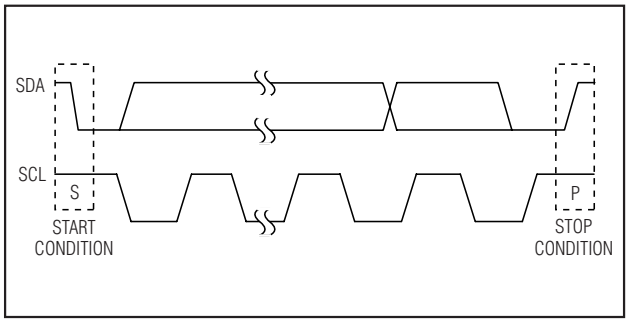



*Figure 10. Start and Stop Conditions*

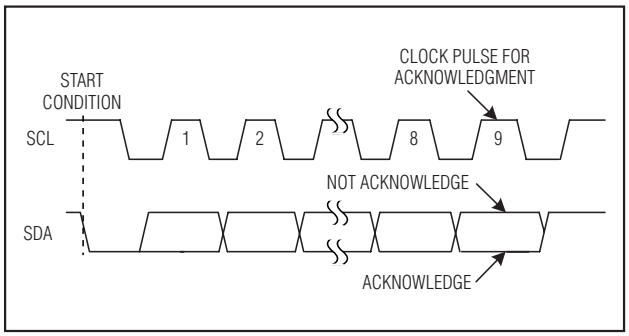



*Figure 11. Acknowledge*

### Serial Addressing

A master initiates communication with a slave device by issuing a START condition followed by a slave address byte. The slave address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). When idle, the MAX7367/MAX7368/MAX7369 continuously wait for a START condition followed by its slave address. After recognizing a start condition followed by the correct address, the MAX7367/MAX7368/MAX7369 are ready to accept or send data. The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX7367/MAX7368/MAX7369 (R/$\overline{W}$ = 0 selects a write command, R/$\overline{W}$ = 1 selects a read command as shown in Figures 12 and 13). After receiving the proper address, the MAX7367/MAX7368/MAX7369 (slave) issue an ACK by pulling SDA low for one clock cycle.

## Applications Information

### Repeated Slave Addresses

The MAX7367/MAX7368/MAX7369 allow systems to reuse slave addresses individually on each channel of the extended bus. To reuse slave addresses on the extended bus channels of the MAX7367/MAX7368, ensure no more than one channel with a reused address is selected at the same time.

### Power-Supply Considerations

The MAX7367/MAX7368/MAX7369 operate from a +2.3V to +5.5V power-supply voltage. Good power-supply decoupling is needed to maintain the performance of these parts. Bypass $V_{DD}$ to GND with a 0.1µF surface-mount ceramic capacitor. Mount the bypass capacitor as close as possible to the device.

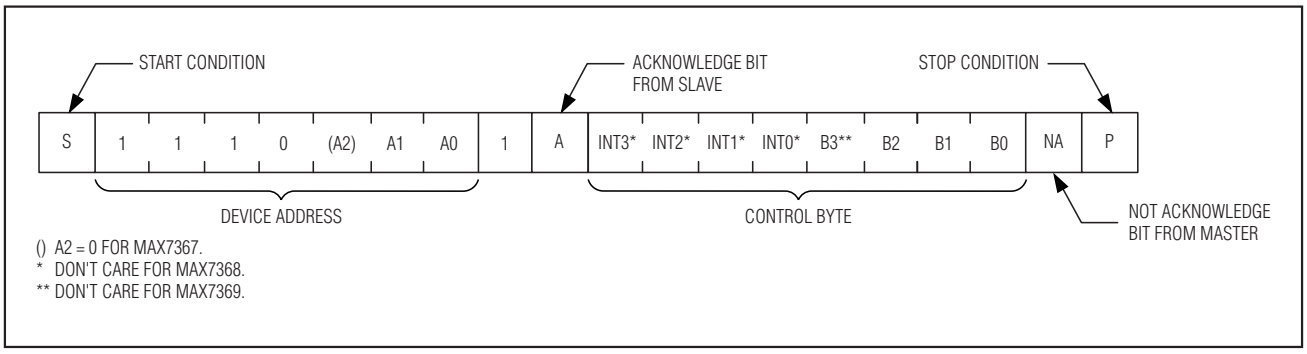



*Figure 12. Read Command*

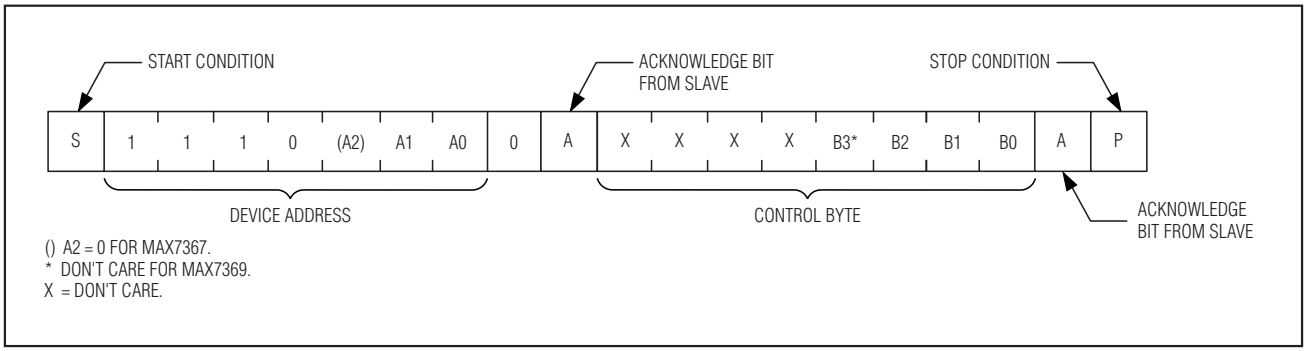



*Figure 13. Write Command*

# 4-Channel I²C Switches/Multiplexer

### Choosing Pullup Resistors

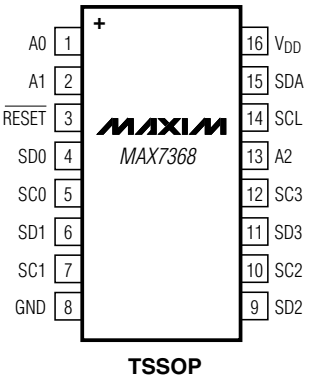
I²C requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for a data rate of 400kbps (refer to I²C specifications for details). In order to meet the rise time requirement, choose the pullup resistors such that the rise time ($t_R$ = $0.85R_{PULLUP} \times C_{BUS}$) is less than 300ns. For a bus capacitance of 400pF, choose a pullup resistor less than 880Ω. Often I²C devices work when the maximum specified rise time is exceeded. However, if the rise times become too slow, the devices on the bus do not recognize the command signals. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines and also minimize crosstalk and undershoot of the bus signals.

## Chip Information

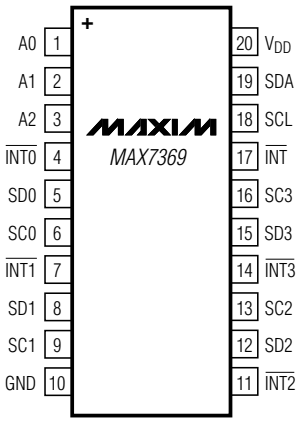
PROCESS: BiCMOS

## Pin Configurations (continued)

TOP VIEW



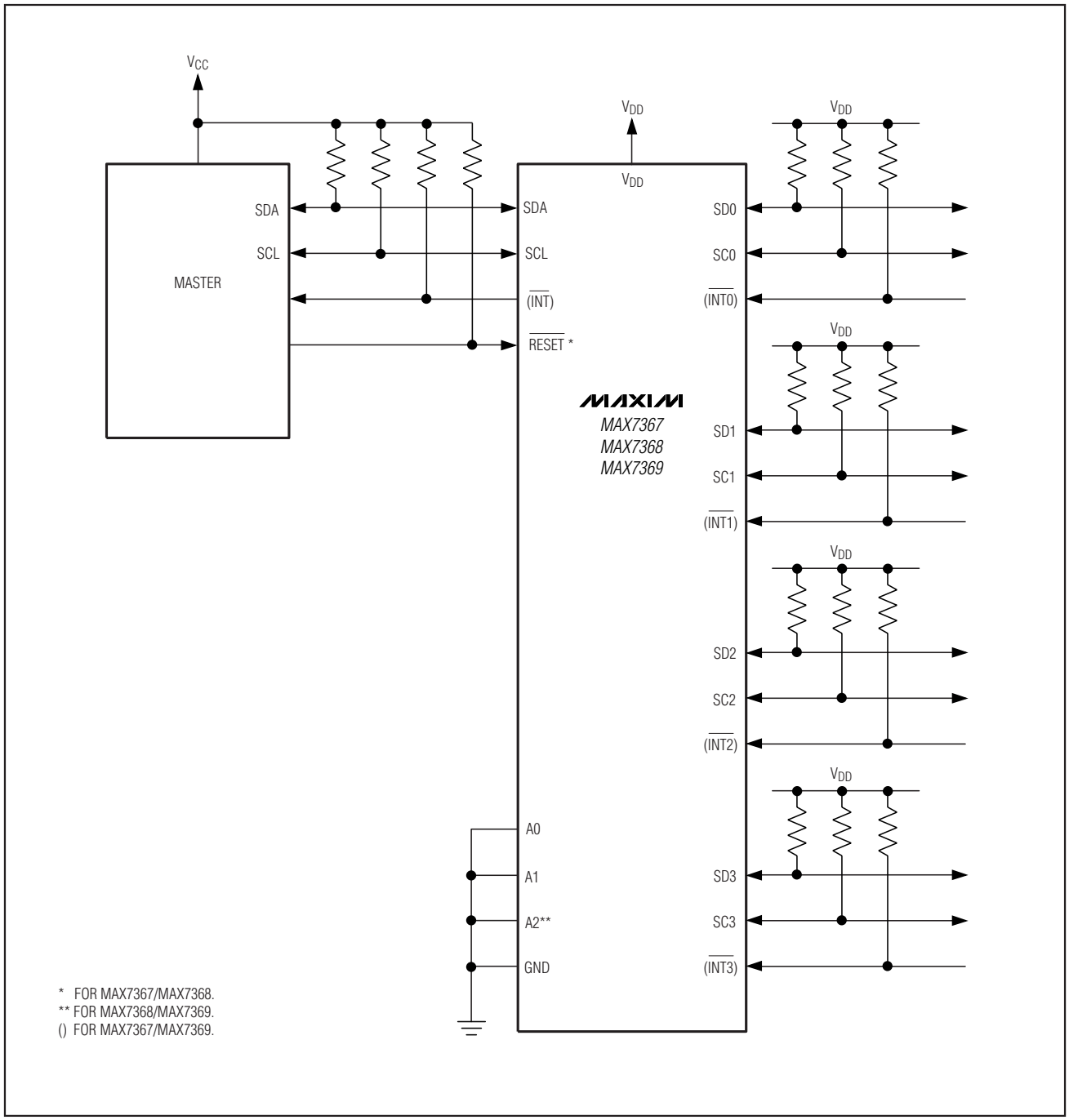

TSSOP




TSSOP

# 4-Channel I²C Switches/Multiplexer

## Typical Operating Circuit



# 4-Channel I²C Switches/Multiplexer

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 20 TSSOP | U20-3 | 21-0066 |
| 16 TSSOP | U16-1 | 21-0066 |

# 4-Channel I²C Switches/Multiplexer

## Revision History

| REVISION | REVISION | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/06 | Initial release of the MAX7369 | — |
| 1 | 12/06 | Initial release of the MAX7367/MAX7368 | 1 |
| 2 | 2/09 | Changed the minimum $V_{IL}$ spec | 2–5 |