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**SN74F1056**  
**8-BIT SCHOTTKY BARRIER DIODE**  
**BUS-TERMINATION ARRAY**

SDFS085A – AUGUST 1992 – REVISED JULY 1997

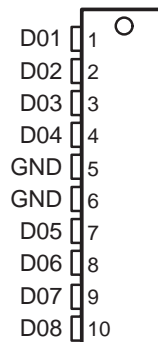
- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current 300 mA
- 8-Bit Array Structure Suited for Bus-Oriented Systems

**description**

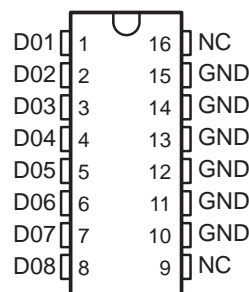
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74F1056 is characterized for operation from 0°C to 70°C.

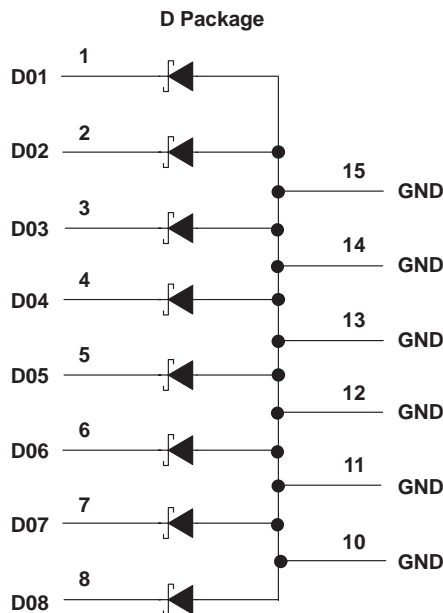
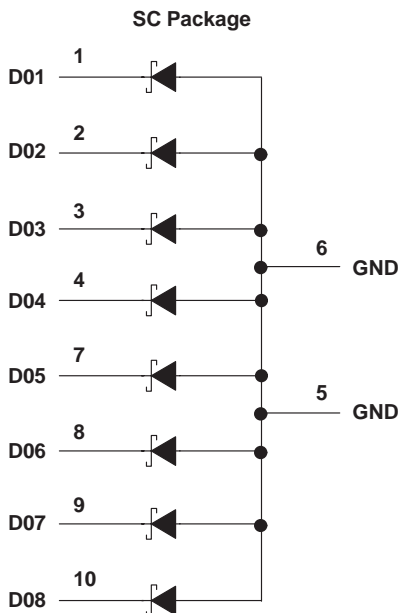
**SC PACKAGE**  
**(TOP VIEW)**



**D PACKAGE**  
**(TOP VIEW)**



**schematic diagrams**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Steady-state reverse voltage, $V_R$	7 V
Continuous forward current, $I_F$ : Any D terminal from GND	50 mA
Total through all GND terminals	170 mA
Repetitive peak forward current, $I_{FRM}$ (see Note 1): Any D terminal from GND	300 mA
Total through all GND terminals	1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These values apply for  $t_W \leq 100 \mu s$ , duty cycle  $\leq 20\%$ .

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

**single-diode operation (see Note 2)**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_R$ Static reverse current	$V_R = 7 V$			2	$\mu A$
$V_F$ Static forward voltage	$I_F = 18 mA$		0.8	1	V
	$I_F = 50 mA$		1	1.2	
$V_{FM}$ Peak forward voltage	$I_F = 200 mA$		1.23		V
$C_t$ Total capacitance	$V_R = 0,$ $f = 1 MHz$		3	3.75	pF
	$V_R = 2 V,$ $f = 1 MHz$		2.5	3	

‡ All typical values are at  $T_A = 25^\circ C$ .

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

**multiple-diode operation**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_x$ Internal crosstalk current	Total GND current = 1.2 A, See Note 3		10	50	$\mu A$

‡ All typical values are at  $T_A = 25^\circ C$ .

NOTE 3:  $I_x$  is measured under the following conditions with one diode static, all others switching:  
 Switching diodes:  $t_W = 100 \mu s$ , duty cycle = 20%  
 Static diode:  $V_R = 5 V$   
 The static diode input current is the internal crosstalk current  $I_x$ .

**switching characteristics,  $T_A = 25^\circ C$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$ Reverse recovery time	$I_F = 10 mA,$ $I_{RM(REC)} = 10 mA,$ $I_{R(REC)} = 1 mA,$ $R_L = 100 \Omega$		5	7	ns

**undershoot characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{US}$ Undershoot voltage	$t_f = 2 ns,$ $t_W = 50 ns,$ $V_{IH} = 5 V,$ $V_{IL} = 0,$ $Z_S = 25 \Omega,$ $Z_O = 50 \Omega,$ $L = 36\text{-inch coax}$		0.6	0.7	V

**SN74F1056**  
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**APPLICATION INFORMATION**

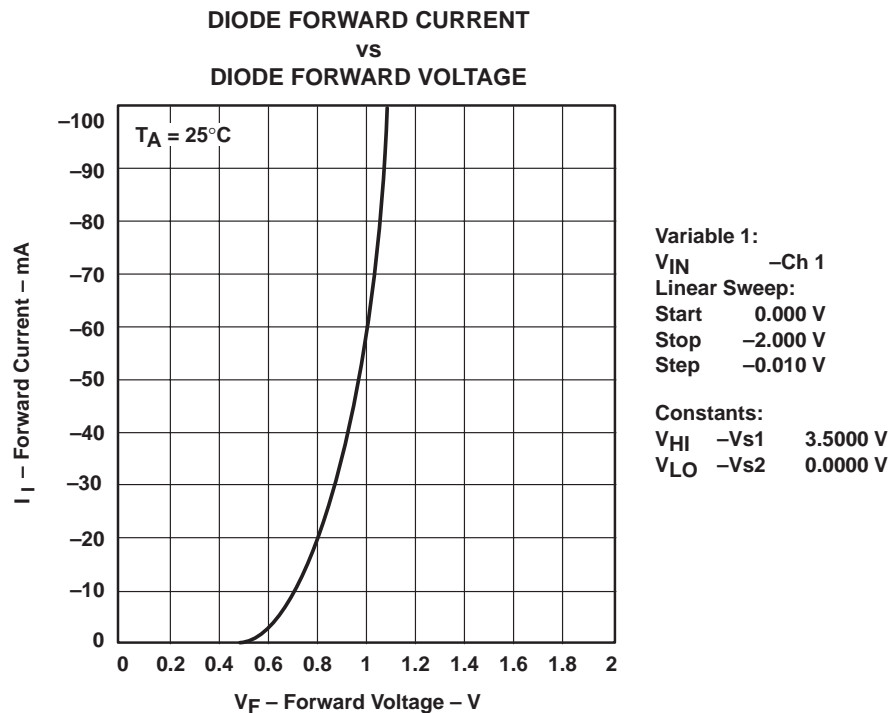
Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1056 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current versus voltage plot for the SN74F1056 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 2(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes also can be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.



**Figure 1. Current Versus Voltage for the SN74F1056**

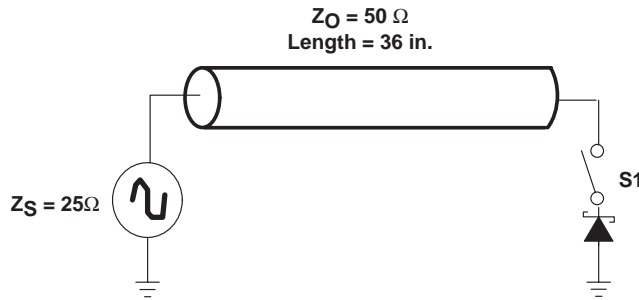
**SN74F1056**

**8-BIT SCHOTTKY BARRIER DIODE**

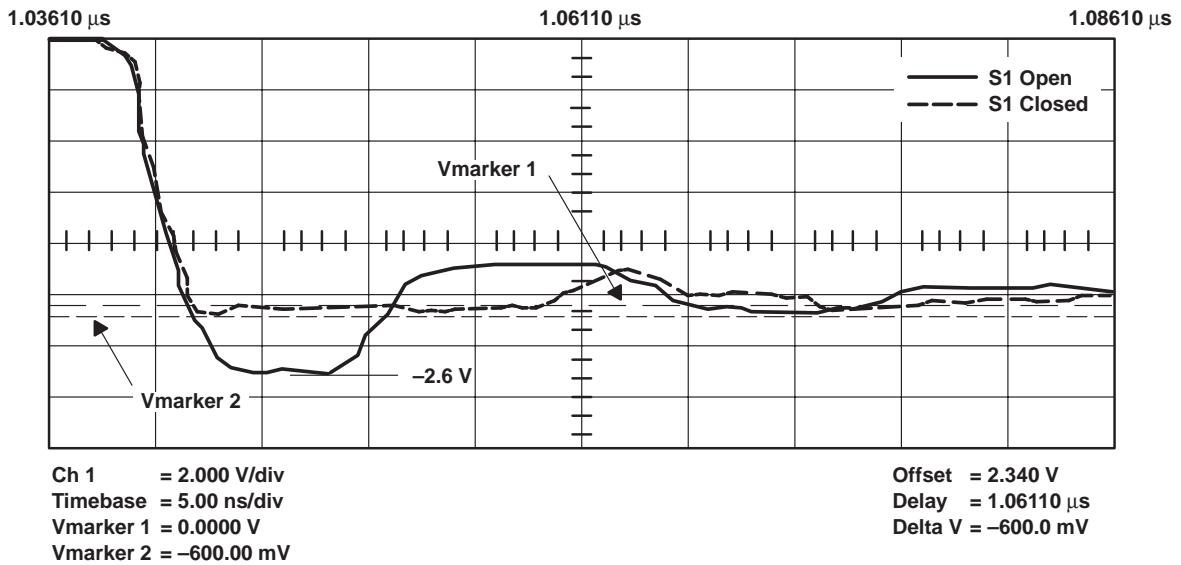
**BUS-TERMINATION ARRAY**

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**APPLICATION INFORMATION**



(a) UNDERSHOOT TEST SETUP



(b) OSCILLOSCOPE DISPLAY

**Figure 2. Undershoot Test Setup and Oscilloscope Display**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F1056D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F1056	<a href="#">Samples</a>
SN74F1056DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F1056	<a href="#">Samples</a>
SN74F1056DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F1056	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Datasheet of SN74F1056D - IC ARRAY BUS-TERM 8BIT 16-SOIC

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**PACKAGE OPTION ADDENDUM**

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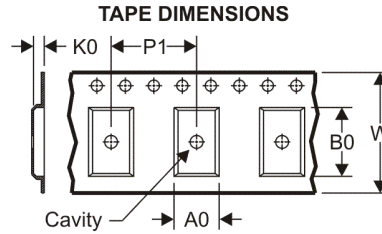
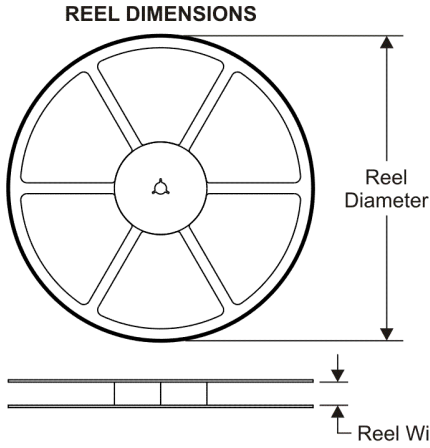
10-Jun-2014

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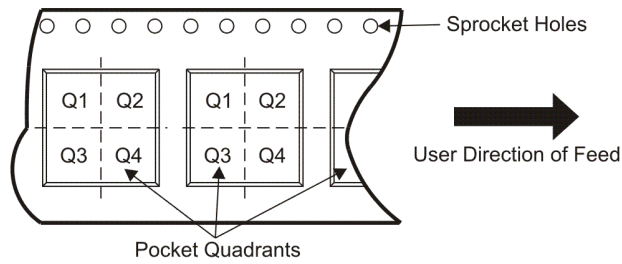
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**TAPE AND REEL INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

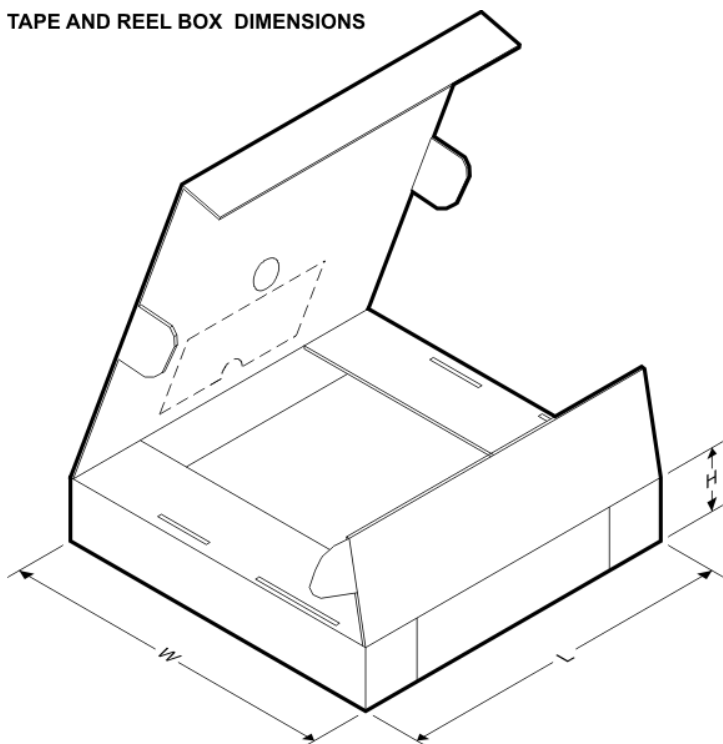


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F1056DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



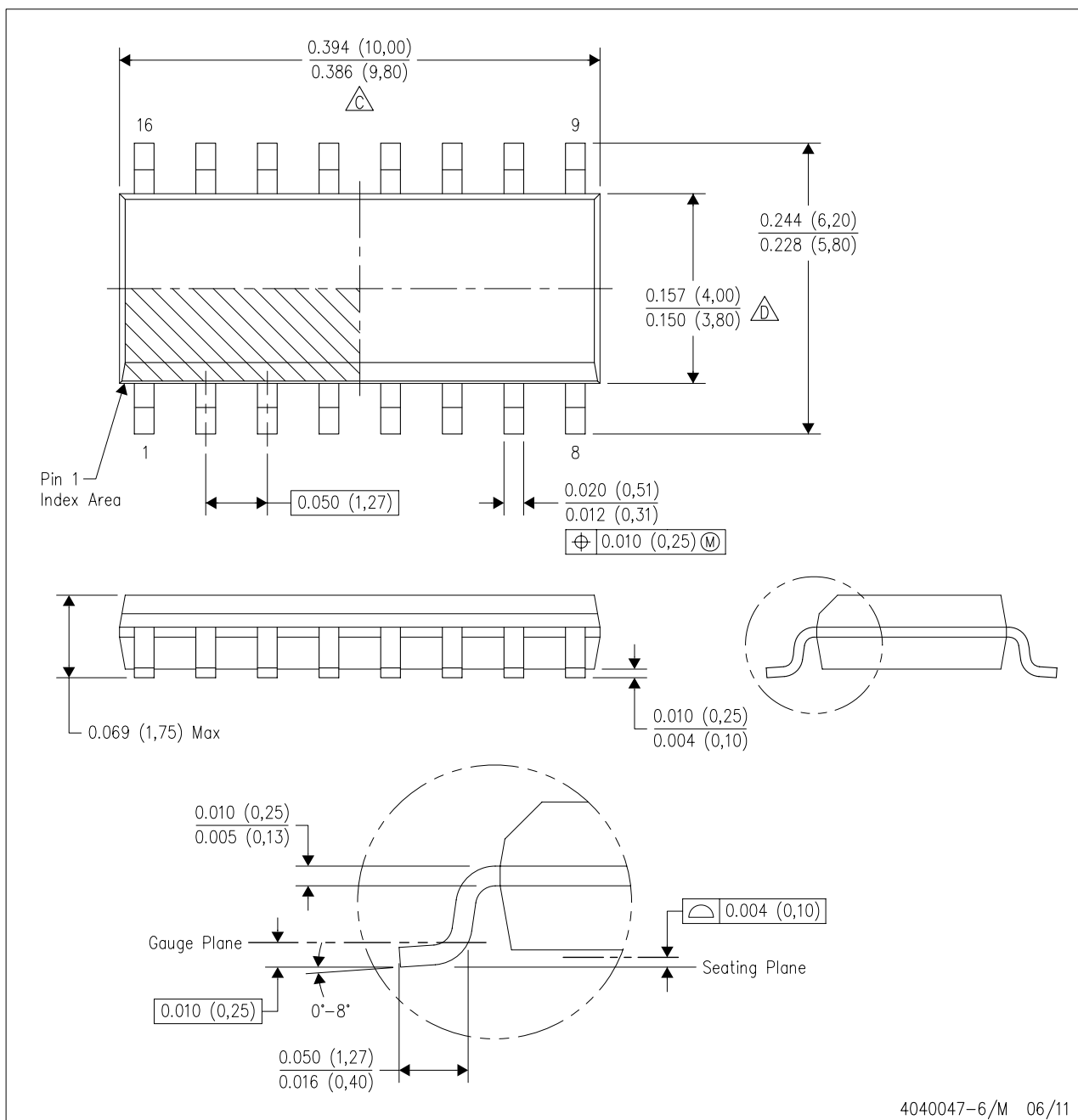
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F1056DR	SOIC	D	16	2500	333.2	345.9	28.6

**MECHANICAL DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



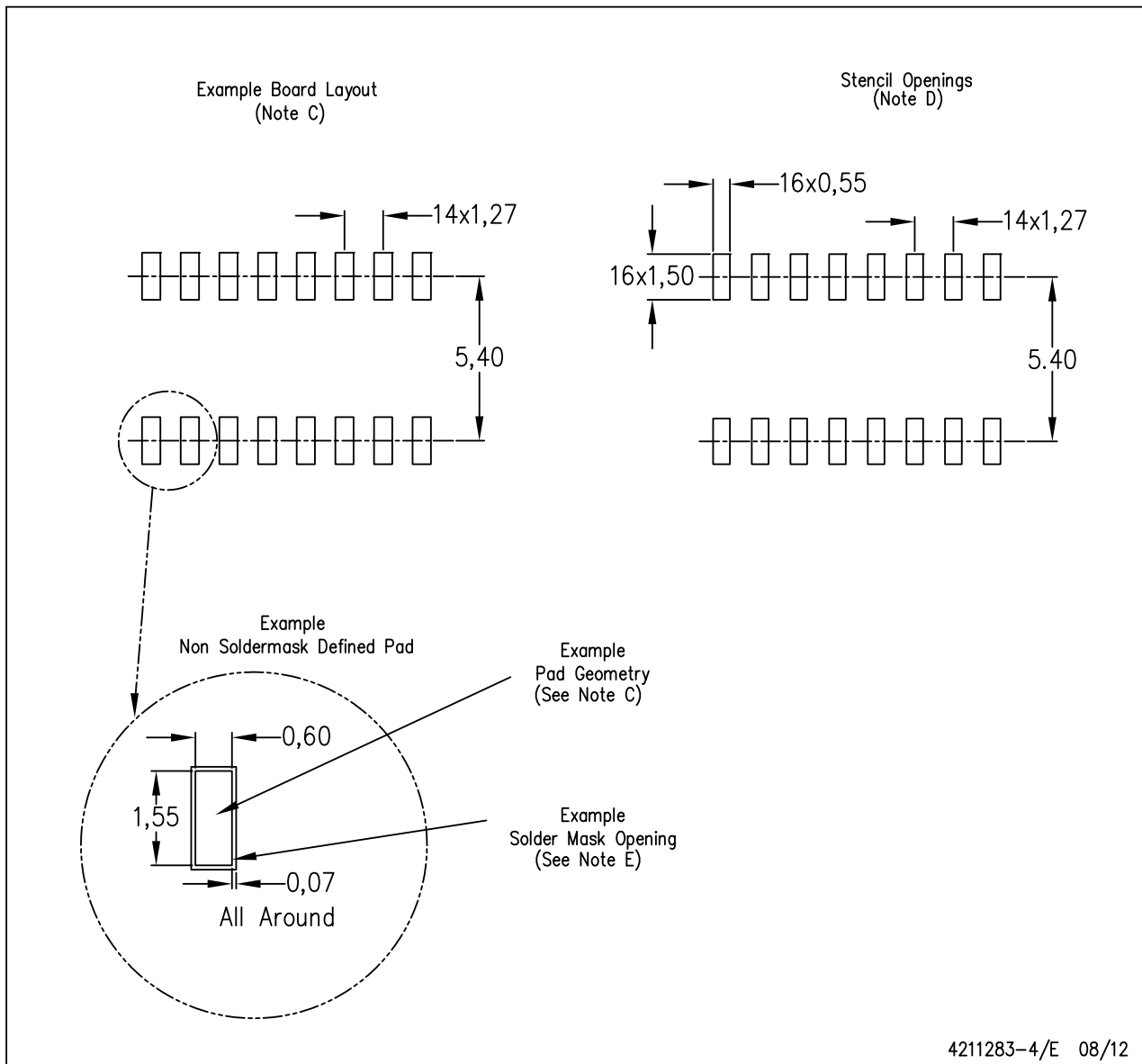
4040047-6/M 06/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - Reference JEDEC MS-012 variation AC.

**LAND PATTERN DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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