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SN64BCT245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCBS040A – JANUARY 1990 – REVISED JANUARY 1994

- BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State True Outputs Drive Bus Lines Directly
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

description

This octal bus transceiver is designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

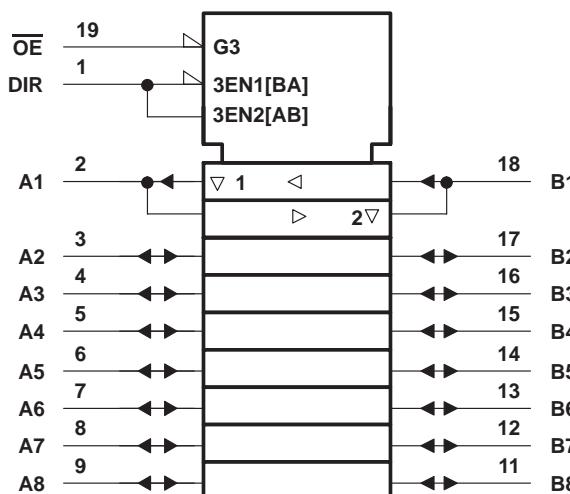
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT245 is characterized for operation from -40°C to 85°C and 0°C to 70°C .

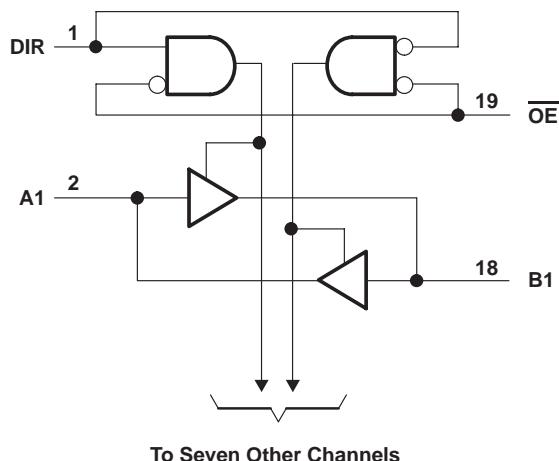
FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	– 40°C to 85°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current	A1 – A8		–3	mA
		B1 – B8		–15	
I_{OL}	Low-level output current	A1 – A8		24	mA
		B1 – B8		64	
T_A	Operating free-air temperature	–40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYPT [†]	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA						-1.2	V
V _{OH}	Any A	V _{CC} = 4.5 V	I _{OH} = -1 mA			2.5	3.4		V
	Any A or B		I _{OH} = -3 mA			2.4	3.3		
	Any B		I _{OH} = -15 mA			2	3.1		
V _{OL}	Any A	V _{CC} = 4.5 V	I _{OL} = 24 mA			0.35	0.5		V
	Any B		I _{OL} = 64 mA			0.42	0.55		
I _{OZ}	Power up	V _{CC} = 0 to 2.3 V	V _O = 2.7 V	OE at 0.8 V			70		μA
			V _O = 0.5 V				-0.65		mA
	Power down	V _{CC} = 1.8 V to 0	V _O = 2.7 V	OE at 0.8 V			70		μA
			V _O = 0.5 V				-0.65		mA
I _I [‡]	A and B	V _{CC} = 5.5 V, DIR and OE	V _I = 5.5 V				1		mA
							0.1		
I _{IH} [‡]	A and B	V _{CC} = 5.5 V, DIR and OE	V _I = 2.7 V				70		μA
							20		
I _{IL}	A and B	V _{CC} = 5.5 V, DIR and OE	V _I = 0.5 V				-0.65		mA
							-1.2		
I _{OS} [§]	Any A	V _{CC} = 5.5 V, Any B	V _O = 0			-60	-150		mA
						-100	-225		
I _{CCH}	A-to-B	V _{CC} = 5.5 V				36	57		mA
I _{CCL}	A-to-B	V _{CC} = 5.5 V				57	90		
I _{CCZ}		V _{CC} = 5.5 V				10	15		
C _i	OE and DIR	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V				7			pF
C _{io}	A to B	V _{CC} = 5 V, B to A	V _I = 2.5 V or 0.5 V			9			pF
						12			

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT	
				T _A = -40°C to 85°C		T _A = 0°C to 70°C			
				MIN	MAX	MIN	MAX		
t _{PLH}	A or B	B or A	1.5	1	6	1.5	7.2	1	ns
				6.6		7.6		7	
t _{PHL}	OE	A or B	1.5	1.5	9.4	1.5	11.2	1.5	ns
				10.2		11.8		10.9	
t _{PZH}	OE	A or B	1.5	1.5	8.3	1.5	9.7	1.5	ns
				7.8		9.6		9.3	
t _{PZL}	OE	A or B	1.5	1.5	10.2	1.5	11.8	1.5	ns
				11.6				11.6	
t _{PHZ}	OE	A or B	1.5	1.5	7.8	1.5	9.6	1.5	ns
				9.1				9.1	
t _{PLZ}	OE	A or B	1.5	1.5	10.2	1.5	11.8	1.5	ns
				11.6				11.6	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN64BCT245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT245	Samples
SN64BCT245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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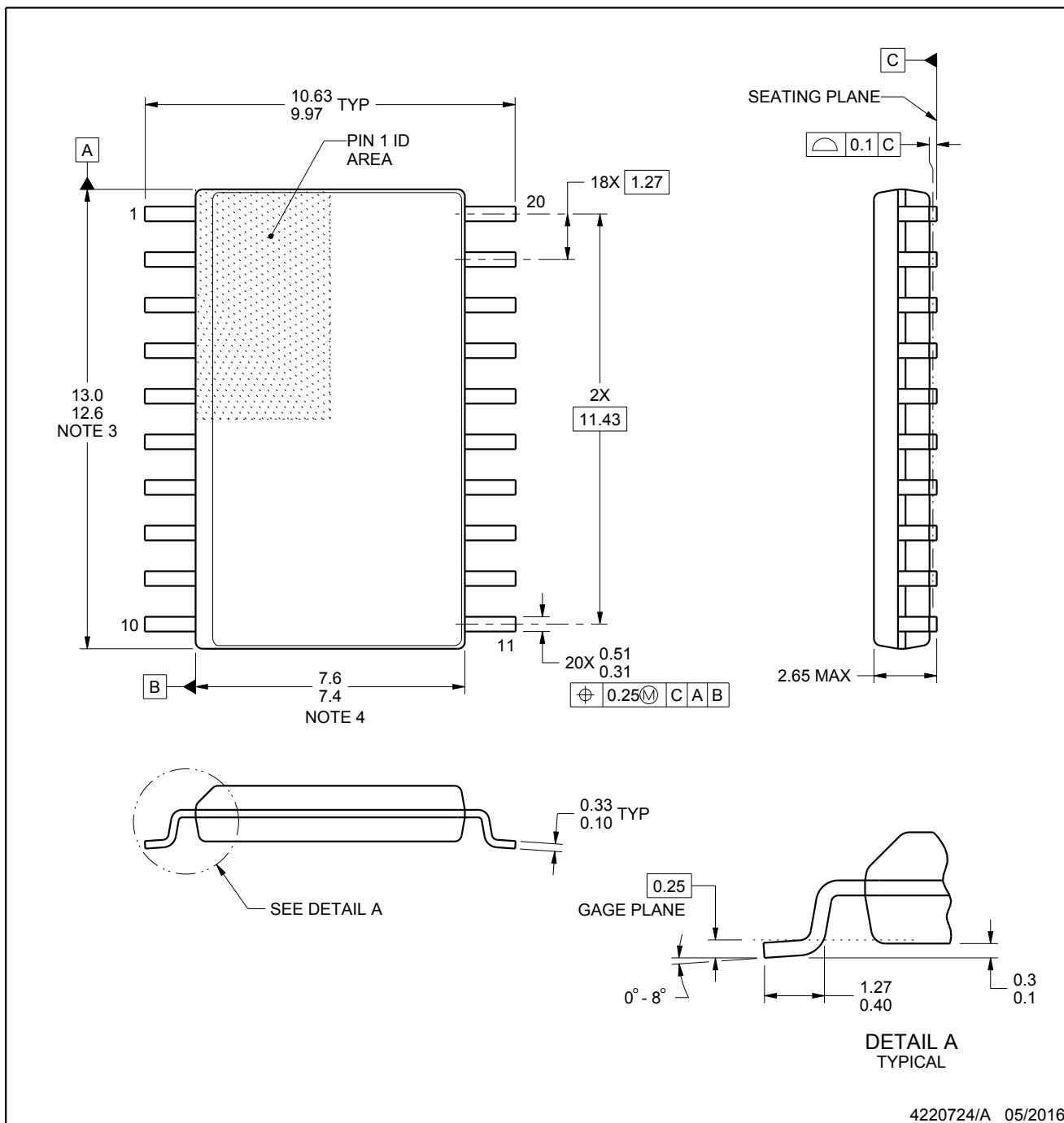


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

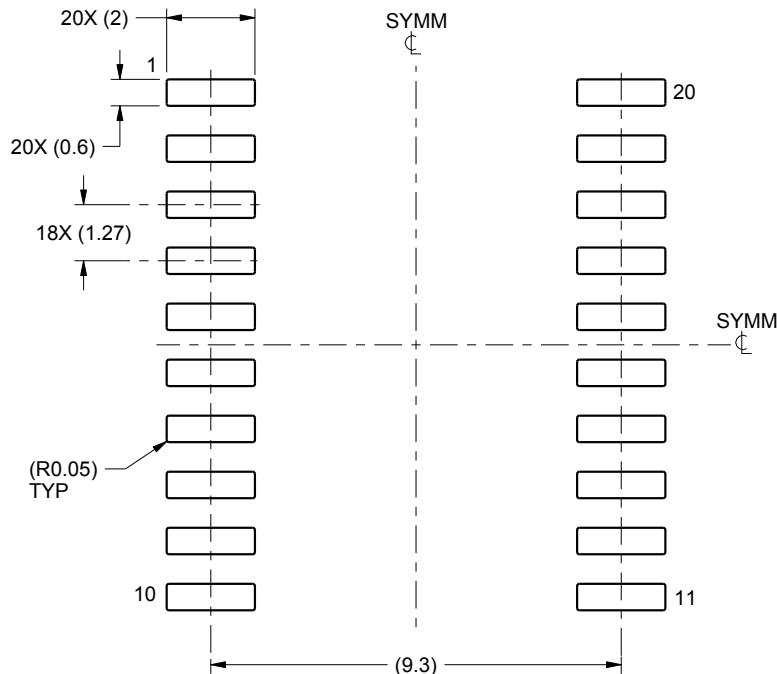
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

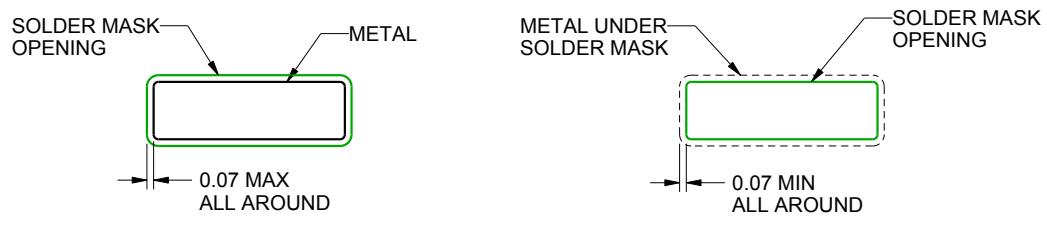
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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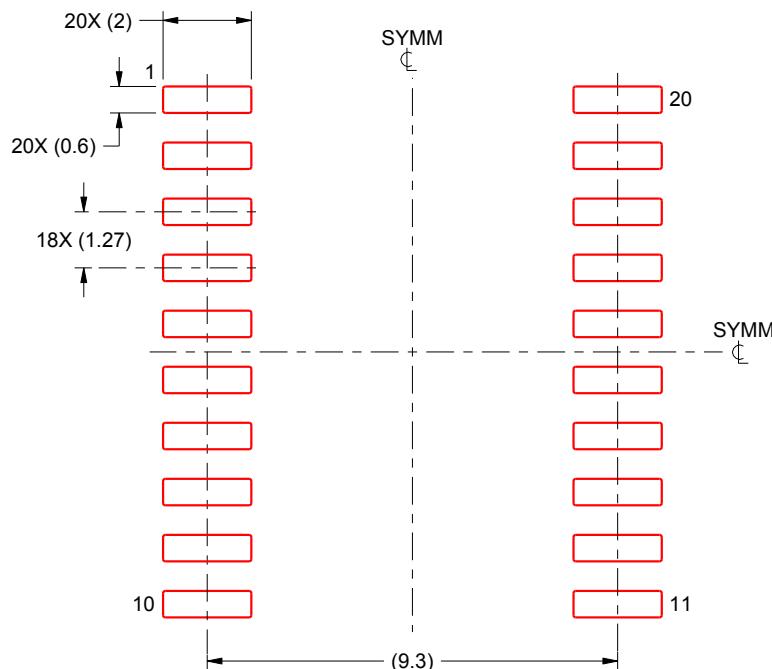
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**DW0020A****SOIC - 2.65 mm max height**

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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