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[SN74AHC1G08QDBVRQ1](#)

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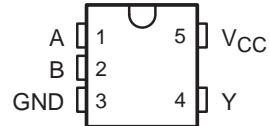
sales@integrated-circuit.com

SN74AHC1G08-Q1
SINGLE 2-INPUT POSITIVE-AND GATE

SCLS592C – OCTOBER 2004 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Operating Range of 2 V to 5.5 V
- Max t_{pd} of 9 ns at 5 V
- Low Power Consumption, 20- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- ESD Protection Level Per AEC-Q100 Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

DBV OR DCK PACKAGE
 (TOP VIEW)



description/ordering information

The SN74AHC1G08 is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION[†]

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING [§]
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G08IDBVRQ1	A08_
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G08IDCKRQ1	AE_
–40°C to 125°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G08QDBVRQ1	A08_
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G08QDCKRQ1	AE_

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

[§] The actual top-side marking has one additional character that designates the wafer fab/assembly site.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L



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SN74AHC1G08-Q1 **SINGLE 2-INPUT POSITIVE-AND GATE**

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5			V
		V _{CC} = 3 V	2.1	2.1			
		V _{CC} = 5.5 V	3.85	3.85			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5			V
		V _{CC} = 3 V	0.9	0.9			
		V _{CC} = 5.5 V	1.65	1.65			
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50			μA
		V _{CC} = 3.3 V ± 0.3 V	-4	-4			mA
		V _{CC} = 5 V ± 0.5 V	-8	-8			
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50			μA
		V _{CC} = 3.3 V ± 0.3 V	4	4			mA
		V _{CC} = 5 V ± 0.5 V	8	8			
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	100			ns/V
		V _{CC} = 5 V ± 0.5 V	20	20			
T _A	Operating free-air temperature	I Suffix	-40	85			°C
		Q Suffix			-40	125	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AHC1G08-Q1
SINGLE 2-INPUT POSITIVE-AND GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C TO 85°C		-40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.4		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.7		
V _{OL}	I _{OL} = 50 µA	2 V	0.1			0.1		0.1		V
		3 V	0.1			0.1		0.1		
		4.5 V	0.1			0.1		0.1		
	I _{OL} = 4 mA	3 V	0.36			0.44		0.52		
	I _{OL} = 8 mA	4.5 V	0.36			0.44		0.52		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V	±0.1			±1		±1		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	1			10		20		µA
C _i	V _I = V _{CC} or GND	5 V	4			10		10		pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C			-40°C TO 85°C		-40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	6.2	8.8	1	10.5		12.5		ns
t _{PHL}				6.2	8.8	1	10.5		12.5		
t _{PLH}	A or B	Y	C _L = 50 pF	8.7	12.3	1	14		16.5		ns
t _{PHL}				8.7	12.3	1	14		16.5		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C			-40°C TO 85°C		-40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	4.3	5.9		7		9		ns
t _{PHL}				4.3	5.9		7		9		
t _{PLH}	A or B	Y	C _L = 50 pF	5.8	7.9		9		11		ns
t _{PHL}				5.8	7.9		9		11		

operating characteristics, V_{CC} = 5 V, T_A = 25°C

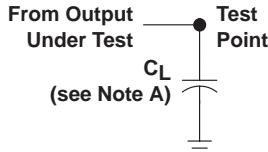
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	18	pF

SN74AHC1G08-Q1

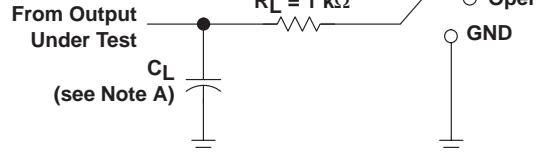
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PARAMETER MEASUREMENT INFORMATION

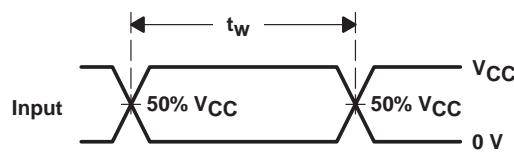


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

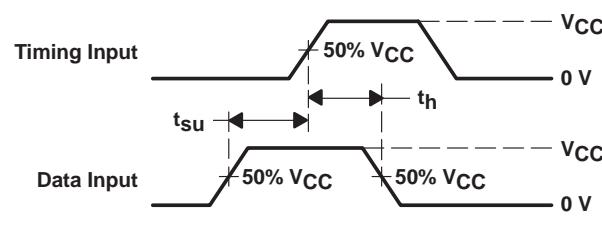


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

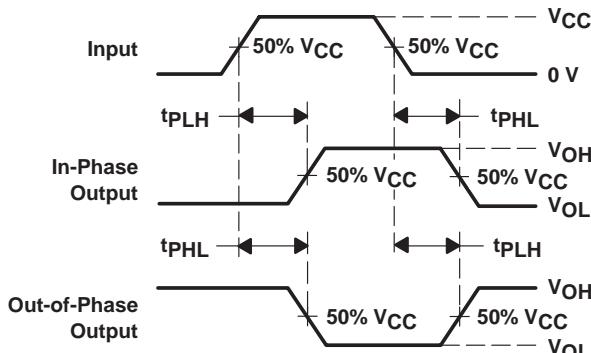
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



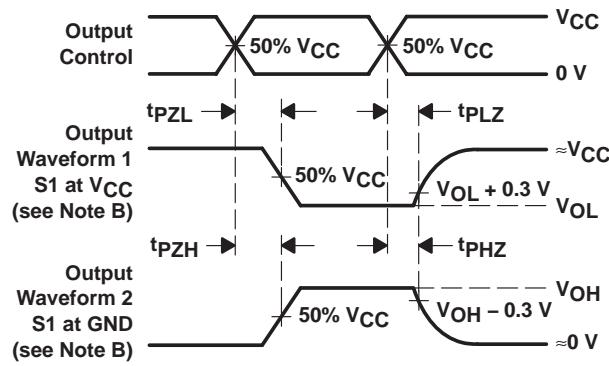
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AHC1G08QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A08U	Samples
SN74AHC1G08QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "—" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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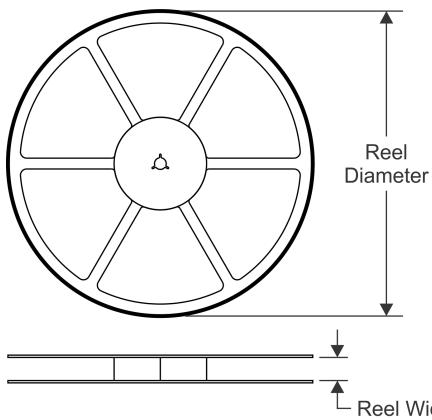
- Catalog: [SN74AHC1G08](#)

NOTE: Qualified Version Definitions:

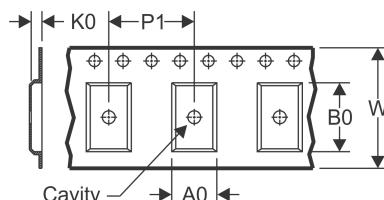
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

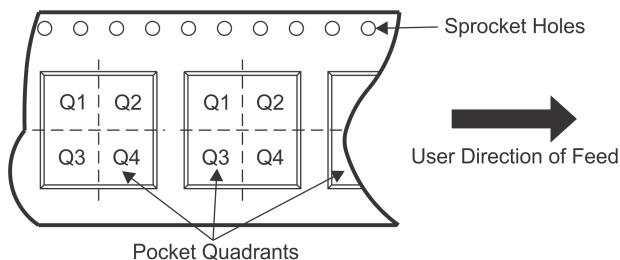


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

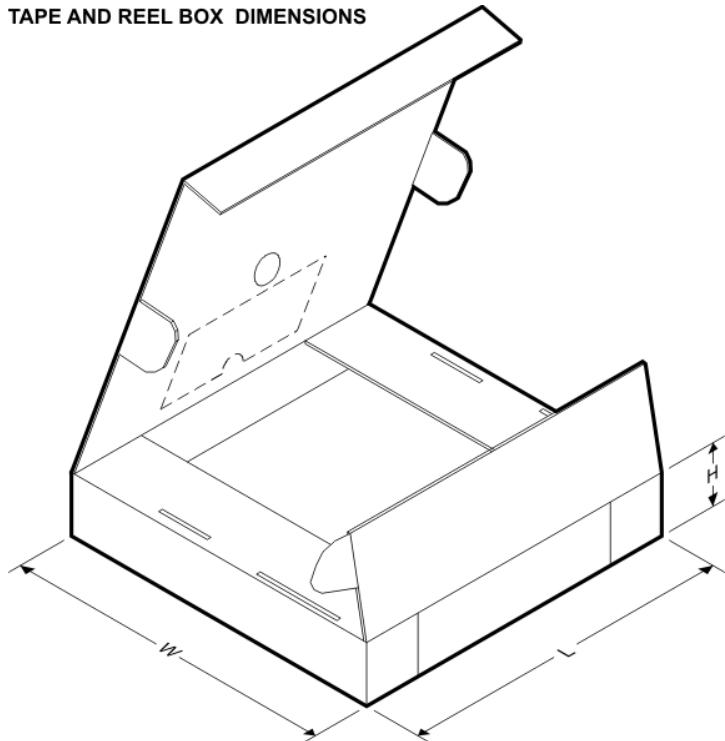
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G08QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G08QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



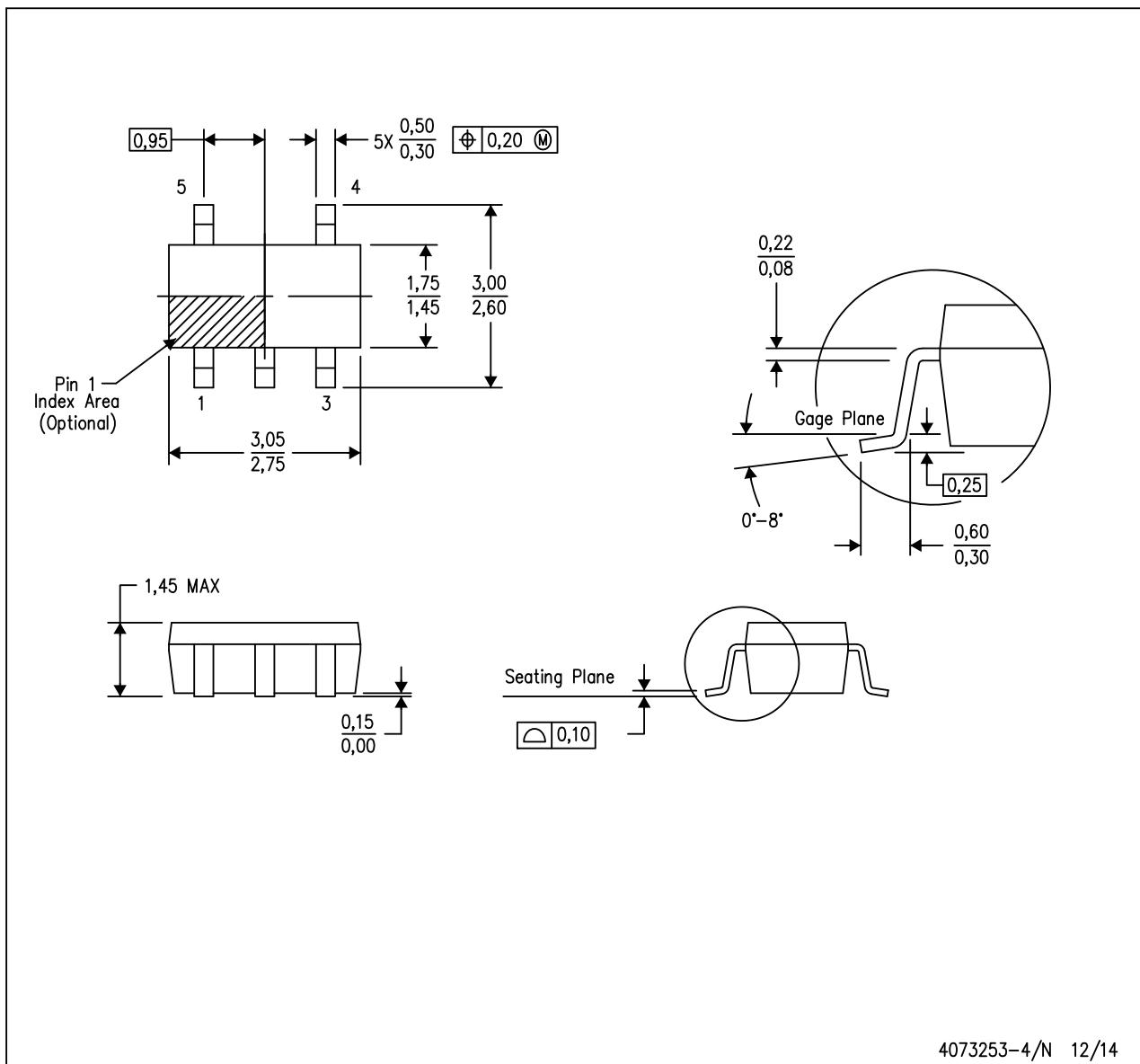
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G08QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
SN74AHC1G08QDCKRQ1	SC70	DCK	5	3000	203.0	203.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

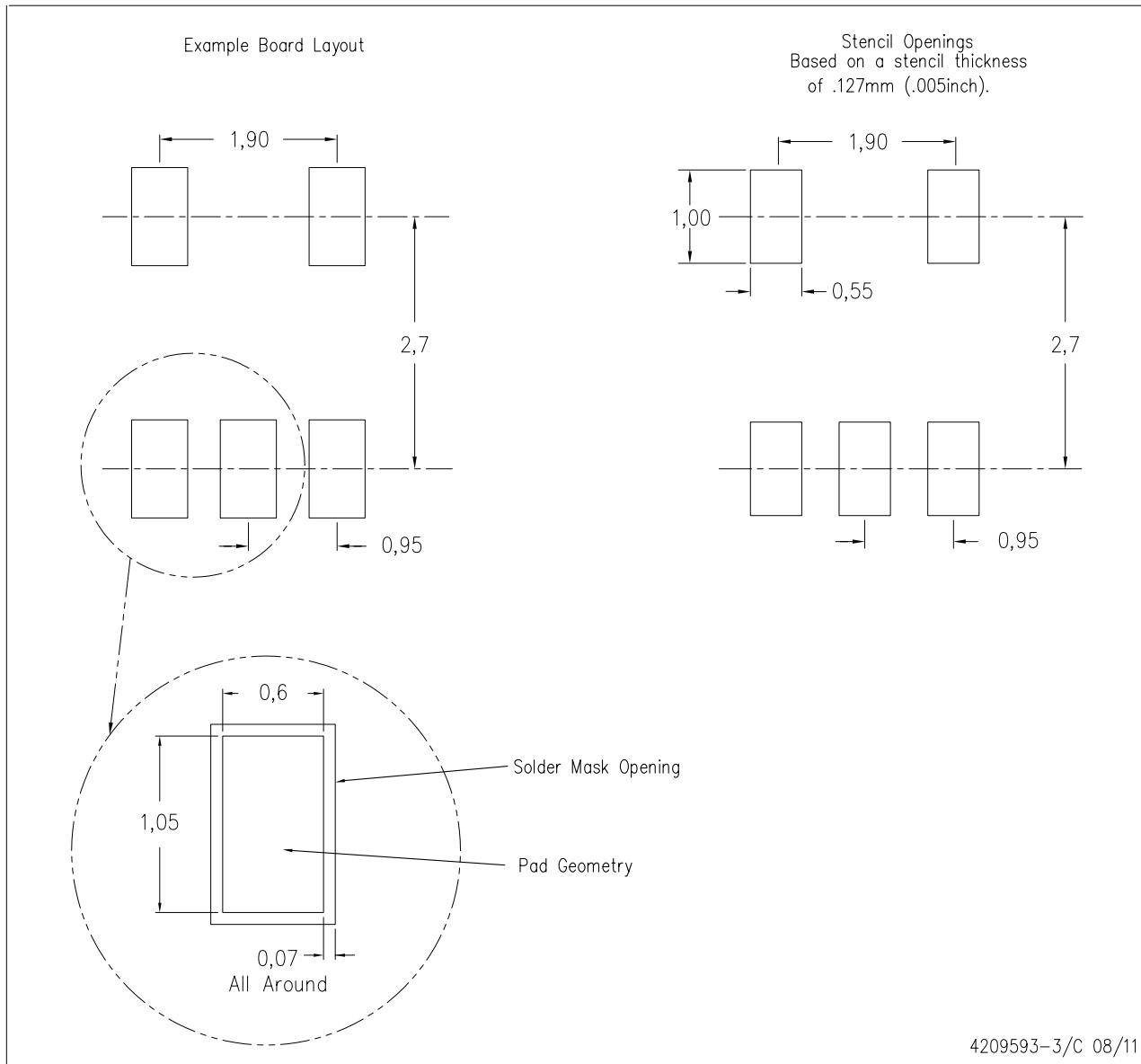
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-178 Variation AA.

LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



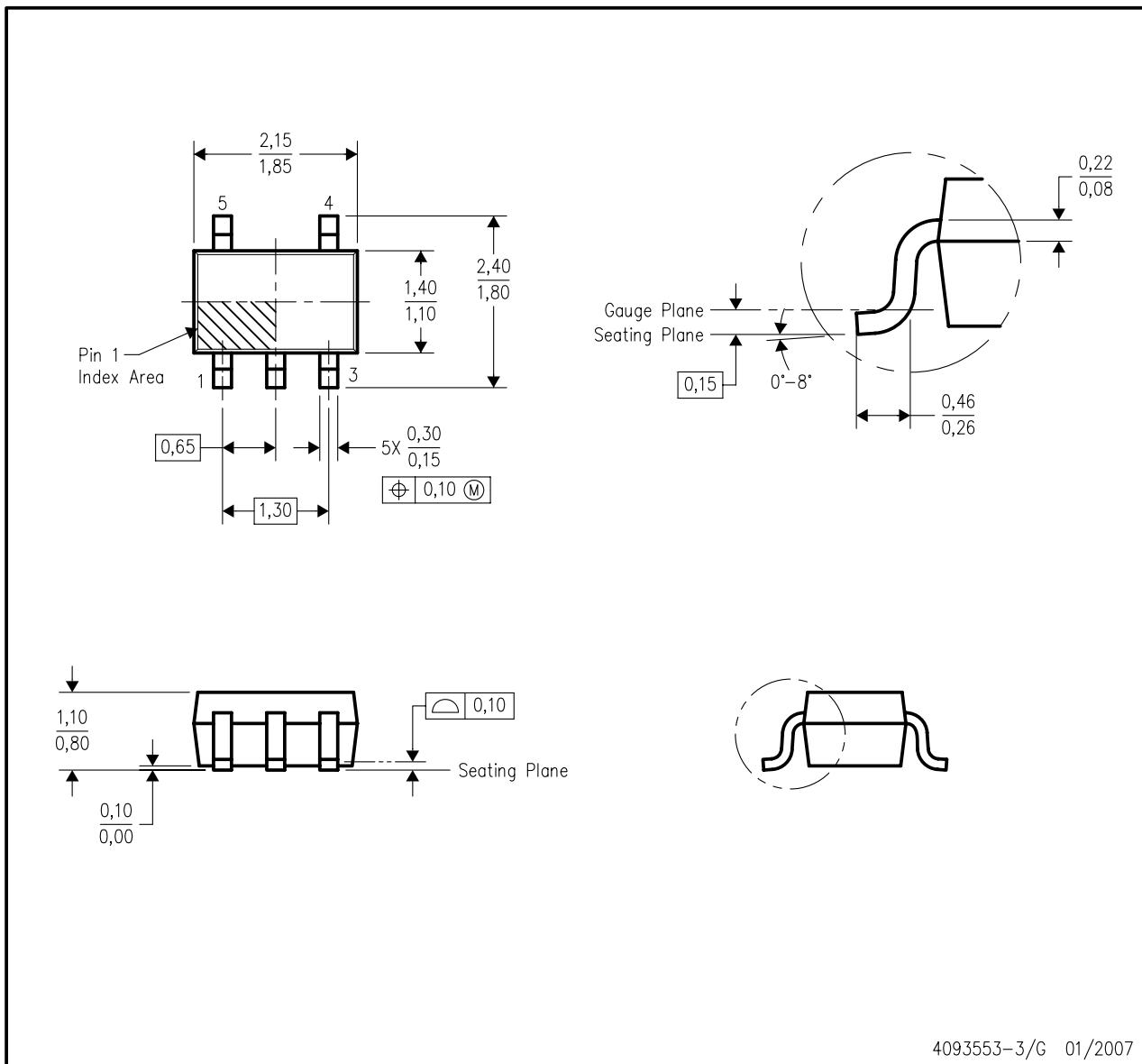
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

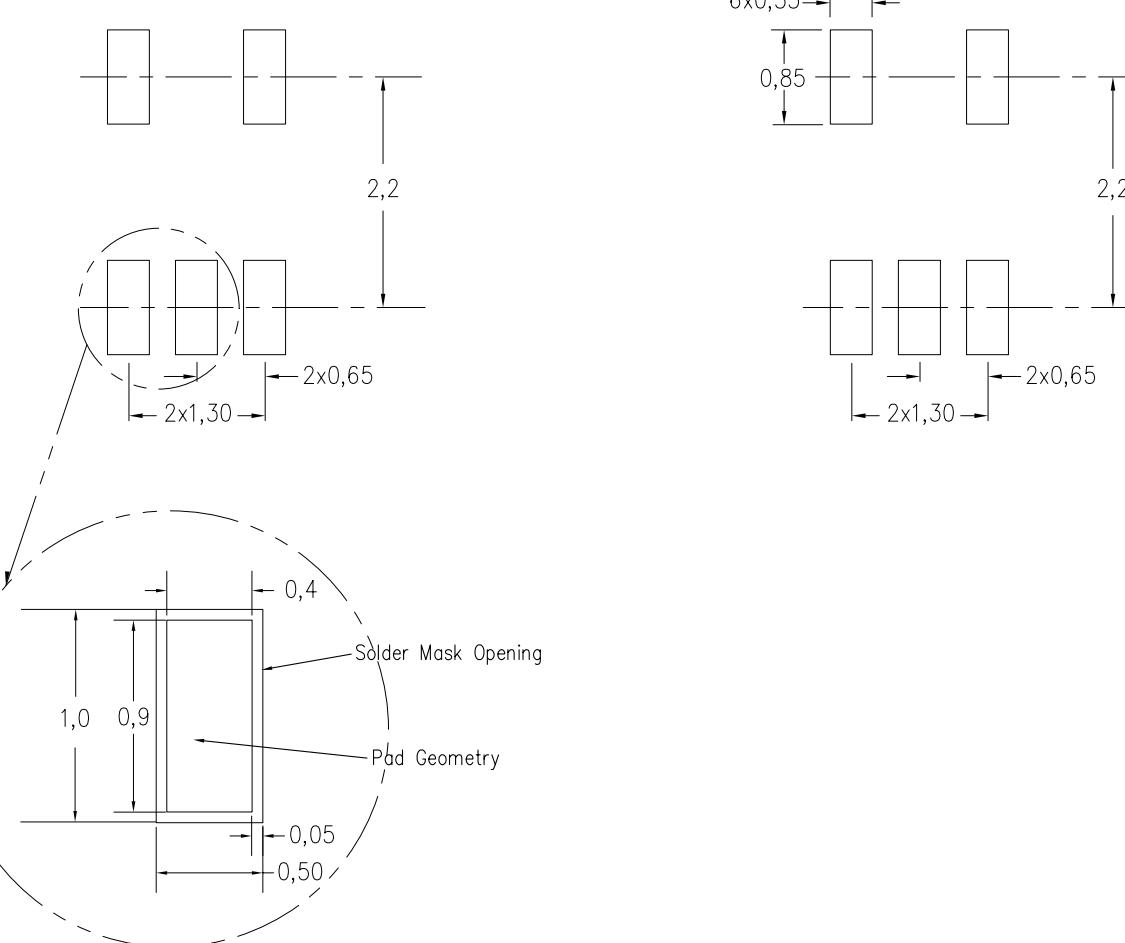
LAND PATTERN DATA

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4210356-2/C 07/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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