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**SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS**

SDLS179 - JANUARY 1981 - REVISED MARCH 1988

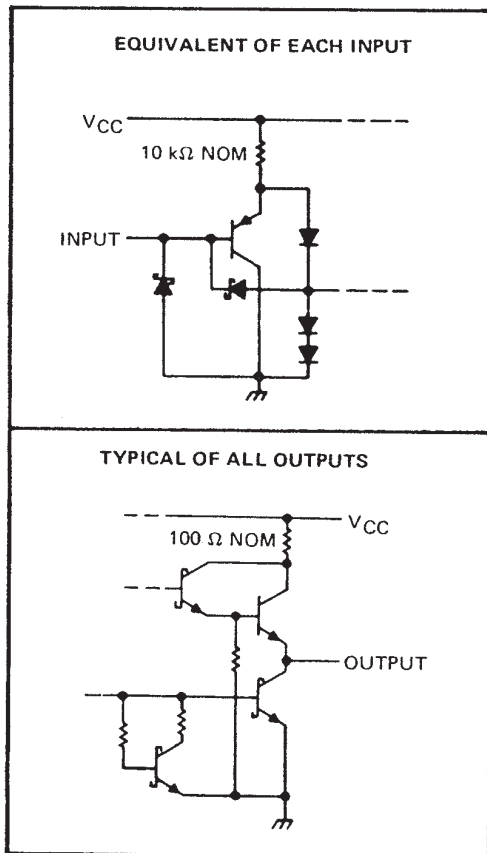
- Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98
- P-N-P Inputs Reduce Bus Loading
- 3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively

DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

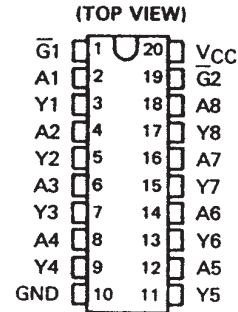
description

These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any \bar{G} places the affected outputs at high impedance.

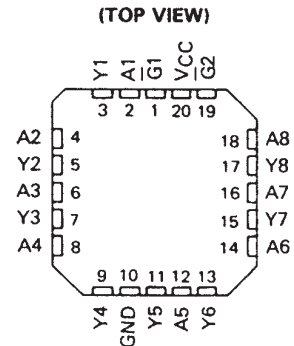
schematics of inputs and outputs



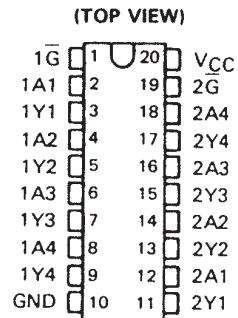
**SN54LS465 AND SN54LS466 . . . J PACKAGE
SN74LS465 AND SN74LS466 . . . DW OR N PACKAGE**



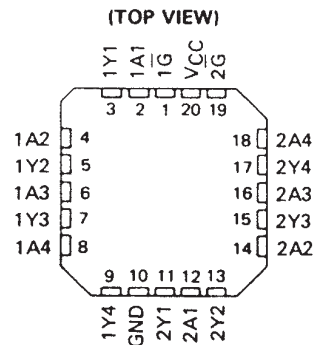
SN54LS465 AND SN54LS466 . . . FK PACKAGE



**SN54LS467 AND SN54LS468 . . . J PACKAGE
SN74LS467 AND SN74LS468 . . . DW OR N PACKAGE**



SN54LS467 AND SN54LS468 . . . FK PACKAGE

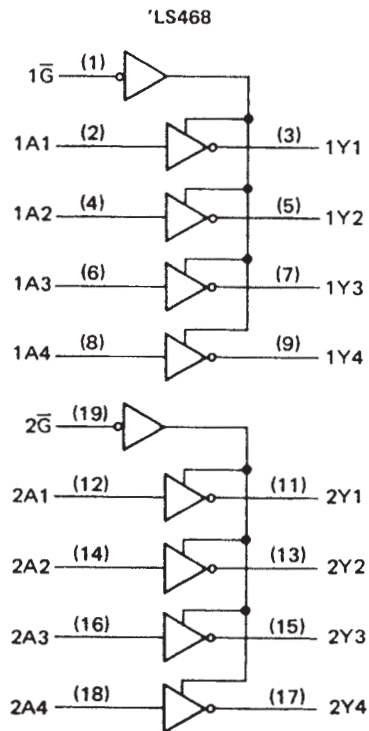
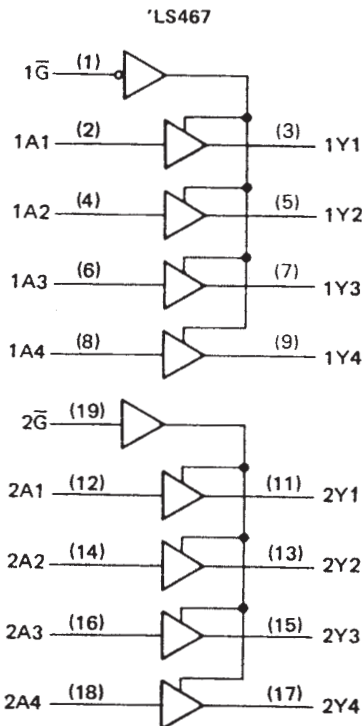
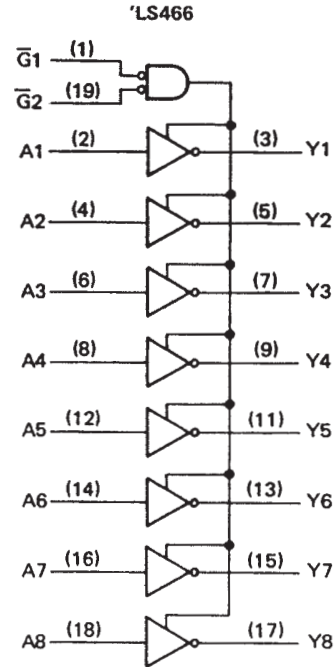
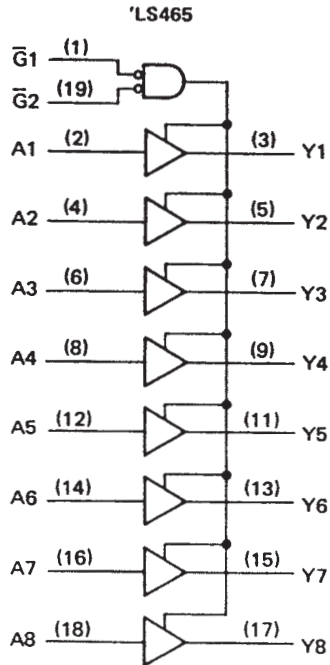


PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
 OCTAL BUFFERS WITH 3-STATE OUTPUTS**

SDLS179 – JANUARY 1981 – REVISED MARCH 1988

logic diagrams (positive logic)

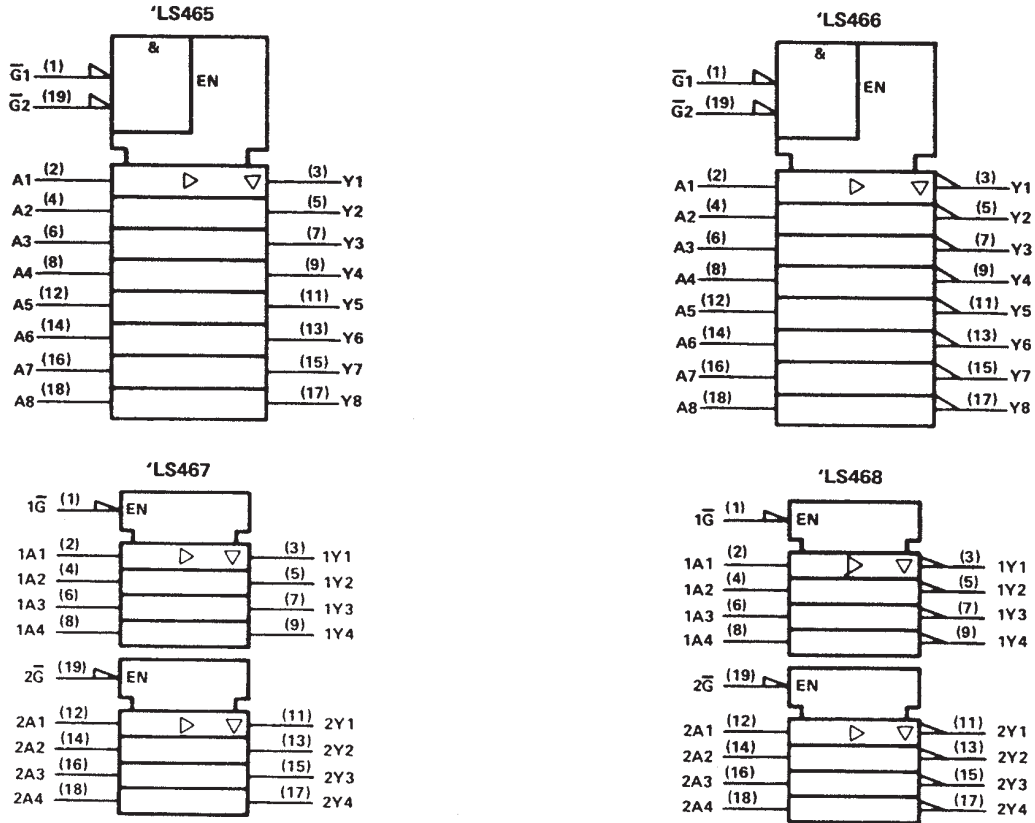


Pin numbers shown are for DW, J, and N packages.

**SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS**

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logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS465 thru SN54LS468	-55°C to 125°C
SN74LS465 thru SN74LS468	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468 OCTAL BUFFERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IH} High-level input voltage		2			2	V		
V _{IL} Low-level input voltage				0.7		0.8	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OH} = -1 mA I _{OH} = -2.6 mA		2.4	3.3		V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 12 mA I _{OL} = 24 mA		0.25	0.4	0.25 0.4 0.35 0.5	V	
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V, V _{IL} = V _{IL} max			20		20	μA	
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V, V _{IL} = V _{IL} max			-20		-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA	
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20		20	μA	
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.2		-0.2	mA	
I _{OS} Short-circuit output current§	V _{CC} = MAX, V _O = 0 V			-30	-130	-30 -130	mA	
I _{CC} Supply current	V _{CC} = MAX		Outputs low	19	32	19	32	mA
			Outputs high	13	22	13	22	
			Output Hi-Z	22	37	22	37	
			Outputs low	14	23	14	23	
			Outputs high	6	10	6	10	
			Outputs Hi-Z	17	28	17	28	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467			'LS466, 'LS468			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	A _i	Y _i	R _L = 667 Ω, C _L = 45 pF		9	15		7	12	ns
t _{PHL}	A _i	Y _i			12	18		9	15	ns
t _{PZH}	\bar{G} ↓	Y			25	40		25	40	ns
t _{PZL}	\bar{G} ↓	Y			29	45		29	45	ns
t _{PHZ}	\bar{G} ↑	Y	R _L = 667 Ω, C _L = 5 pF		25	40		25	40	ns
t _{PLZ}	\bar{G} ↑	Y			30	45		30	45	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS465DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	LS465	
SN74LS465N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70	SN74LS465N	
SN74LS465N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70	SN74LS465N	
SN74LS465NE4	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS465NE4	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS466DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74LS466DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74LS466N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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Datasheet of SN74LS465DW - IC BUFF/DVR TRI-ST 8BIT 20SOIC

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PACKAGE OPTION ADDENDUM

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6-Sep-2015

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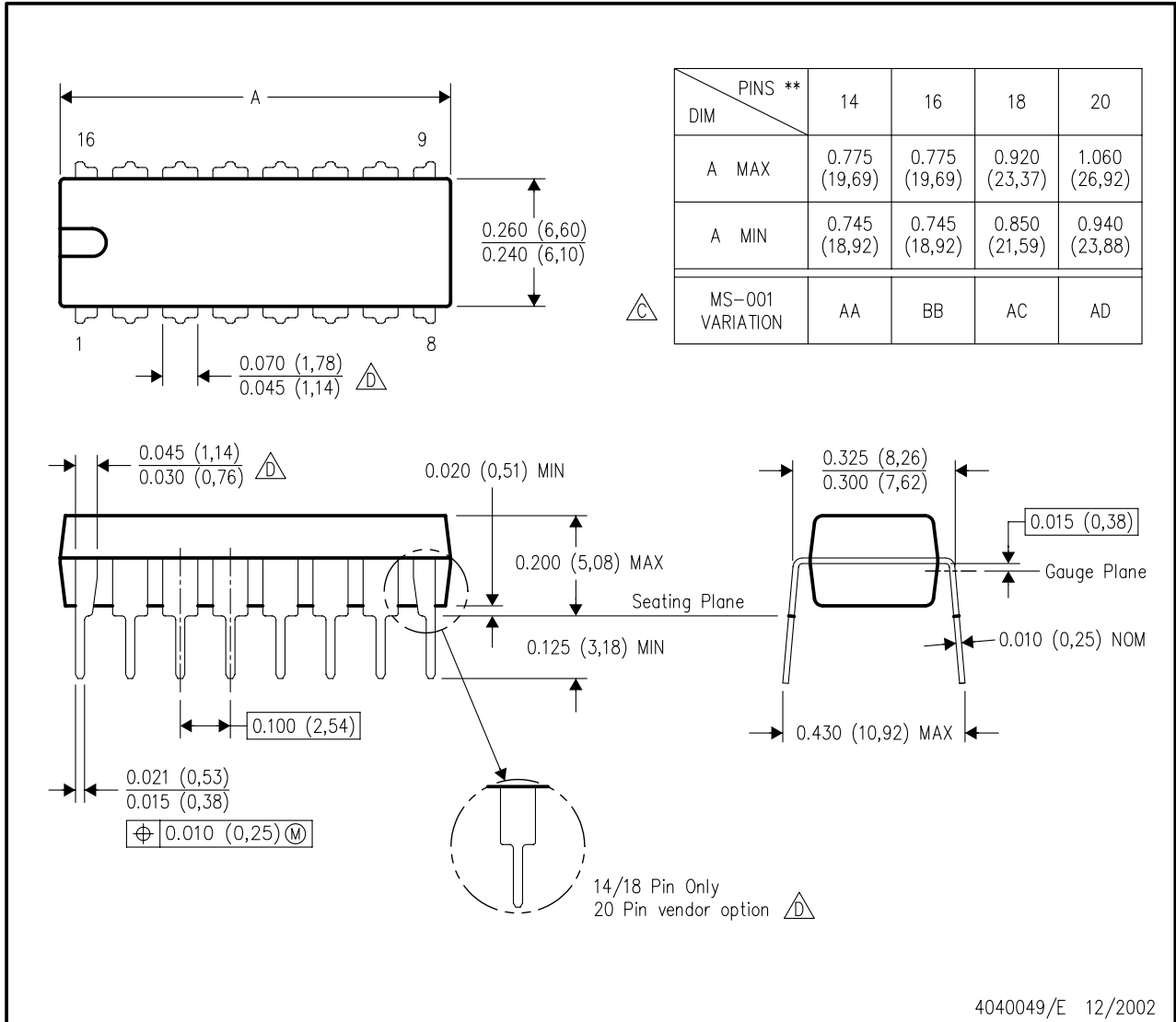
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MECHANICAL DATA

N (R-PDIP-T)**

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

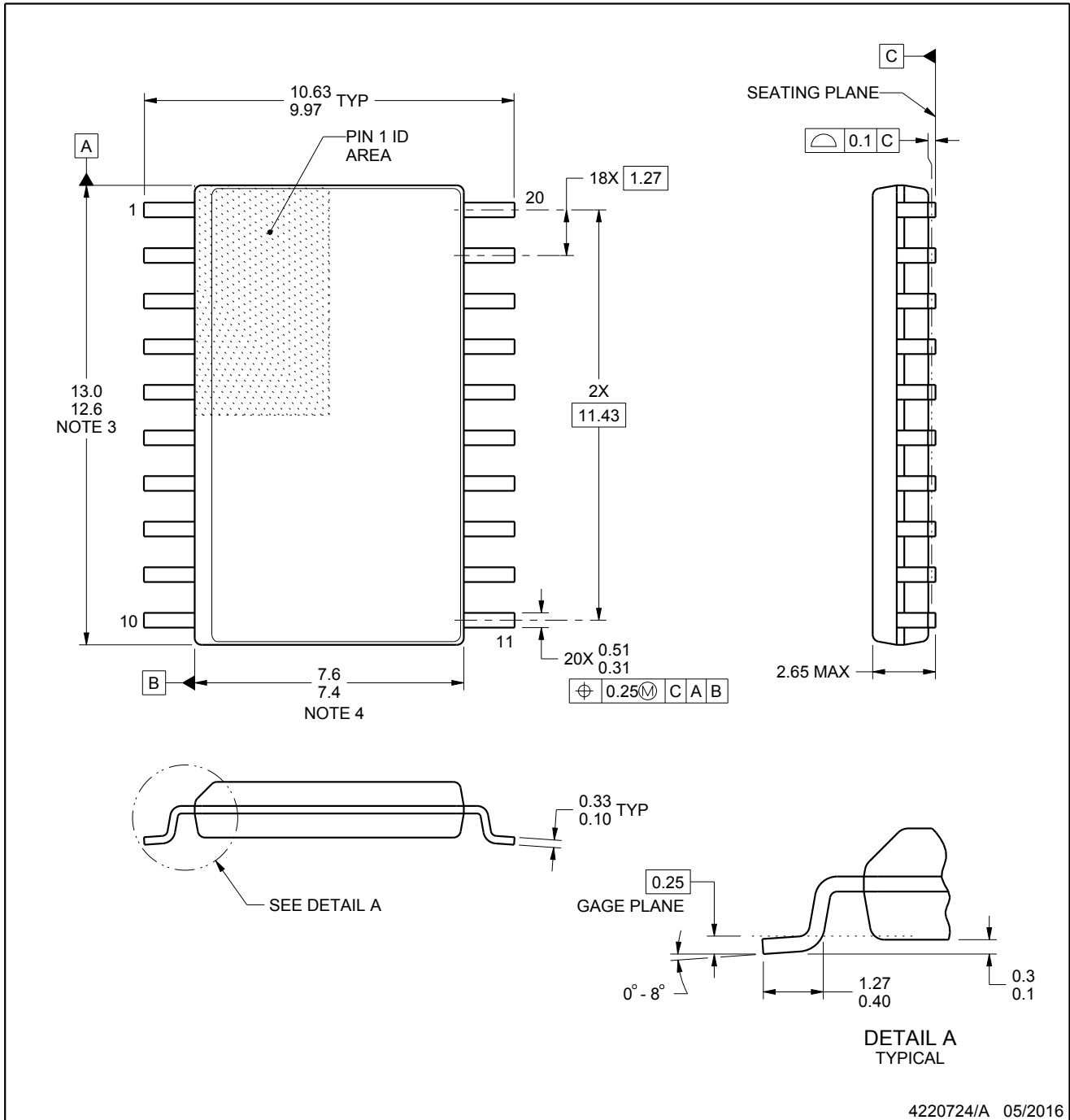


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

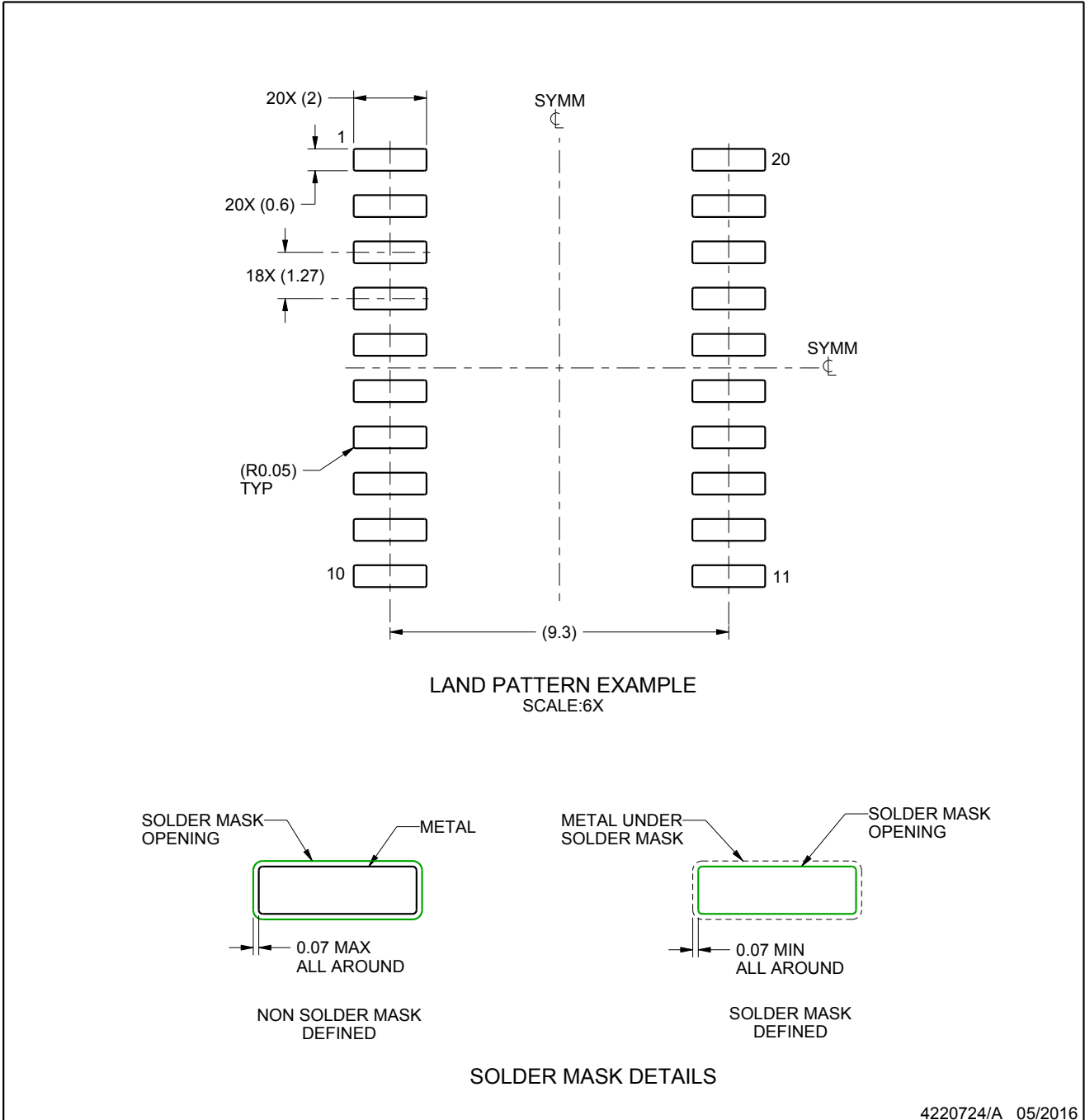
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES: (continued)

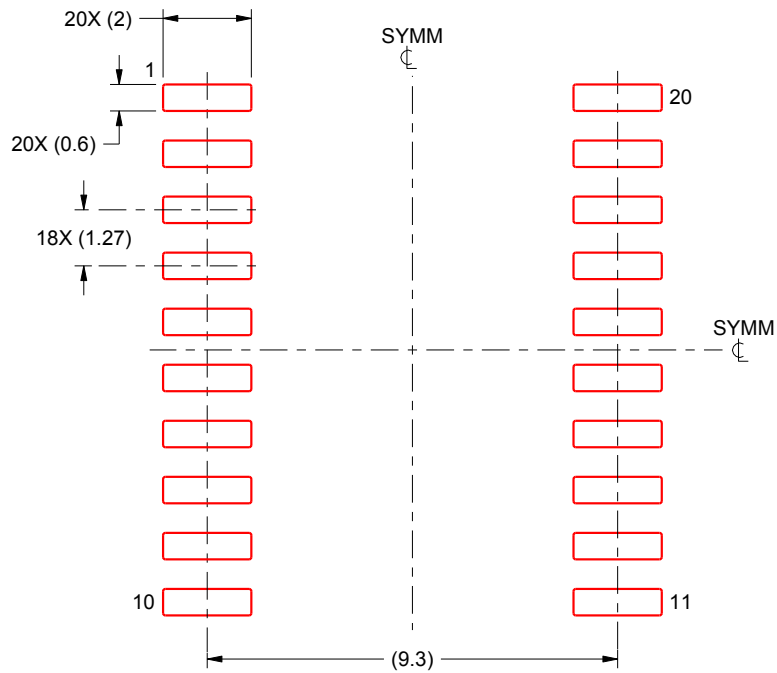
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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