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Texas Instruments
LMH6734MQ/NOPB

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# LMH6734 Single Supply, Ultra High-Speed, Triple Selectable Gain Buffer

**Check for Samples: LMH6734**

## FEATURES

- **(Typical Values Unless Otherwise Specified.)**
- **Supply Range 3V to 12V Single Supply**
- **Supply Range ±1.5V to ±6V Split Supply**
- **925 MHz −3 dB Small Signal Bandwidth ($A_V$ = +1, $V_S$ = ±5V)**
- **650 MHz −3 dB Small Signal Bandwidth ($A_V$ = +2, $V_S$ = 5V)**
- **Low Supply Current (5.5 mA per op amp, $V_S$ = 5V)**
- **2.1 nV/√Hz Input Noise Voltage**
- **3750 V/µs Slew Rate ($V_S$ = ±5V)**
- **70 mA Linear Output Current ($A_V$ = +2, $V_S$ = ±5V)**
- **Input Range and Output Swing to 1V from each Supply Rail**

## APPLICATIONS

- **HDTV Component Video Driver**
- **CAT5 Component Video Driver**
- **High Resolution Projectors**
- **Wide Dynamic Range IF Amp**
- **DDS Post-amps**
- **Wideband Inverting Summer**
- **Line Driver**

## DESCRIPTION

The LMH6734 is a high speed monolithic selectable gain buffer designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from TI's current feedback architecture, the LMH6734 offers gains of −1, +1 and +2. At a gain of +2 the LMH6734 supports ultra high resolution video systems with a 560 MHz 2 $V_{PP}$3 dB bandwidth. With this large signal bandwidth and 2.1 nV/√Hz of input referred noise, the LMH6734 is ideal for driving component video over CAT5 cable up to 200 ft without frequency and gain equalization. The LMH6734 is offered in a space saving 16-Pin SSOP package.

## Connection Diagram

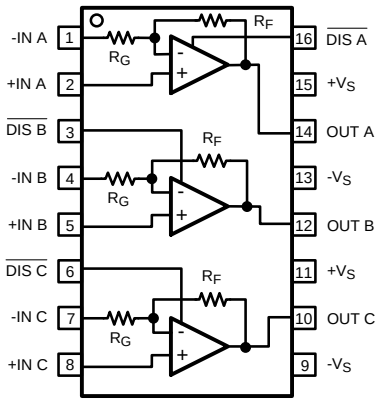


**Figure 1. 16-Pin SSOP - Top View**
**$R_F$ = $R_G$ = 327Ω**

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | | |
|---|---|---|
| ESD Tolerance(3) | Human Body Model | 2000V |
| | Machine Model | 200V |
| Supply Voltage ($V^+$ - $V^-$) | | 13.2V |
| $I_{OUT}$ | | See(4) |
| Common Mode Input Voltage | | $\pm V_{CC}$ |
| Maximum Junction Temperature | | +150°C |
| Storage Temperature Range | | −65°C to +150°C |
| Soldering Information | Infrared or Convection (20 sec.) | 235°C |
| | Wave Soldering (10 sec.) | 260°C |
| Storage Temperature Range | | −65°C to +150°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDECField-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current ($I_{OUT}$) is determined by device power dissipation limitations. See the POWER DISSIPATION section of the Application Information for more details.

## Operating Ratings(1)

| | | |
|---|---|---|
| Temperature Range(2) | | −40°C to +85°C |
| Supply Voltage ($V^+$ - $V^-$) | | 3V to 12V |
| Thermal Resistance | | |
| **Package** | **($\theta_{JC}$)** | **($\theta_{JA}$)** |
| 16-Pin SSOP | 36°C/W | 120°C/W |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

## 5V Electrical Characteristics(1)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = +5V, $A_V$ = +2, $R_L$ = 100Ω. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min(2) | Typ(3) | Max(2) | Units |
|---|---|---|---|---|---|---|
| **Frequency Domain Performance** | | | | | | |
| UGBW | −3 dB Bandwidth | Unity Gain, $V_{OUT}$ = 200 $mV_{PP}$ | | 870 | | MHz |
| SSBW | −3 dB Bandwidth | $V_{OUT}$ = 200 $mV_{PP}$, $R_L$ = 100Ω | | 650 | | MHz |
| SSBW | | $V_{OUT}$ = 200 $mV_{PP}$, $R_L$ = 150Ω | | 685 | | |
| LSBW | | $V_{OUT}$ = 2 $V_{PP}$ | | 480 | | |
| 0.1 dB BW | 0.1 dB Gain Flatness | $V_{OUT}$ = 200 $mV_{PP}$ | | 130 | | MHz |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Information for information on temperature de-rating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

## 5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = +5V, $A_V$ = +2, $R_L$ = 100Ω. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| **Time Domain Response** | | | | | | |
| TRS | Rise and Fall Time (10% to 90%) | 2V Step | | 0.7 | | ns |
| SR | Slew Rate | 2V Step | | 1900 | | V/µs |
| $t_s$ | Settling Time to 0.1% | 2V Step | | 10 | | ns |
| $t_e$ | Enable Time | From $\overline{\text{Disable}}$ = Rising Edge | | 10 | | ns |
| $t_d$ | Disable Time | From $\overline{\text{Disable}}$ = Falling Edge | | 15 | | ns |
| **Distortion** | | | | | | |
| HD2L | 2nd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −63 | | dBc |
| HD3L | 3rd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −73 | | dBc |
| **Equivalent Input Noise** | | | | | | |
| $V_N$ | Non-Inverting Voltage | >10 MHz | | 2.1 | | nV/√Hz |
| $I_{CN}$ | Inverting Current | >10 MHz | | 18.6 | | pA/√Hz |
| $N_{CN}$ | Non-Inverting Current | >10 MHz | | 26.9 | | pA/√Hz |
| **Video Performance** | | | | | | |
| DG | Differential Gain | 4.43 MHz, $R_L$ = 150Ω | | 0.03 | | % |
| DP | Differential Phase | 4.43 MHz, $R_L$ = 150Ω | | 0.025 | | deg |
| **Static, DC Performance** | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | | 0.4 | 2.0<br>**2.5** | mV |
| $I_{BN}$ | Input Bias Current | Non-Inverting | 2 | 16.7 | 28<br>**32** | µA |
| PSRR | Power Supply Rejection Ratio | +PSRR | 59<br>**59** | 61 | | dB |
| | | −PSRR | 58<br>**56** | 61 | | |
| CMRR | Common Mode Rejection Ratio | | 52<br>**52** | 54.5 | | dB |
| XTLK | Crosstalk | Input Referred, f = 10 MHz, Drive Channels A, C and Measure Channel B | | −80 | | dB |
| $I_{CC}$ | Supply Current | All three amps Enabled, No Load | 15<br>**15** | 16.7 | 18<br>**19** | mA |
| | Supply Current Disabled $V^+$ | $R_L$ = ∞ | | 1.54 | 1.8 | mA |
| | Supply Current Disabled $V^-$ | $R_L$ = ∞ | | 0.75 | 1.8 | mA |
| | Gain Error | $R_L$ = ∞ | | 0.2 | 1.25 | % |
| | Gain | $A_V$ = +2 | 1.975 | 1.996 | 2.025 | V/V |
| | | $A_V$ = +1 | | 0.998 | | |
| | | $A_V$ = −1 | −0.9875 | −0.998 | −1.0125 | |
| **Miscellaneous Performance** | | | | | | |
| $R_{IN}$+ | Non-Inverting Input Resistance | | | 200 | | kΩ |
| $C_{IN}$+ | Non-Inverting Input Capacitance | | | 1 | | pF |
| $R_O$ | Output Impedance | DC | | 0.05 | | Ω |
| $V_O$ | Output Voltage Range | $R_L$ = 100Ω | 1.25-3.75<br>**1.3-3.7** | 1.12-3.88 | | V |
| | | $R_L$ = ∞ | 1.11-3.89<br>**1.15-3.85** | 1.03-3.97 | | |
| CMIR | Input Range | Driving input +INA, CMRR > 40 dB | 1.1-3.9<br>**1.2-3.8** | 1.0-4.0 | | V |

## 5V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = +5V, $A_V$ = +2, $R_L$ = 100Ω. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min(2) | Typ(3) | Max(2) | Units |
|---|---|---|---|---|---|---|
| $I_O$ | Linear Output Current | $V_{IN}$ = 0V, $V_{OUT}$ < ±42 mV(4) | ±50 | ±60 | | mA |
| $I_{SC}$ | Short Circuit Current | $V_{IN}$ = 2V Output Shorted to Ground(5) | | 170 | | mA |
| $I_{IH}$ | Disable Pin Bias Current High | $\overline{\text{Disable}}$ Pin = $V^+$ | | −72 | | µA |
| $I_{IL}$ | Disable Pin Bias Current Low | $\overline{\text{Disable}}$ Pin = 0V | | −360 | | µA |
| $V_{DMAX}$ | Voltage for Disable | $\overline{\text{Disable}}$ Pin ≤ $V_{DMAX}$ | | 3.2 | | V |
| $V_{DMIM}$ | Voltage for Enable | $\overline{\text{Disable}}$ Pin ≥ $V_{DMIN}$ | | 3.6 | | V |

(4) The maximum output current ($I_{OUT}$) is determined by device power dissipation limitations. See the POWER DISSIPATION section of the Application Information for more details.
(5) Short circuit current should be limited in duration to no more than 10 seconds. See the POWER DISSIPATION section of the Application Information for more details.

## ±5V Electrical Characteristics(1)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = +5V, $V^-$ = −5V, $A_V$ = +2, $R_L$ = 100Ω. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min(2) | Typ(3) | Max(2) | Units |
|---|---|---|---|---|---|---|
| **Frequency Domain Performance** | | | | | | |
| UGBW | −3 dB Bandwidth | Unity Gain, $V_{OUT}$ = 200 $mV_{PP}$ | | 925 | | MHz |
| SSBW | −3 dB Bandwidth | $V_{OUT}$ = 200 $mV_{PP}$, $R_L$ = 100Ω | | 730 | | MHz |
| SSBW | | $V_{OUT}$ = 200 $mV_{PP}$, $R_L$ = 150Ω | | 760 | | |
| LSBW | | $V_{OUT}$ = 2 $V_{PP}$ | | 560 | | |
| 0.1 dB BW | 0.1 dB Gain Flatness | $V_{OUT}$ = 200 $mV_{PP}$ | | 270 | | MHz |
| **Time Domain Response** | | | | | | |
| TRS | Rise and Fall Time (10% to 90%) | 2V Step | | 0.7 | | ns |
| TRL | | 5V Step | | 0.8 | | |
| SR | Slew Rate | 2V Step | | 3750 | | V/µs |
| $t_s$ | Settling Time to 0.1% | 2V Step | | 10 | | ns |
| $t_e$ | Enable Time | From $\overline{\text{Disable}}$ = Rising Edge | | 10 | | ns |
| $t_d$ | Disable Time | From $\overline{\text{Disable}}$ = Falling Edge | | 15 | | ns |
| **Distortion** | | | | | | |
| HD2L | 2nd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −72 | | dBc |
| HD3L | 3rd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −63 | | dBc |
| **Equivalent Input Noise** | | | | | | |
| $V_N$ | Non-Inverting Voltage | >10 MHz | | 2.1 | | nV/√Hz |
| $I_{CN}$ | Inverting Current | >10 MHz | | 18.6 | | pA/√Hz |
| $N_{CN}$ | Non-Inverting Current | >10 MHz | | 26.9 | | pA/√Hz |
| **Video Performance** | | | | | | |
| DG | Differential Gain | 4.43 MHz, $R_L$ = 150Ω | | 0.03 | | % |
| DP | Differential Phase | 4.43 MHz, $R_L$ = 150Ω | | 0.03 | | deg |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$> $T_A$. See Application Information for information on temperature de-rating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

## ±5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = +5V, $V^-$ = −5V, $A_V$ = +2, $R_L$ = 100Ω. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| **Static, DC Performance** | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | | 0.6 | 2.4<br>**3.4** | mV |
| $I_{BN}$ | Input Bias Current | Non-Inverting | −14<br>**−19** | 3.5 | 19<br>**24** | µA |
| PSRR | Power Supply Rejection Ratio | +PSRR | 59<br>**59** | 61.5 | | dB |
| | | −PSRR | 58<br>**58** | 61 | | |
| CMRR | Common Mode Rejection Ratio | | 53<br>**53** | 55 | | dB |
| XTLK | Crosstalk | Input Referred, f = 10 MHz, Drive Channels A, C and Measure Channel B | | −80 | | dB |
| $I_{CC}$ | Supply Current | All three amps Enabled, No Load | 18<br>**18** | 19.5 | 20.8<br>**22** | mA |
| | Supply Current Disabled $V^+$ | $R_L$ = ∞ | | 1.54 | 1.8 | mA |
| | Supply Current Disabled $V^-$ | $R_L$ = ∞ | | 0.75 | 1.8 | mA |
| | Gain Error | $R_L$ = ∞ | | 0.2 | 1.25 | % |
| | Gain | $A_V$ = +2 | 1.975 | 1.996 | 2.025 | V/V |
| | | $A_V$ = +1 | | 0.998 | | |
| | | $A_V$ = −1 | −0.9875 | −0.998 | −1.0125 | |
| **Miscellaneous Performance** | | | | | | |
| $R_{IN}$+ | Non-Inverting Input Resistance | | | 200 | | kΩ |
| $C_{IN}$+ | Non-Inverting Input Capacitance | | | 1 | | pF |
| $R_O$ | Output Impedance | DC | | 0.05 | | Ω |
| $V_O$ | Output Voltage Range | $R_L$ = 100Ω | ±3.55<br>**±3.5** | ±3.7 | | V |
| | | $R_L$ = ∞ | ±3.85 | ±4.0 | | |
| CMIR | Input Range | Driving input +INA, CMRR > 40 dB | ±3.9<br>**±3.8** | ±4.0 | | V |
| $I_O$ | Linear Output Current | $V_{IN}$ = 0V, $V_{OUT}$ < ±43 mV[4] | 70 | ±80 | | mA |
| $I_{SC}$ | Short Circuit Current | $V_{IN}$ = 2V Output Shorted to Ground[5] | | 237 | | mA |
| $I_{IH}$ | Disable Pin Bias Current High | $\overline{\text{Disable}}$ Pin = $V^+$ | | −72 | | µA |
| $I_{IL}$ | Disable Pin Bias Current Low | $\overline{\text{Disable}}$ Pin = 0V | | −360 | | µA |
| $V_{DMAX}$ | Voltage for Disable | $\overline{\text{Disable}}$ Pin ≤ $V_{DMAX}$ | | 3.2 | | V |
| $V_{DMIM}$ | Voltage for Enable | $\overline{\text{Disable}}$ Pin ≥ $V_{DMIN}$ | | 3.6 | | V |

(4) The maximum output current ($I_{OUT}$) is determined by device power dissipation limitations. See the POWER DISSIPATION section of the Application Information for more details.
(5) Short circuit current should be limited in duration to no more than 10 seconds. See the POWER DISSIPATION section of the Application Information for more details.

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## Typical Performance Characteristics $V^+$ = +5V

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**Large Signal Frequency Response**

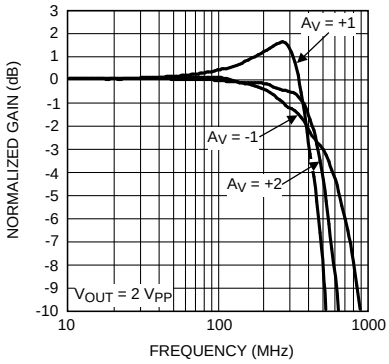


**Figure 2.**

**Small Signal Frequency Response**

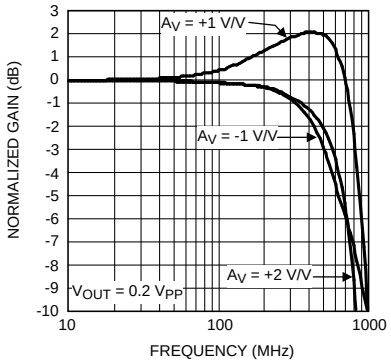


**Figure 3.**

**Small Signal Frequency Response**

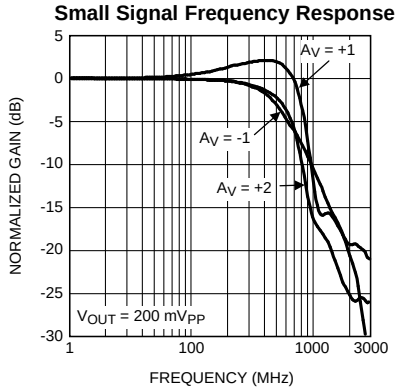


**Figure 4.**

**Frequency Response vs. $V_{OUT}$**

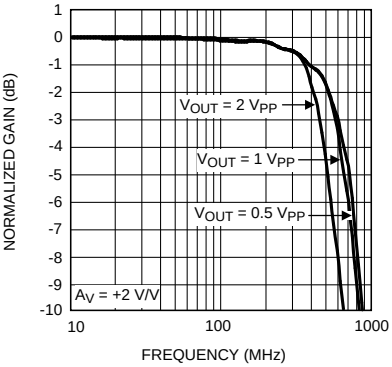


**Figure 5.**

**Frequency Response vs. Supply Voltage**

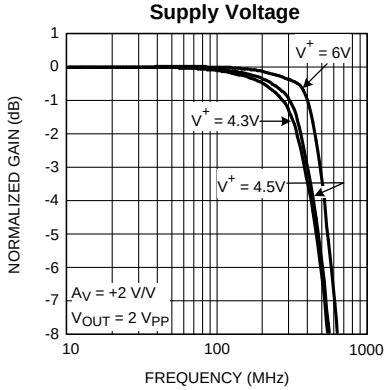


**Figure 6.**

**Gain Flatness**

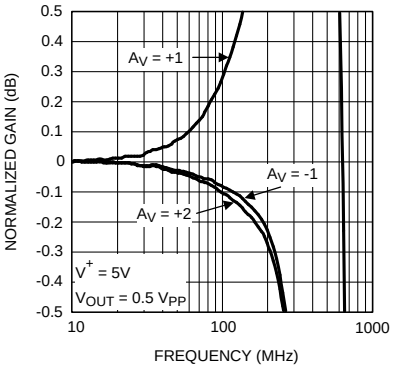


**Figure 7.**

## Typical Performance Characteristics $V^+$ = +5V (continued)

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**Gain Flatness, Dual Input Buffer**

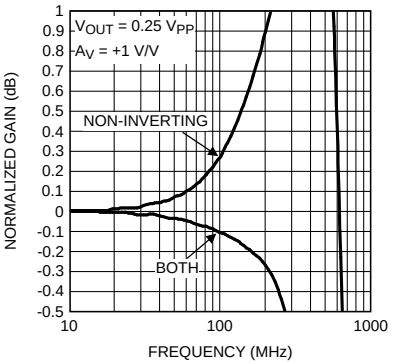


**Figure 8.**

**Pulse Response**

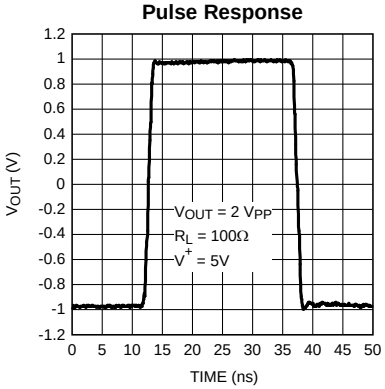


**Figure 9.**

**Crosstalk vs. Frequency**

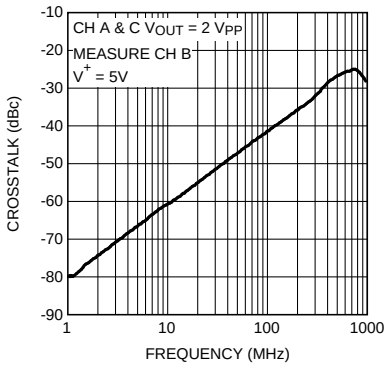


**Figure 10.**

**Distortion vs. Frequency**

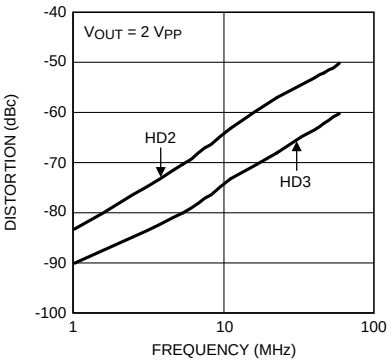


**Figure 11.**

**Distortion vs. Output Voltage**

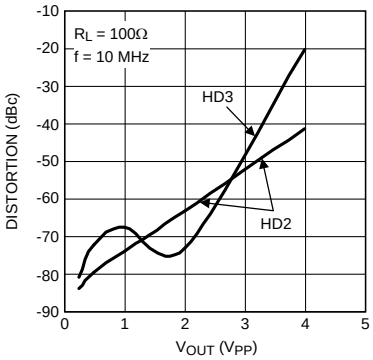


**Figure 12.**

**Small Signal Frequency Response vs. Resistive Load**

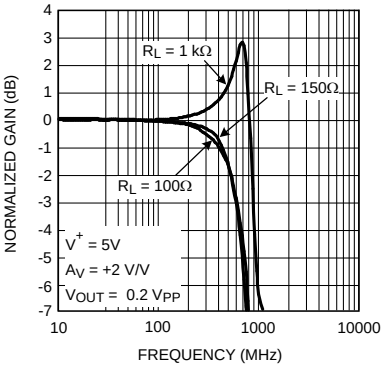


**Figure 13.**

## Typical Performance Characteristics $V^+$ = +5V (continued)

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**Frequency Response vs. Capacitive Load**

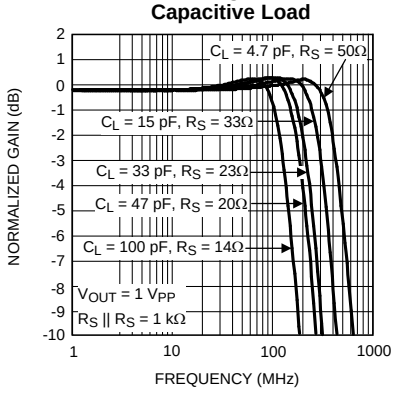


**Figure 14.**

**Series Output Resistance vs. Capacitive Load**

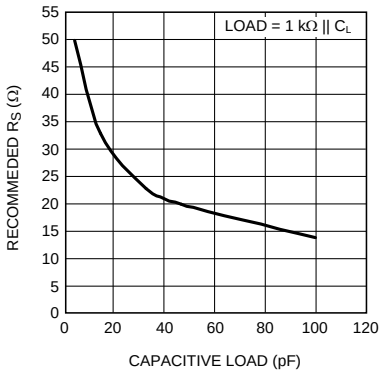


**Figure 15.**

**PSRR vs. Frequency**

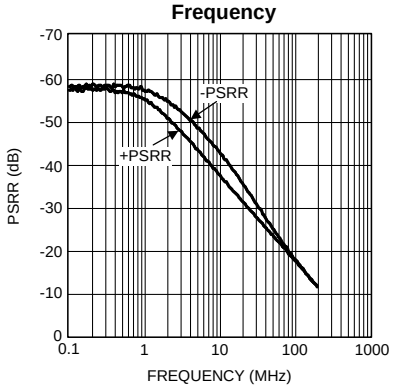


**Figure 16.**

**Open Loop Gain and Phase**

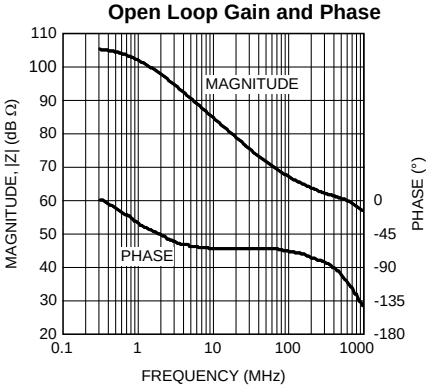


**Figure 17.**

**Closed Loop Output Impedance |Z|**

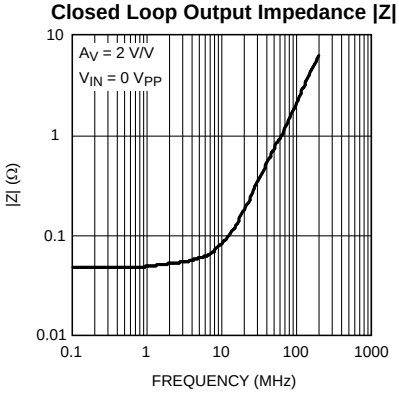


**Figure 18.**

**Disable Timing**

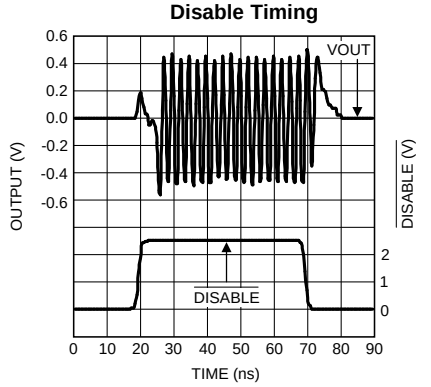


**Figure 19.**

## Typical Performance Characteristics $V^+$ = +5V (continued)

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**DC Errors vs. Temperature**

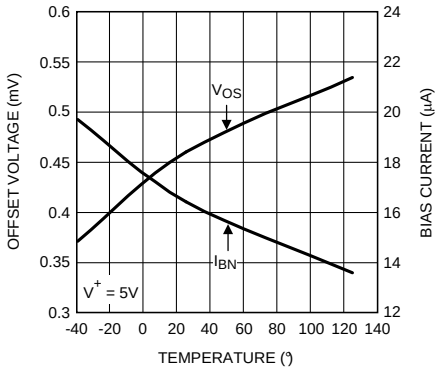


**Figure 20.**

**Channel to Channel Crosstalk vs. Frequency**

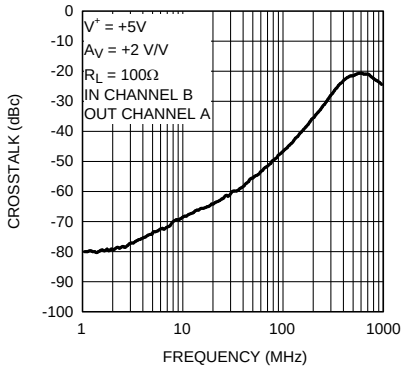


**Figure 21.**

**Disabled Channel Isolation vs. Frequency**

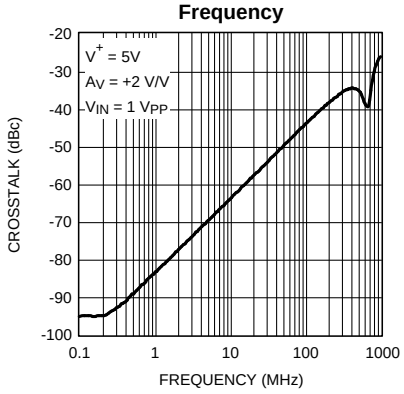


**Figure 22.**

## Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**Large Signal Frequency Response**

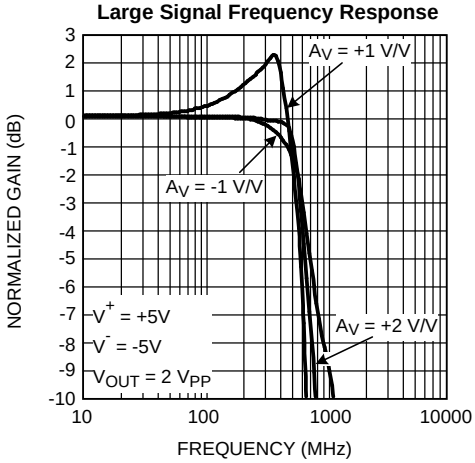


**Figure 23.**

**Small Signal Frequency Response**

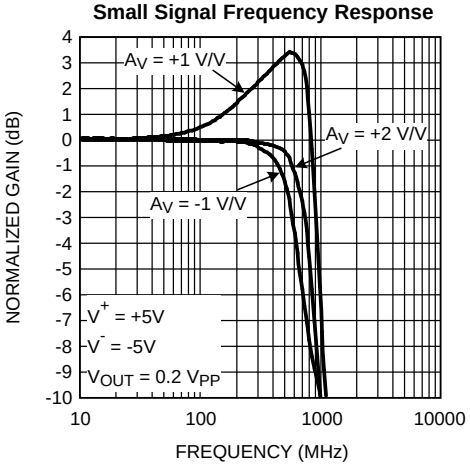


**Figure 24.**

**Frequency Response vs. $V_{OUT}$**

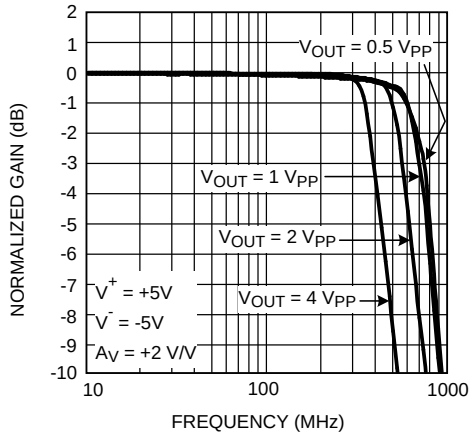


**Figure 25.**

**Frequency Response vs. Supply Voltage**

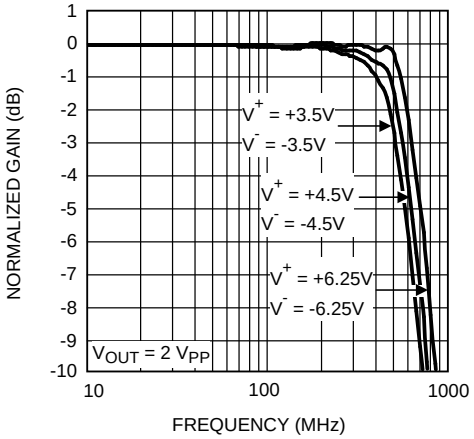


**Figure 26.**

**Gain Flatness**

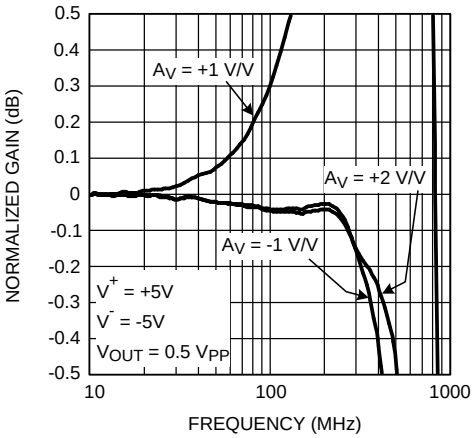


**Figure 27.**

**Gain Flatness, Dual Input Buffer**

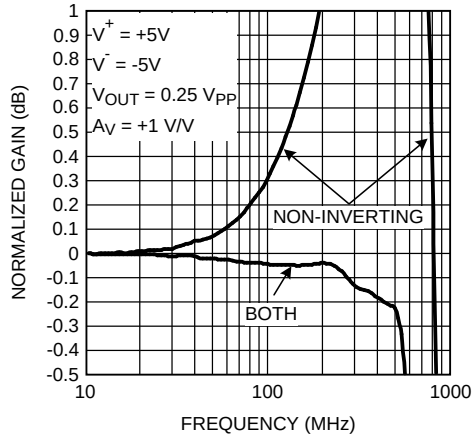


**Figure 28.**

## Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

($T_A$ = 25°C, $A_V$ = +2, $R_L$ = 100Ω, unless otherwise specified.)

**Pulse Response**

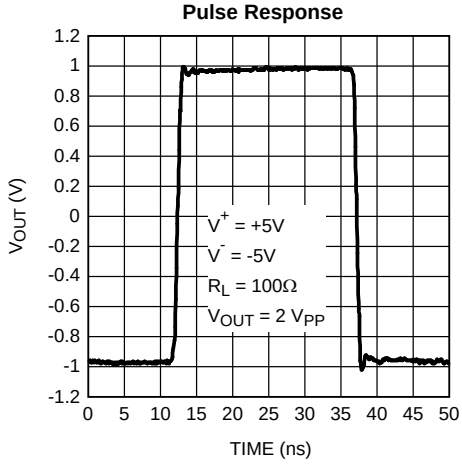


**Figure 29.**

**Pulse Response**

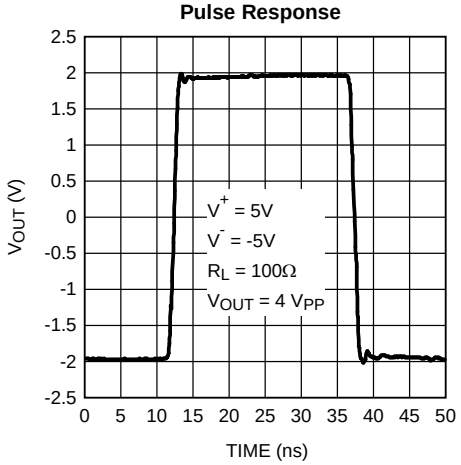


**Figure 30.**

**Distortion vs. Frequency**

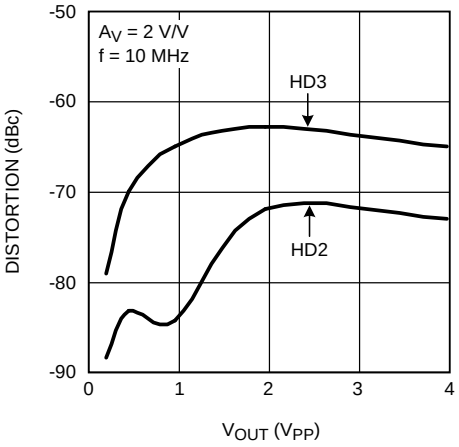


**Figure 31.**

**Distortion vs. Output Voltage**

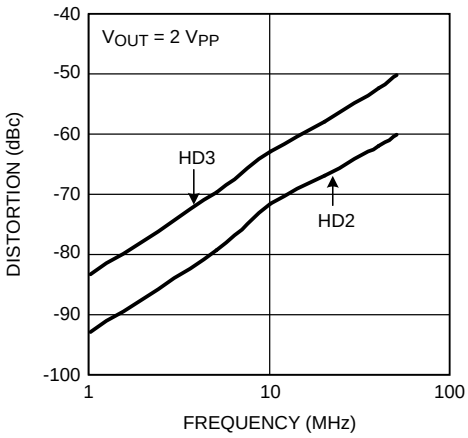


**Figure 32.**

**DC Errors vs. Temperature**

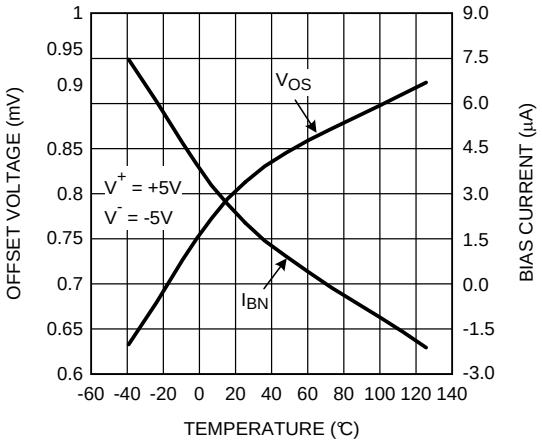


**Figure 33.**

**Crosstalk vs. Frequency**

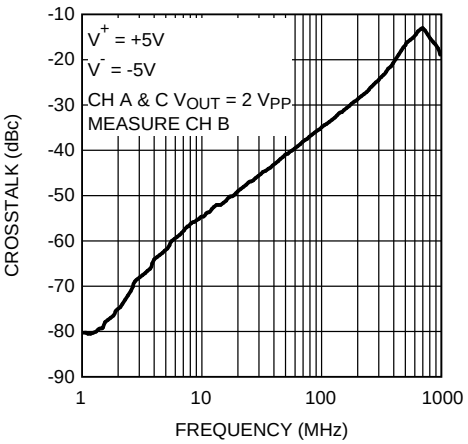


**Figure 34.**

# APPLICATION INFORMATION

## GENERAL INFORMATION

The LMH6734 is a high speed current feedback selectable gain buffer (SGB), optimized for very high speed applications. With its internal feedback and gain-setting resistors, $R_F = R_G = 327\Omega$, the LMH6734 offers excellent AC performance while simplifying board layout and minimizing the effects of layout related parasitic components. The LMH6734 has no internal ground reference so single or split supply configurations are both equally useful.

## SETTING THE CLOSED LOOP GAIN

The LMH6734 can be configured with gain settings of $A_V$ = +2, +1, or −1. Table 1 shows the non-inverting and inverting pin connections to achieve the desired closed loop gain.

**Table 1. Setting the Closed Loop Gain**

| GAIN $A_V$ | INPUT CONNECTIONS | |
|---|---|---|
| | Non-Inverting | Inverting |
| −1 V/V | Ground | Input Signal |
| +1 V/V | Input Signal | NC (Open) |
| +2 V/V | Input Signal | Ground |

## SPLIT SUPPLY APPLICATION

The recommended split supply circuit applications are shown in Figure 35, Figure 36 , and Figure 37. In all three configurations the input signal is DC coupled with a termination resister input $R_{IN}$ = 50Ω. In Figure 35 the inverting input is connected to ground completing the internal feedback loop to set the gain to +2 V/V. In Figure 36 the inverting input is open (no-connect), thus providing a buffer configuration of +1 V/V. Figure 37 shows a buffer configuration with a gain of −1 V/V. In this configuration an input resistor of 59Ω was used to balance the internal $R_G$ resistor of 327Ω and to provide a 50Ω termination.

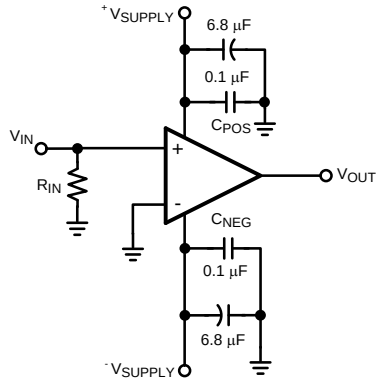


**Figure 35. Recommended Split Supply Non-Inverting Gain Circuit, Gain = +2 V/V**

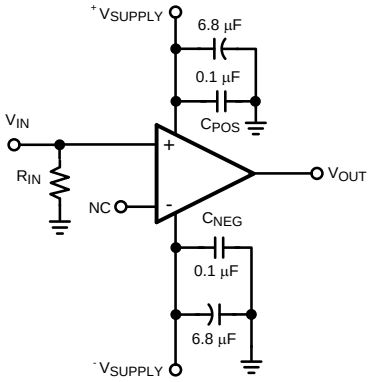


**Figure 36. Recommended Split Supply Non-Inverting Gain Circuit, Gain +1 V/V**

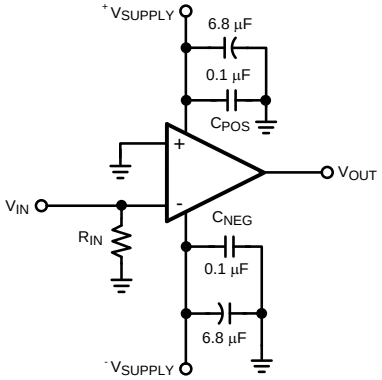


**Figure 37. Recommended Split Supply Inverting Gain Circuit, Gain = –1 V/V**

## SINGLE SUPPLY APPLICATION

The LMH6734 can also be configured for single supply applications as shown in Figure 38, Figure 39, and Figure 40. In Figure 38, the 220 µF capacitor was chosen to satisfy low frequency input signals and to provide an open for the internal feedback network path, thus setting the gain to +1 V/V. With an AC signal present, this 220 µF capacitor is shunted to ground and completes the feedback resistor network to set the AC coupled gain of +2 V/V. The input is AC coupled with the 22 µF capacitor and the two 4.7 kΩ resistors to set the input DC bias voltage. Figure 39 shows the single supply buffer configuration with the inverting input open (no-connect) creating an open to the internal feedback network giving a gain of +1 V/V. The input voltage is AC coupled with the 22 µF capacitor along with two 4.7 kΩ resistors to set the input DC bias voltage. Figure 40 shows the single supply buffer configuration for a gain of −1 V/V. In this circuit, the input signal is DC coupled into the inverting input closing the internal feedback network and creating a gain of −1 V/V while an AC gain of +2 V/V is present at the non-inverting input. Thus, the 6.8 kΩ and the 2.2 kΩ resistors were chosen to set the input DC bias voltage to 1/4 the supply voltage such that at high frequencies the output voltage is gained up by +2 V/V.

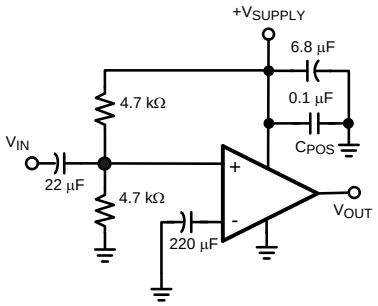


**Figure 38. Recommended Single Supply Non-Inverting Gain Circuit, Gain = +2 V/V**

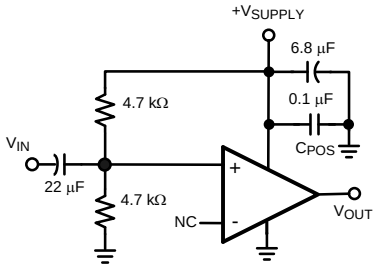


**Figure 39. Recommended Single Supply Non-Inverting Gain Circuit, Gain = +1 V/V**

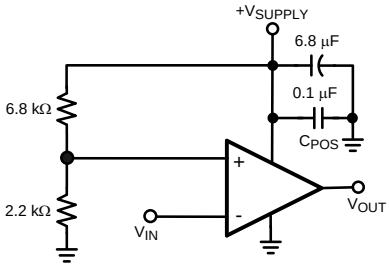


**Figure 40. Recommended Single Supply Inverting Gain Circuit, Gain = −1 V/V**

The gain of the LMH6734 is accurate to ±1% and stable over temperature. The internal gain setting resistors, $R_F$ and $R_G$, match very well. However, over process and temperature their absolute value will change. Using external resistors in series with $R_G$ to change the gain will result in poor gain accuracy over temperature and from part to part.

## UNITY GAIN COMPENSATION

With a current feedback Selectable Gain Buffer like the LMH6734, the feedback resistor is a compromise between the value needed for stability at unity gain and the optimized value used at a gain of two. The result of this compromise is substantial peaking at unity gain. If this peaking is undesirable a simple RC filter at the input of the buffer will smooth the frequency response as shown in Figure 41. Figure 42 shows the results of a simple filter placed on the non-inverting input. See Figure 43 and Figure 44 for another method of reducing unity gain peaking.

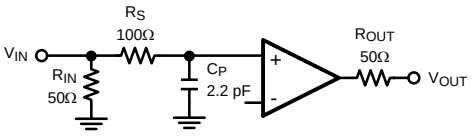


**Figure 41. Correction for Unity Gain Peaking**

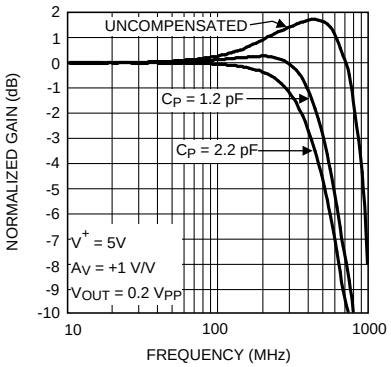


**Figure 42. Frequency Response for Circuit in Figure 41**

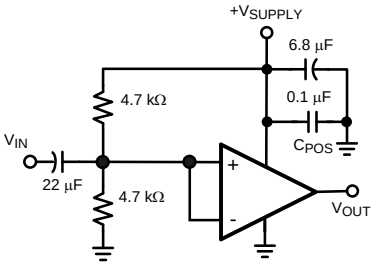


**Figure 43. Alternate Unity Gain Compensation**

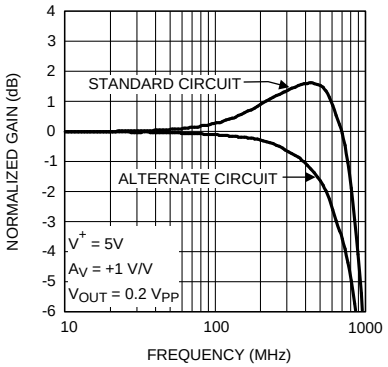


**Figure 44. Frequency Response for Circuit in Figure 43 (Standard Circuit Figure 39)**

## COMPONENT DRIVER

The LMH6734 is capable of transmitting and receiving component video over short to moderate unshielded twisted-pair (UTP) CAT5 cables, as shown in Figure 45. The component signals Y, Pb, and Pr are connected to the LMH6734 transmit side inputs with a 75Ω termination. The LMH6734 transmit amplifiers are configured for a gain of +2 V/V before driving the CAT5 cable. Only three out of the four pairs in the standard CAT5 are utilized, the fourth pair is available for audio. The output of the LMH6734 transmit amplifier drives a 50Ω transmission system with one side of the twisted pair terminated 50Ω to ground. Note this system, without signal equalization, will satisfy transmission up to 200 ft. For longer cable lengths, frequency and gain equalization to compensate for signal degradation is recommended.

The LMH6734 receive side is configured for a unity gain buffer for the component signals received through the CAT5 cable. The inputs of the receiver channels are 100Ω differentially terminated. The two 327Ω external resisters were chosen to match the internal $R_F$ and $R_G$ value of 327Ω. Figure 46, shows the LMH6734 transceiver frequency response over various lengths of CAT5 cable with a 1 $V_{PP}$ input signal at ±5 supply voltage. The CMRR of the LMH6734 receive side at low frequencies is 55 dB at best with a split power supply of ±5V.

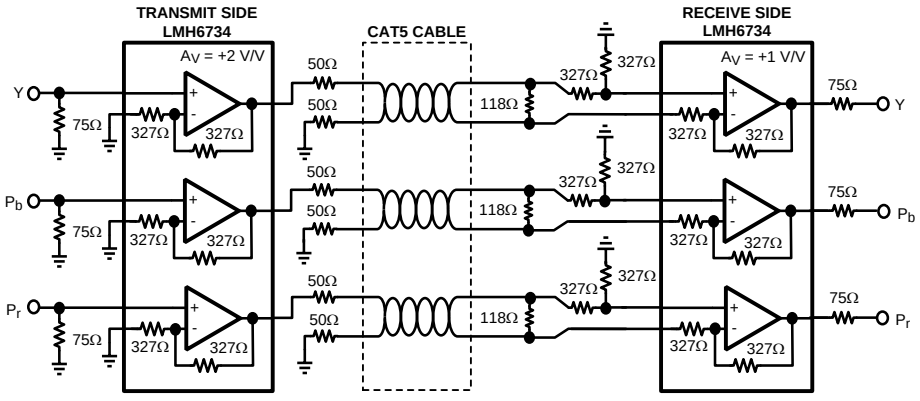


**Figure 45. Component Video Transmission Over UTP (CAT5)**

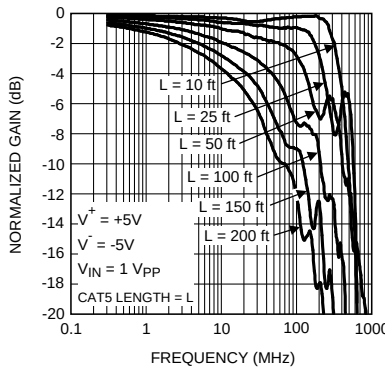


**Figure 46. Frequency Response vs. Normalized Gain and CAT5 Cable Length**

## DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor $R_{OUT}$. Figure 47 shows the use of a series output resistor, $R_{OUT}$, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The charts "Suggested $R_{OUT}$ vs. Cap Load" give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of $R_{OUT}$ can be reduced slightly from the recommended values.

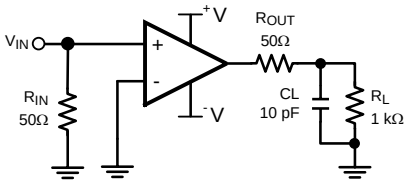


**Figure 47. Decoupling Capacitive Loads**

## LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board supplied with samples of the LMH6734.

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6734 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In Figure 35, Figure 36, and Figure 37 it is recommended an optional capacitor, $C_{SS}$= 0.01 µF, be connected between the split supplies for best second harmonic distortion. Another option to using $C_{SS}$ is to use pairs of 0.01 µF and 0.1 µF ceramic capacitors for each supply bypass.

## VIDEO PERFORMANCE

The LMH6734 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 41 shows a typical configuration for driving a 75Ω cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in $R_{OUT}$.

## POWER DISSIPATION

The LMH6734 is optimized for maximum speed and performance in the small form factor of the standard 16-Pin SSOP package. To achieve its high level of performance, the LMH6734 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used ($V_S$ = ±5V, all three channels on). Therefore, it is easy to see the need for proper precautions in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the $T_{JMAX}$ is never exceeded due to the overall power dissipation (all three channels).

With the LMH6734 used in a back-terminated 75Ω RGB analog video system (with 2 $V_{PP}$ output voltage), the total power dissipation is around 305 mW of which 220 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, the junction temperature rises to about 120°C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the 16-Pin SSOP package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the 16-Pin SSOP package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the maximum power dissipation for the LMH6734:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC} \times (V_S)$ $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage:
   - $P_D$ (rms) = rms $((V_S - V_{OUT}) \times I_{OUT})$ where $V_{OUT}$ and $I_{OUT}$ are the voltage and current across the external load and $V_S$ is the total supply current
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$

The maximum power that the LMH6734 package can dissipate at a given temperature (See Figure 48) can be derived with the following equation:

$P_{MAX} = (150° C/W - T_{AMB})/ \theta_{JA}$, where $T_{AMB}$ = Ambient temperature (°C) and $\theta_{JA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SSOP package $\theta_{JA}$ is 120°C/W.

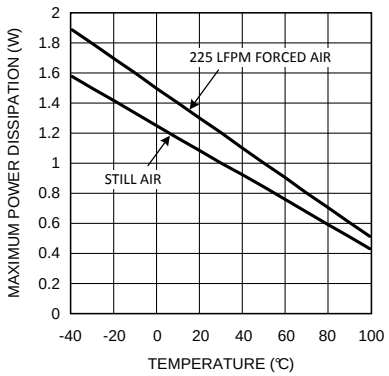


**Figure 48. Maximum Power Dissipation**

## ESD PROTECTION

The LMH6734 is protected against electrostatic discharge (ESD) on all pins. The LMH6734 will survive 2000V Human Body Model and 200V Machine Model events.

Under closed loop operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6734 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

## EVALUATION BOARDS

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

| Device | Package | Evaluation Board Part Number |
|---|---|---|
| LMH6734MQ | SSOP | LMH730275 |

A bare evaluation board can be ordered when a sample request is placed with Texas Instruments.

## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 19 |

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