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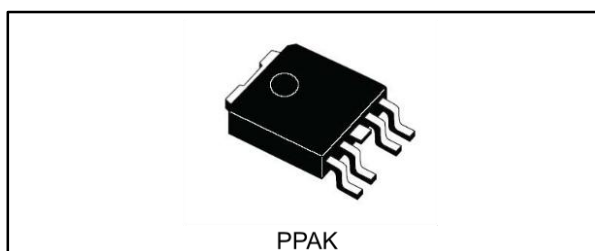
sales@integrated-circuit.com



VN751PT

High-side driver

Datasheet - production data



Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN751PT	60 mΩ	2.5 A	36 V

- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output

Description

The VN751PT is a monolithic device developed using STMicroelectronics' VIPower M03 technology, intended to drive any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controller international standard.

Table 1: Device summary

Order code	Package	Packing
VN751PT	PPAK	Tube
VN751PTTR		Tape and reel

Contents

1	Block diagram.....	5
2	Pin connection.....	6
3	Maximum ratings	7
4	Electrical characteristics	8
5	Test circuits	10
6	Switching time waveforms and truth table	11
7	Application schematic	13
8	Reverse polarity protection	14
9	Package information	15
	9.1 PPAK package information	16
	9.2 PPAK packing information	18
10	Revision history	20

List of tables

Table 1: Device summary	1
Table 2: Absolute maximum ratings	7
Table 3: Thermal data.....	7
Table 4: Power.....	8
Table 5: Switching ($V_{CC} = 24\text{ V}$).....	8
Table 6: Input pin	9
Table 7: Status pin	9
Table 8: Protection.....	9
Table 9: Truth table.....	11
Table 10: PPAK mechanical data	17
Table 11: PPAK tape and reel mechanical data	19
Table 12: Document revision history	20

List of figures

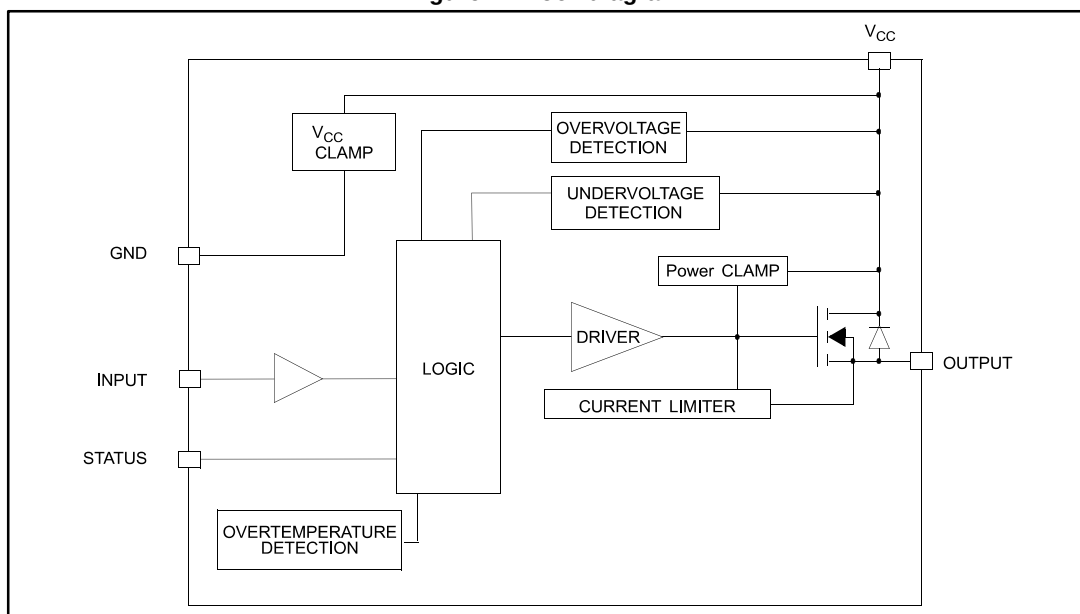
VN751PT

List of figures

Figure 1: Block diagram	5
Figure 2: Connection diagram (top view)	6
Figure 3: Current and voltage conventions	6
Figure 4: Peak short-circuit current	10
Figure 5: Avalanche energy test circuit	10
Figure 6: Switching time waveforms	11
Figure 7: Waveforms	12
Figure 8: Application schematic	13
Figure 9: Reverse polarity protection	14
Figure 10: PPAK package outline	16
Figure 11: PPAK tape outline	18
Figure 12: PPAK reel outline	19

1 Block diagram

Figure 1: Block diagram



2 Pin connection

Figure 2: Connection diagram (top view)

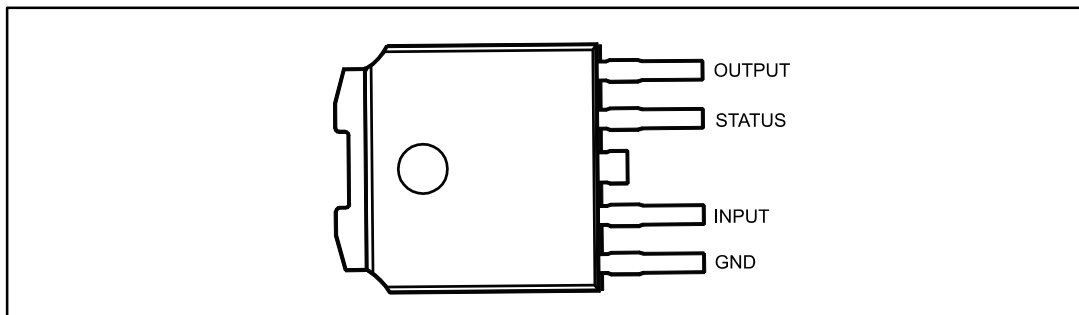
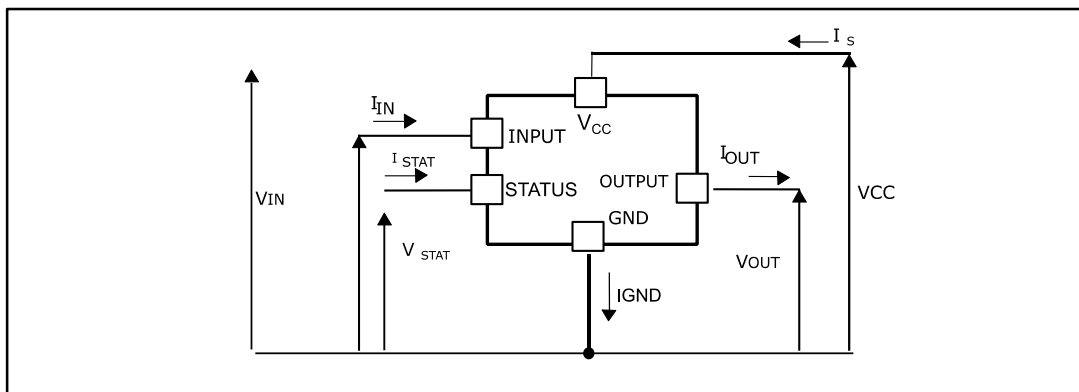


Figure 3: Current and voltage conventions



3 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Power supply voltage	45	V
-V _{CC}	Reverse supply voltage	-0.3	V
-I _{GND}	DC reverse ground pin current	-200	mA
I _{OUT}	DC output current	Internally limited	A
-I _{OUT}	Reverse DC output current	-5	A
I _{IN}	DC input current	-1 to +10	mA
I _{STAT}	DC status current	-1 to +10	mA
V _{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	5000	V
E _{AS}	Single pulse avalanche energy	0.8	J
P _{TOT}	Power dissipation at T _C = 25 °C	Internally limited	W
T _J	Junction operating temperature	Internally limited	°C
T _C	Case operating temperature	-40 to 150	°C
T _{STG}	Storage temperature	-55 to 150	°C

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{th(JC)}	Thermal resistance junction-case	Max. 3	°C/W
R _{th(JA)}	Thermal resistance junction-ambient	Max. 50 ⁽¹⁾	°C/W

Notes:

⁽¹⁾When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35 μm) thick connected to all VCC pins.

Electrical characteristics

VN751PT

4 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 4: Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage		5.5		36	V
R _{DS(on)}	On-state resistance	I _{OUT} = 2 A at T _J = 25 °C		60		mΩ
		I _{OUT} = 2 A			180	
I _S ⁽¹⁾	Supply current	OFF-state, V _{CC} = 24 V, T _J = 25 °C,		10	20	μA
		ON-state, V _{CC} = 24 V, T _J = 25 °C,		3.5		mA
		ON-state, V _{CC} = 24 V, T _J = 100 °C			3.8	mA
V _{USD}	Undervoltage shutdown		3	4	5.5	V
V _{OV}	Overvoltage shutdown		36			V
I _{L(off)}	Off-state output current	V _{IN} = V _{OUT} = 0 V	0		10	μA

Notes:

⁽¹⁾Status: floating

Table 5: Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(ON)}	Turn-on delay time	R _L = 12 Ω from V _{IN} rising edge to V _{OUT} = 2.4 V		12		μs
t _{d(OFF)}	Turn-on delay time of output current	R _L = 12 Ω from V _{IN} falling edge to V _{OUT} = 21.6 V		35		μs
dV _{OUT} /dt _(on)	Turn -on voltage slope	R _L = 12 Ω from V _{OUT} = 2.4 V to V _{OUT} = 19.2 V		0.80		V/μs
dV _{OUT} /dt _(off)	Turn -off voltage slope	R _L = 12 Ω from V _{OUT} = 21.6 V to V _{OUT} = 2.4 V		0.30		

VN751PT

Electrical characteristics

Table 6: Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25\text{ V}$	1			μA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25\text{ V}$			10	μA
$V_{I(HYST)}$	Input hysteresis voltage		0.5			V
I_{IN}	Input current	$V_{IN} = V_{CC} = 5\text{ V}$			10	μA
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$		-0.7		

Table 7: Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1\text{ mA}$	6	6.8	8	μA
		$I_{STAT} = -1\text{ mA}$		-0.7		V

Table 8: Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output clamp voltage	$R_L = 12\ \Omega$; $L = 6\text{ mH}$	$V_{CC} - 47$	$V_{CC} - 52$	$V_{CC} - 57$	V
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
I_{lim}	Current limitation	$V_{CC} = 24\text{ V}$; $R_{LOAD} = 10\text{ m}\Omega$, $t = 0.4\text{ ms}$	2.7		6.0	A
T_{hyst}	Thermal hysteresis		7	20		$^{\circ}\text{C}$
T_R	Reset temperature		135			$^{\circ}\text{C}$

5 Test circuits

Figure 4: Peak short-circuit current

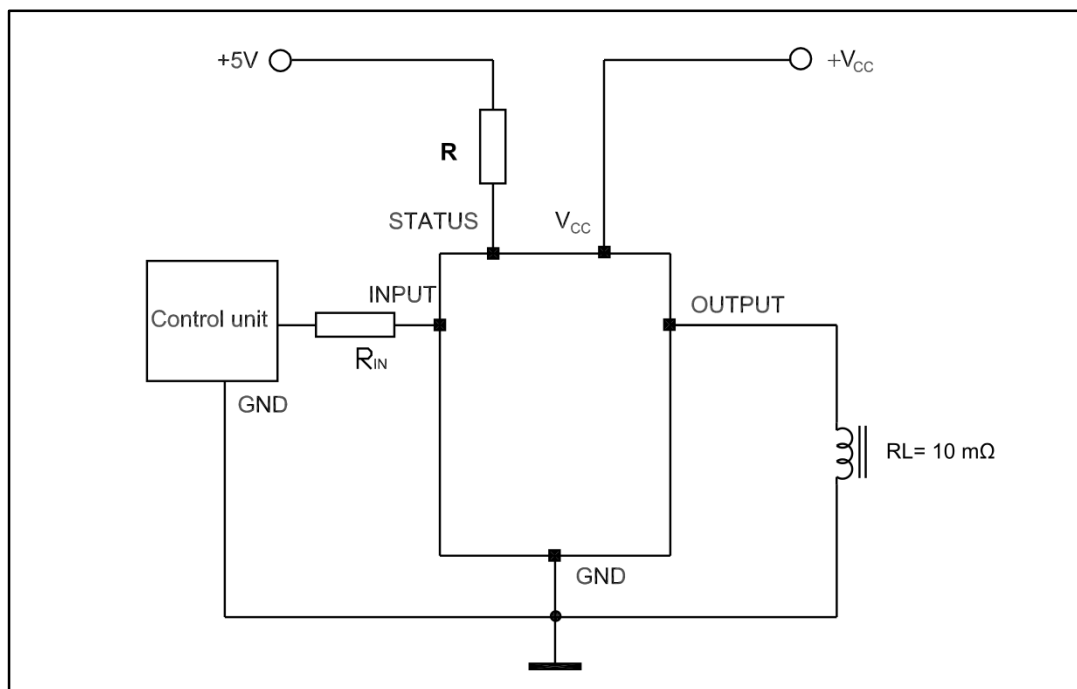
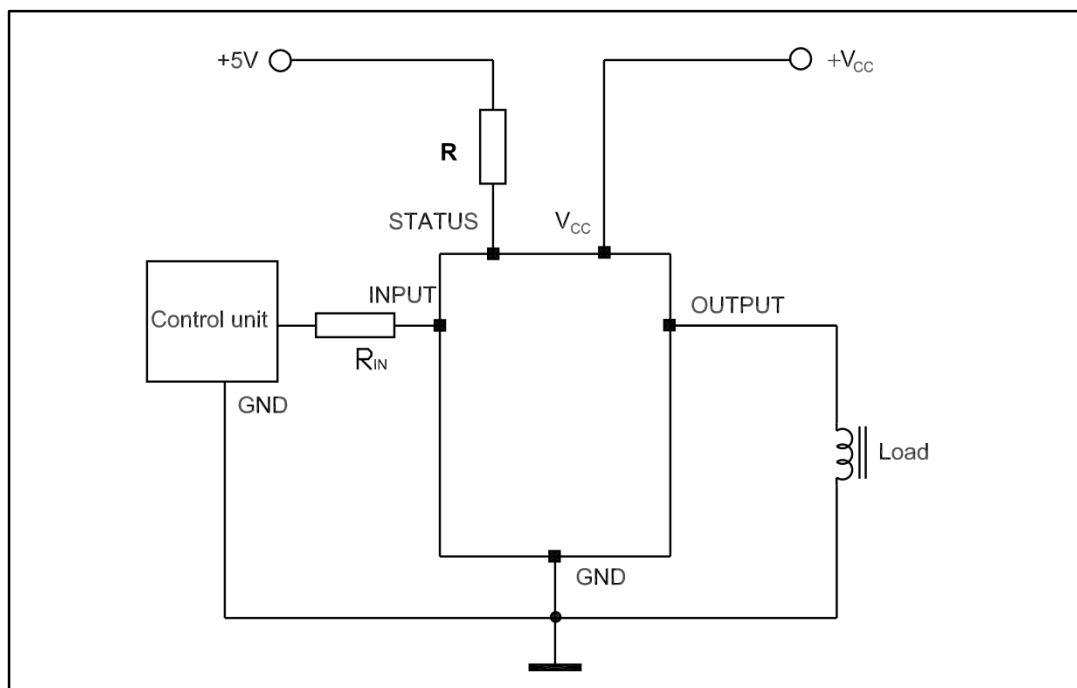


Figure 5: Avalanche energy test circuit



6 Switching time waveforms and truth table

Figure 6: Switching time waveforms

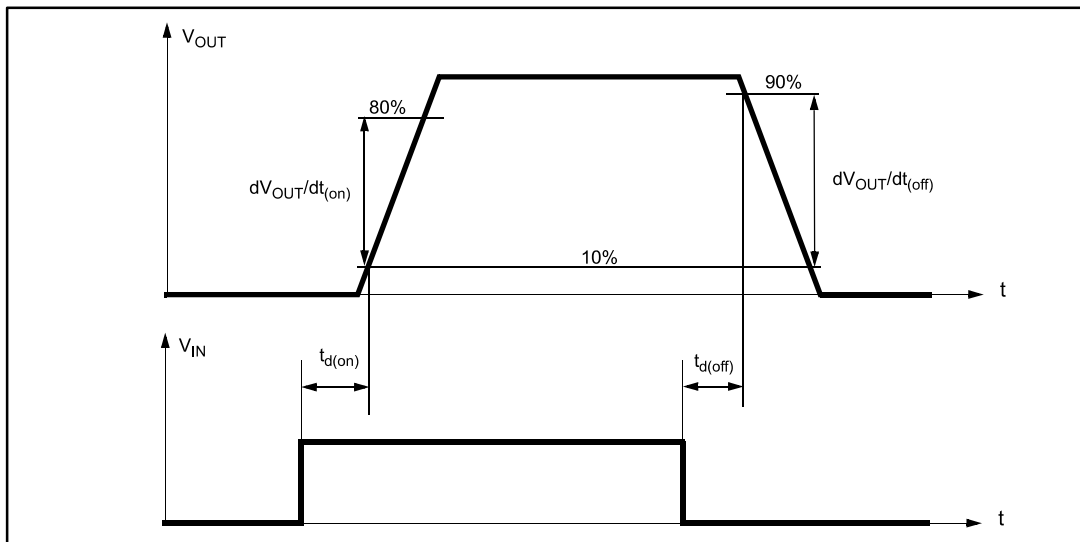


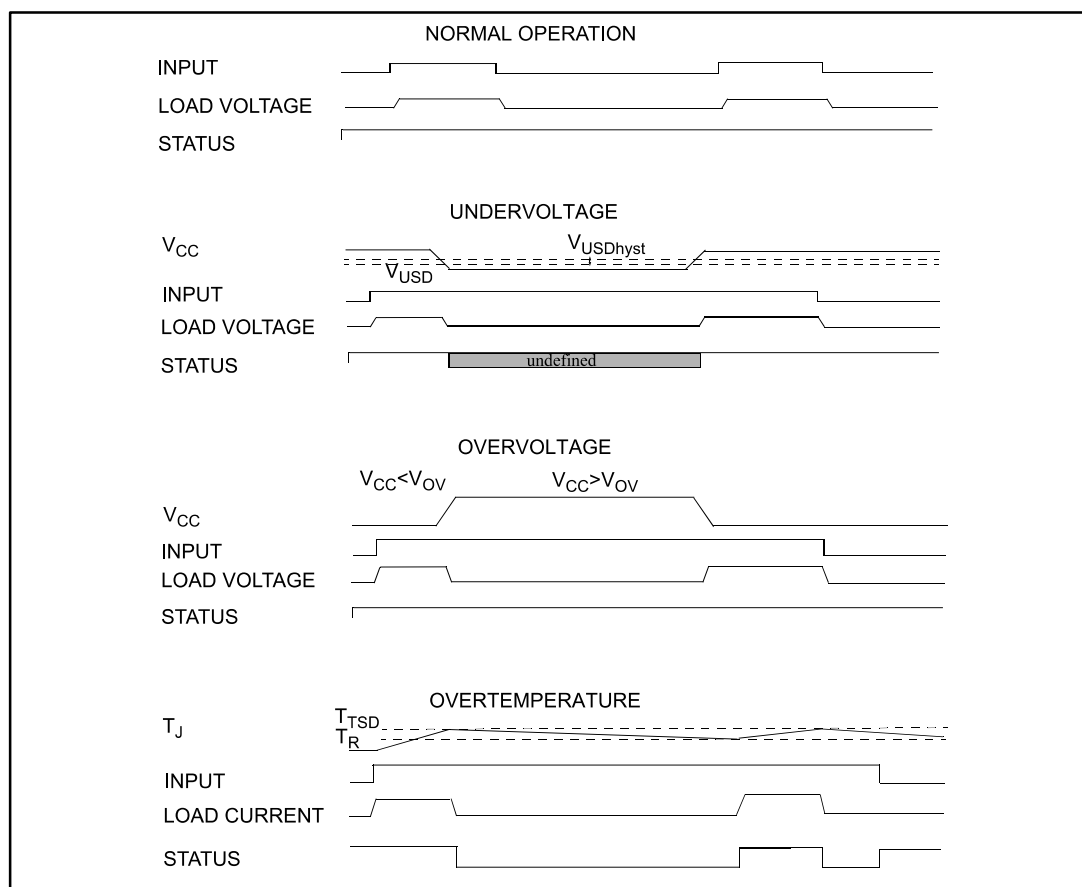
Table 9: Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_J < T_{TSD})H$
	H	X	$(T_J > T_{TSD})L$
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Switching time waveforms and truth table

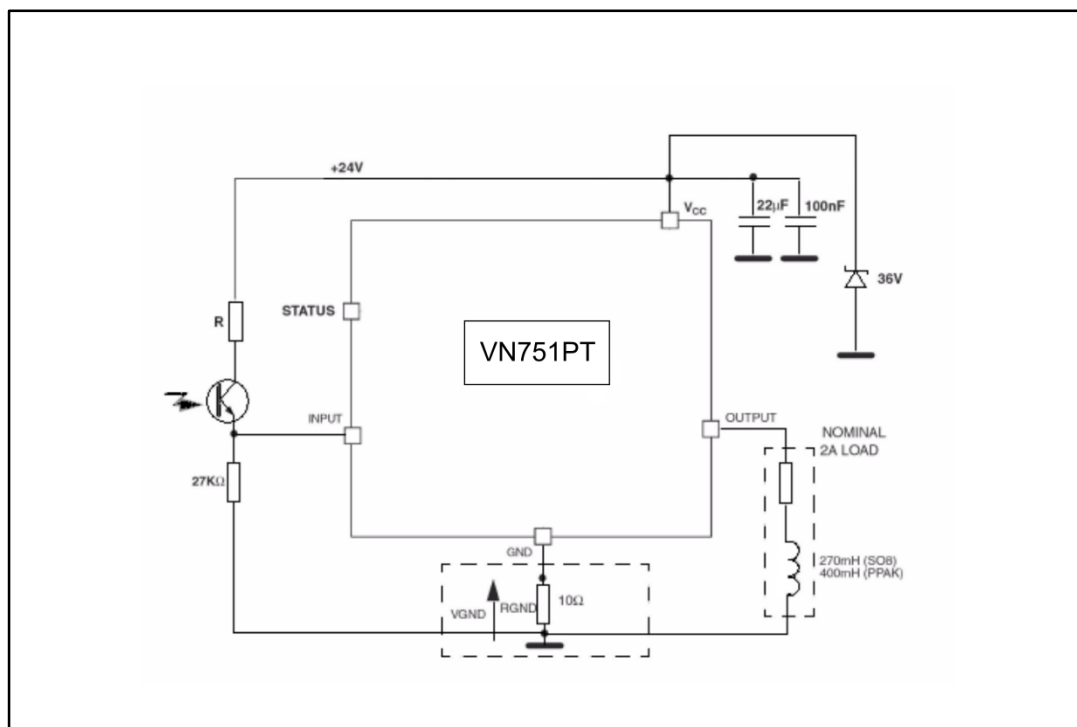
VN751PT

Figure 7: Waveforms



7 Application schematic

Figure 8: Application schematic



8 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC. The R_{GND} resistor value can be selected according to the following conditions:

Equation 1:

$$R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON-state max.})$$

Equation 2:

$$R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

The power dissipation associated to R_{GND} during reverse polarity condition is:

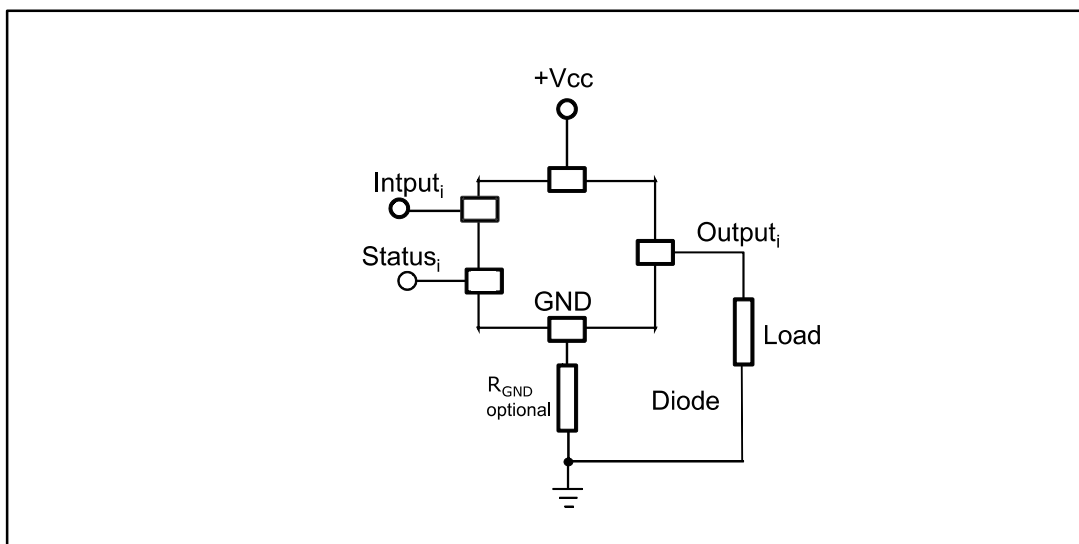
Equation 3:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by several different ICs.

In such case I_S value in equation 1 is the sum of the maximum ON-state currents of the different devices. Please note that if the microprocessor ground and the device ground are separated, the voltage drop across the R_{GND} (given by I_S in ON-state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in case of several high-side switches sharing the same R_{GND} .

Figure 9: Reverse polarity protection



9 Package information

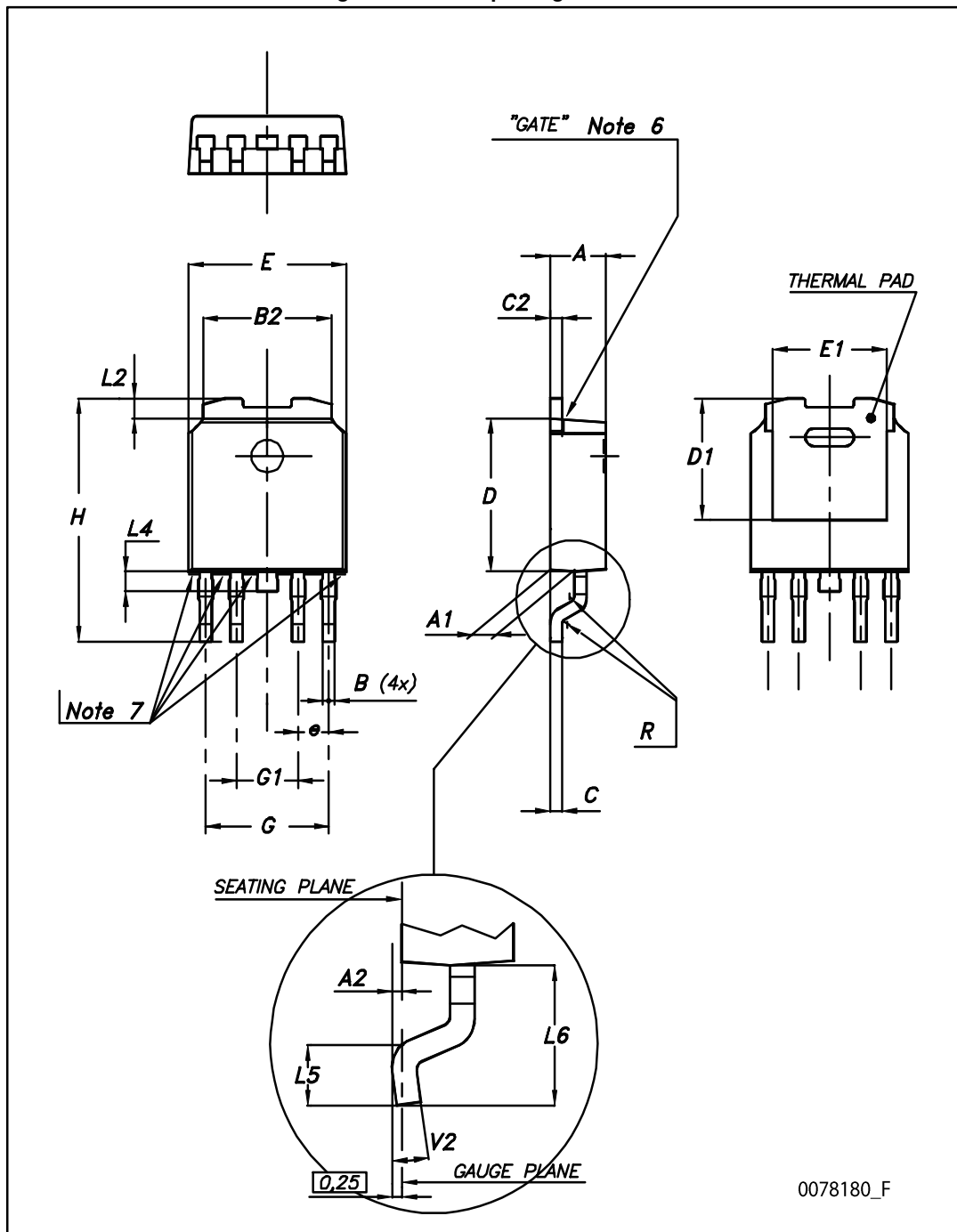
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Package information

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9.1 PPAK package information

Figure 10: PPAK package outline



VN751PT

Package information

Table 10: PPAK mechanical data

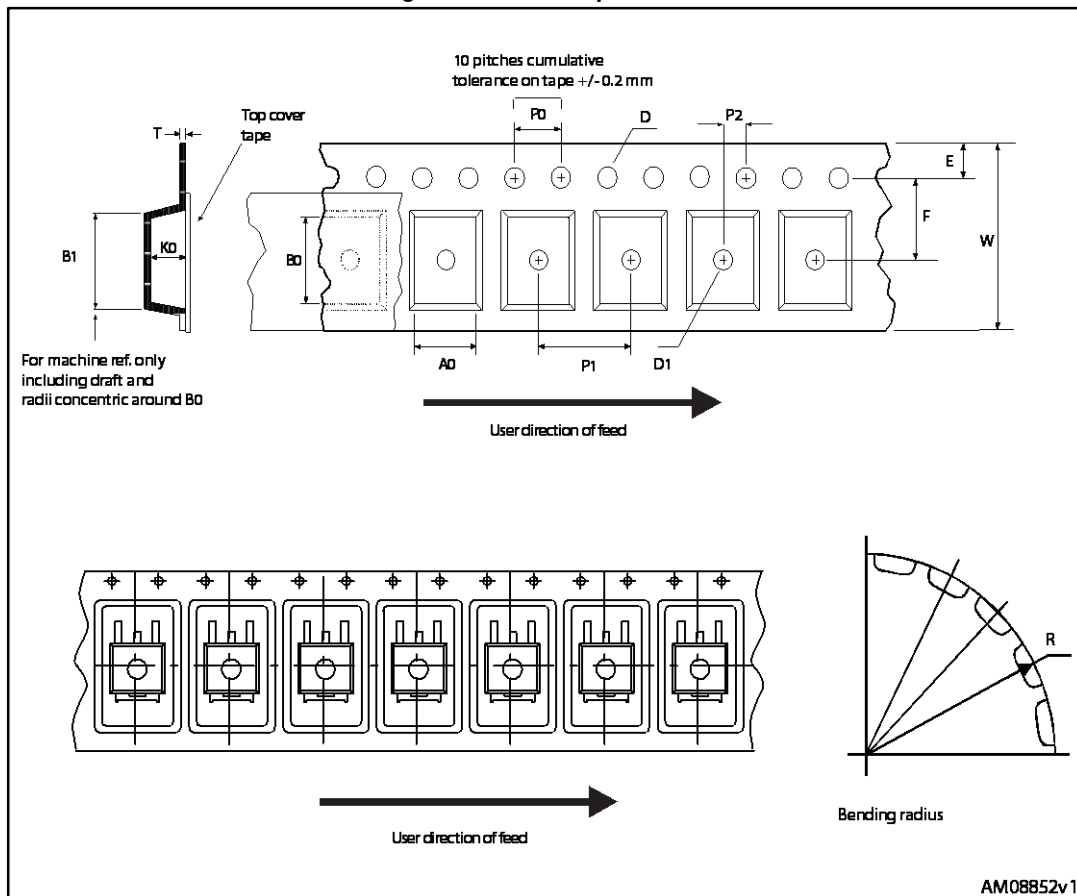
Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

Package information

VN751PT

9.2 PPAK packing information

Figure 11: PPAK tape outline



VN751PT

Package information

Figure 12: PPAK reel outline

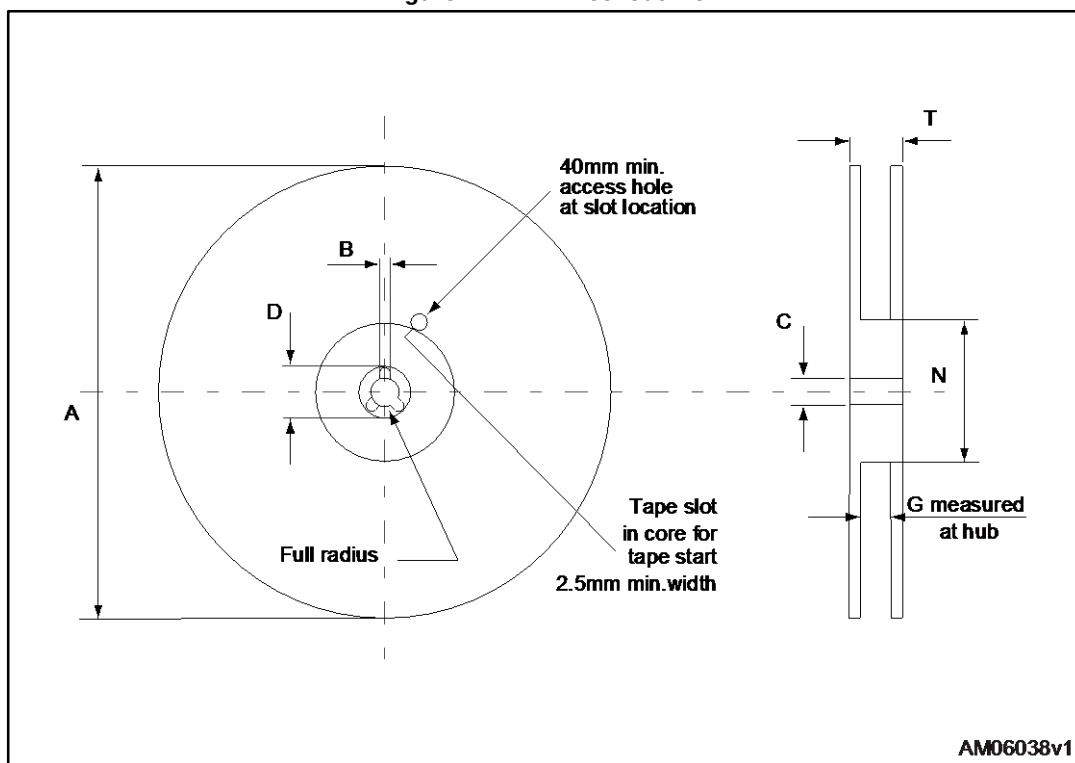


Table 11: PPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

10 Revision history

Table 12: Document revision history

Date	Revision	Changes
07-Mar-2006	1	Initial release.
31-Mar-2006	2	Added V_{SCL} .
10-Jul-2006	3	Updated V_{CC} value <i>table 1</i> , I_{lim} min. value <i>table 7</i> .
12-Mar-2007	4	Typo in <i>table 4</i> , updated P_{tot} value <i>table 1</i> .
15-May-2007	5	Typo in <i>table 1</i> , V_{ESD} .
18-Sep-2007	6	Added I_{STAT} value in <i>table 1</i> .
08-Jul-2008	7	Added <i>section 7</i> .
30-Nov-2009	8	Updated cover page and <i>section 6</i> .
12-Jul-2016	9	Updated <i>Table 4: "Power"</i> .

VN751PT

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