

# **Excellent Integrated System Limited**

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Vishay/Siliconix SI3981DV-T1-E3

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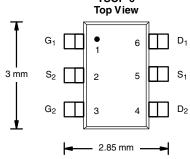
### Si3981DV

Vishay Siliconix

## Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)		
- 20	0.185 at V <sub>GS</sub> = - 4.5 V	- 1.9		
	0.260 at V <sub>GS</sub> = - 2.5 V	- 1.6		
	0.385 at V <sub>GS</sub> = - 1.8 V	- 0.7		

# TSOP-6 Top View



Ordering Information: Si3981DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

MCxxx Marking Code:

#### **FEATURES**

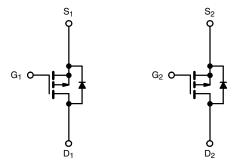
- TrenchFET® Power MOSFET
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



HALOGEN FREE

#### **APPLICATIONS**

- Battery Switch for Portable Devices
- Computers
  - Bus Switch
  - Load Switch



P-Channel MOSFET

P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter		Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 20		V	
Gate-Source Voltage		V <sub>GS</sub>	± 8			
Continuous Drain Current /T = 150 °C)8	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 1.9	- 1.6	A	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		- 1.5	- 1.3		
Pulsed Drain Current		I <sub>DM</sub>	- 8			
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 1	- 0.72		
Mayiraum Daway Dissination	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	1.08	0.80	- W	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		0.69	0.51		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 5 s	R <sub>thJA</sub>	97	115	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	¹ ¹thJA	132	155		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	78	95		

a. Surface mounted on 1" x 1" FR4 board.

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Datasheet of SI3981DV-T1-E3 - MOSFET 2P-CH 20V 1.6A 6-TSOP

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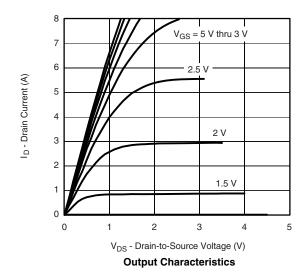
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.40		- 1.1	٧	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	^	
		$V_{DS}$ = - 20 V, $V_{GS}$ = 0 V, $T_{J}$ = 85 °C			- 10	μΑ	
On-State Drain Current <sup>a</sup>	State Drain Current <sup>a</sup> $I_{D(on)}$ $V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$		- 5			Α	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = -4.5 \text{ V}, I_D = -1.9 \text{ A}$		0.146	0.185		
	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1.6 A		0.210	0.260	Ω	
		$V_{GS} = -1.8 \text{ V}, I_D = -0.7 \text{ A}$		0.306	0.385		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 5 V, I <sub>D</sub> = - 1.9 A		4		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = - 1 A, V <sub>GS</sub> = 0 V		- 0.84	- 1.1	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg			3.2	5		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -1.9 \text{ A}$		0.42		nC	
Gate-Drain Charge	Q <sub>gd</sub>			0.84			
Gate Resistance			6		Ω		
Turn-On Delay Time	t <sub>d(on)</sub>			30	45		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 10 $\Omega$		50	85		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 6 $\Omega$		45	85	ns	
Fall Time	t <sub>f</sub>			21	50		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 1 A, dl/dt = 100 A/μs		20	40		

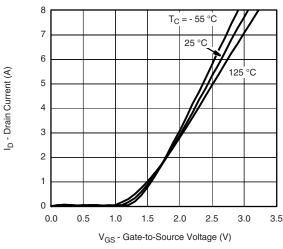
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





**Transfer Characteristics** 

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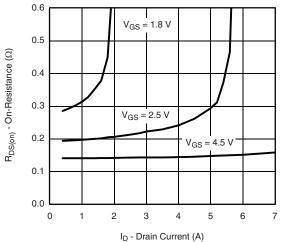
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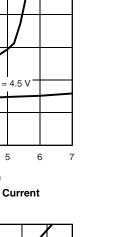
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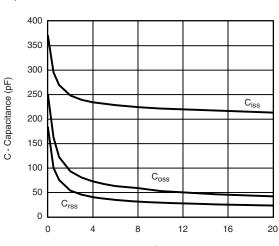
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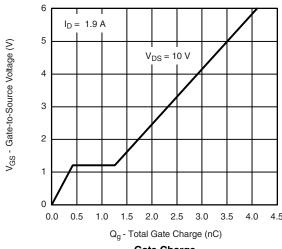


#### On-Resistance vs. Drain Current

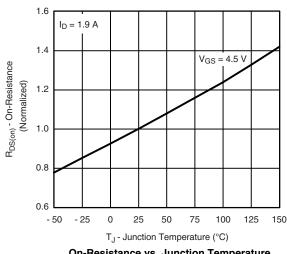




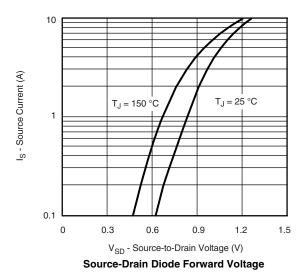
V<sub>DS</sub> - Drain-to-Source Voltage (V) Capacitance

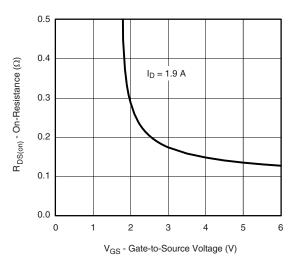


**Gate Charge** 



On-Resistance vs. Junction Temperature





On-Resistance vs. Gate-to-Source Voltage

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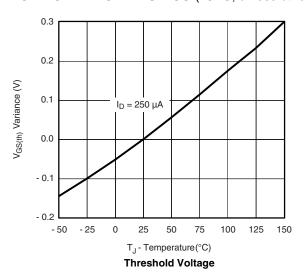


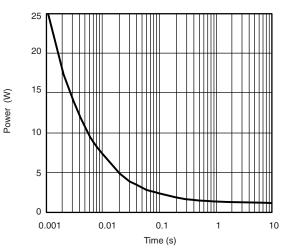
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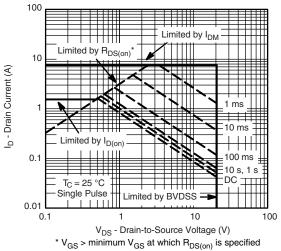
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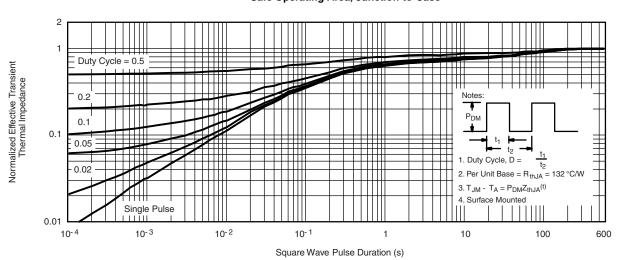




Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

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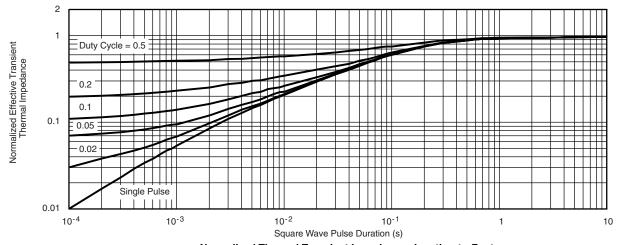
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#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72502

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