

Excellent Integrated System Limited

Stocking Distributor

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Vishay/Siliconix SI4470EY-T1-E3

For any questions, you can email us directly: <u>sales@integrated-circuit.com</u>



Distributor of Vishay/Siliconix: Excellent Integrated System Limited Datasheet of SI4470EY-T1-E3 - MOSFET N-CH 60V 9A 8-SOIC Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com



Si4470EY

Vishay Siliconix

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)			
60	0.011 at V _{GS} = 10 V	12.7			
	0.013 at V _{GS} = 6.0 V	11.7			

FEATURES

Halogen-free According to IEC 61249-2-21
Definition

D

N-Channel MOSFET

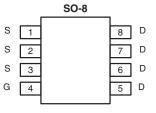
- TrenchFET[®] Power MOSFETs
- 175 °C Maximum Junction Temperature
- Compliant to RoHS Directive 2002/95/EC

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APPLICATIONS

• Primary Side Switch





Top View

Ordering Information: Si4470EY-T1-E3 (Lead (Pb)-free) Si4470EY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unle	ess otherwise	noted)			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	60		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Drain Querent (T. 150 °C)	T _A = 25 °C	- I _D	12.7	9.0		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		10.6	7.5		
Pulsed Drain Current		I _{DM}	50		А	
Avalanche Current	L = 0.1 mH	I _{AS}	50			
Continuous Source Current (Diode Conduction) ^a		۱ _S	3.1	1.5		
	T _A = 25 °C	– P _D	3.75	1.85	W	
Maximum Power Dissipation ^a	T _A = 70 °C		2.6	1.3	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana hartiga ta Archigata	t ≤ 10 s	R _{thJA}	33	40	
Maximum Junction-to-Ambient ^a	Steady State		65	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

a. Surface mounted on 1" x 1" FR4 board.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2.0			V			
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA			
Zara Cata Valtaga Drain Current	1	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			1				
Zero Gate Voltage Drain Current	IDSS			5	μΑ				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5$ V, V_{GS} = 10 V	50			А			
	D	V _{GS} = 10 V, I _D = 12 A	= 12 A		0.011	Ω			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 6.0 V, I _D = 10 A		0.0105	0.013				
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A		50		S			
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S} = 3.0$ A, $V_{\rm GS} = 0$ V		0.75	1.2	V			
Dynamic ^b									
Total Gate Charge	Qg			46	70				
Gate-Source Charge	Q _{gs}	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 12 A		11.5		nC			
Gate-Drain Charge	Q _{gd}			11.5					
Gate Resistance	Rg		0.25	0.85	1.4	Ω			
Turn-On Delay Time	t _{d(on)}			16	25				
Rise Time	t _r	V_{DD} = 30 V, R_L = 30 Ω		12	18				
Turn-Off Delay Time	t _{d(off)}	$\rm I_D \cong 1.0$ A, $\rm V_{GEN}$ = 10 V, $\rm R_g$ = 6 Ω		50	75	ns			
Fall Time	t _f			30	45				
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.0 A, dI/dt = 100 A/μs		40	60				

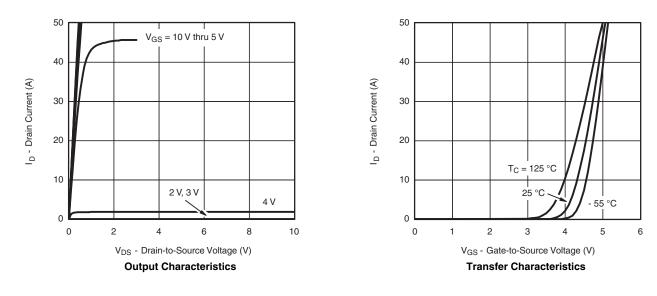
Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





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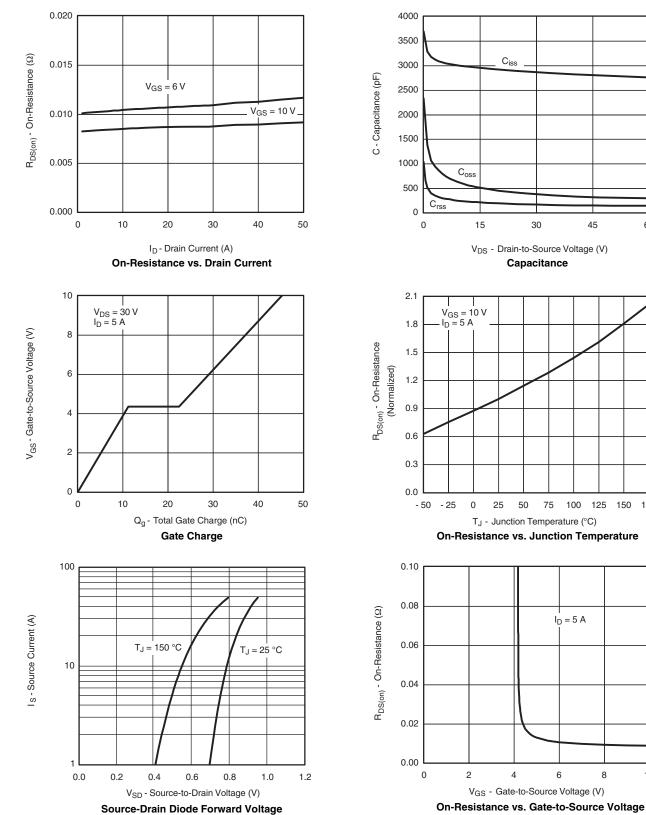


Si4470EY

60

150 175

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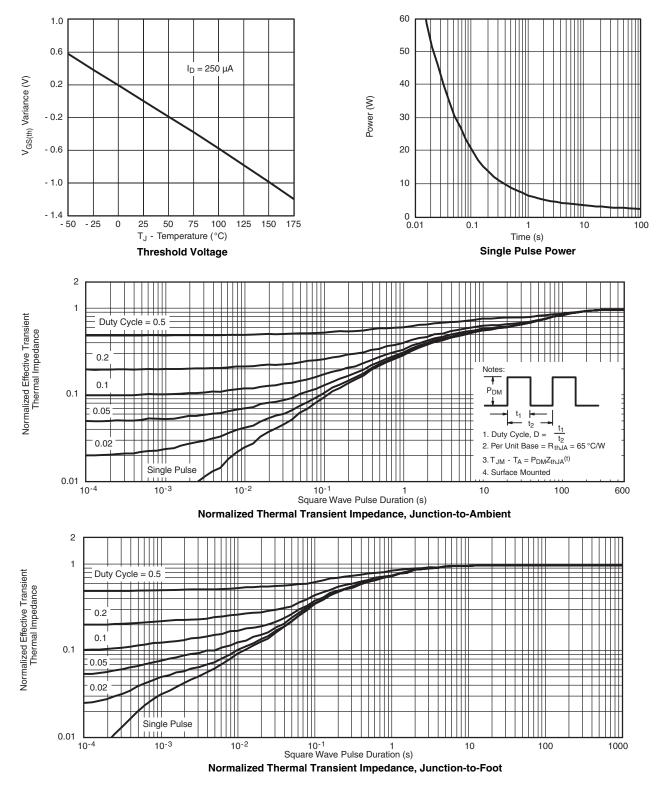
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