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Si5484DU
 Vishay Siliconix

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.016 at V _{GS} = 4.5 V	12	16.5 nC
	0.021 at V _{GS} = 2.5 V	12	

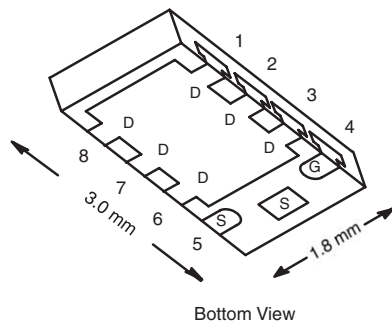
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] ChipFET[®] Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile



RoHS
 COMPLIANT

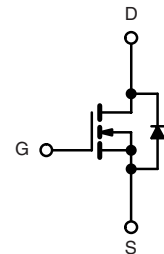
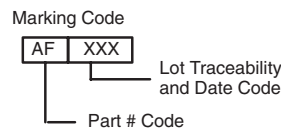
PowerPAK ChipFET Single



Bottom View

APPLICATIONS

- Load Switch, PA Switch, and for Portable Applications



Ordering Information: Si5484DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	12 ^a	A
		T _C = 70 °C	12 ^a	
		T _A = 25 °C	11.4 ^{b, c}	
		T _A = 70 °C	9.1 ^{b, c}	
Pulsed Drain Current	I _{DM}	40		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	12 ^a	
		T _A = 25 °C	2.6 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	31	W
		T _C = 70 °C	20	
		T _A = 25 °C	3.1 ^{b, c}	
		T _A = 70 °C	2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	34	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	3	4	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 90 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	20			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		18.5		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-4.4			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		2	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	30			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 7.6\text{ A}$		0.013	0.016	Ω	
		$V_{GS} = 2.5\text{ V}, I_D = 6.6\text{ A}$		0.017	0.021		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 7.6\text{ A}$		37		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1600		pF	
Output Capacitance	C_{oss}			320			
Reverse Transfer Capacitance	C_{rss}			210			
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 11.4\text{ A}$		35.5	55	nC	
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 11.4\text{ A}$	Q_{gs}		16.5		25
Gate-Source Charge	Q_{gs}			3.5			
Gate-Drain Charge	Q_{gd}			4			
Gate Resistance	R_g	$f = 1\text{ MHz}$		4.5		Ω	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 9.1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns	
Rise Time	t_r			30	45		
Turn-Off Delay Time	$t_{d(off)}$			30	45		
Fall Time	t_f			10	15		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 9.3\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10		
Rise Time	t_r			15	25		
Turn-Off Delay Time	$t_{d(off)}$			35	55		
Fall Time	t_f			10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			12	A	
Pulse Diode Forward Current	I_{SM}				40		
Body Diode Voltage	V_{SD}	$I_S = 9.1\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 9.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns	
Body Diode Reverse Recovery Charge	Q_{rr}				15	30	nC
Reverse Recovery Fall Time	t_a				12		ns
Reverse Recovery Rise Time	t_b				18		

Notes:

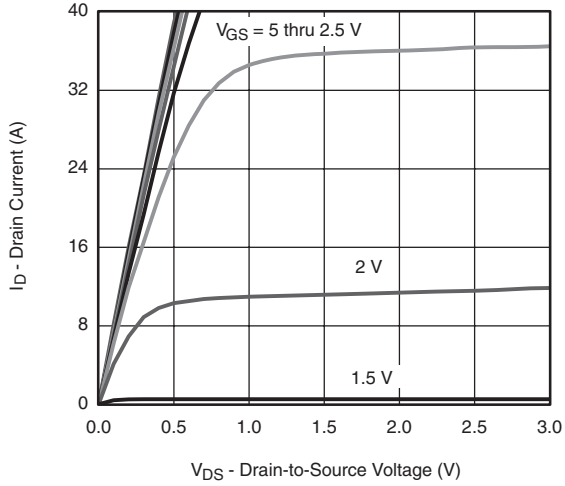
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

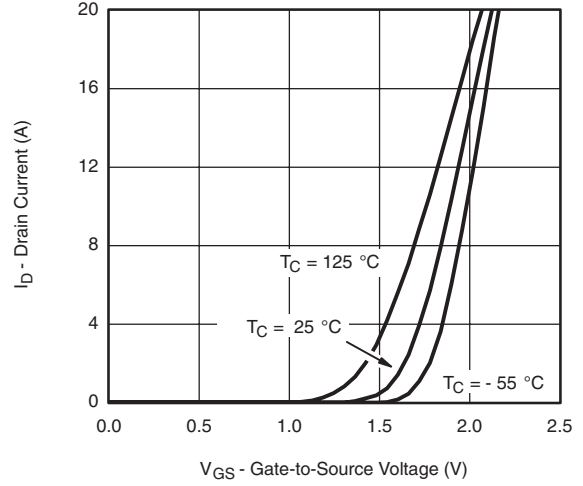


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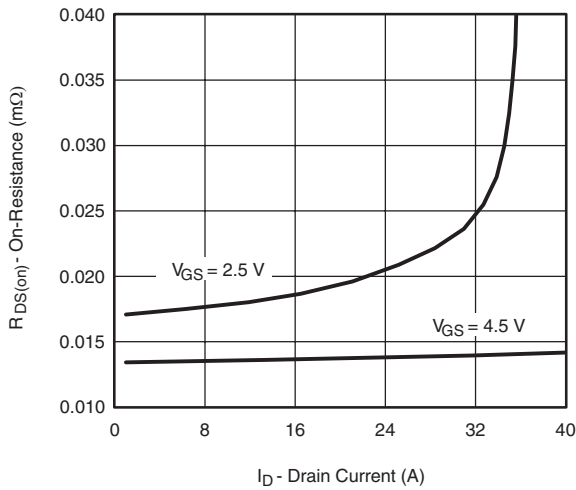
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



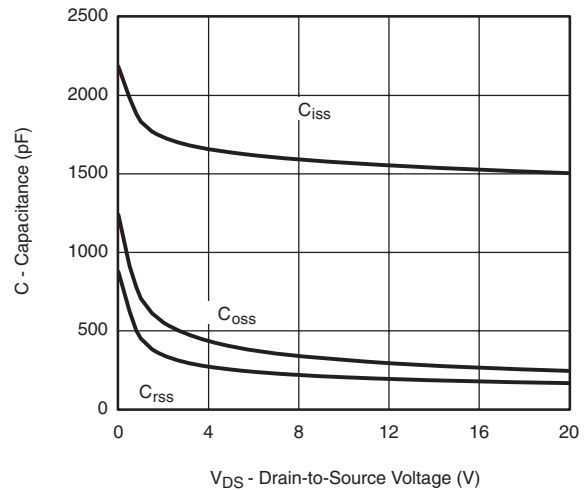
Output Characteristics



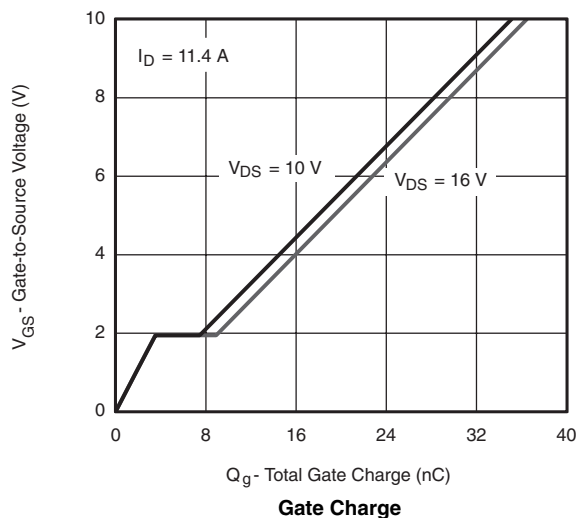
Transfer Characteristics



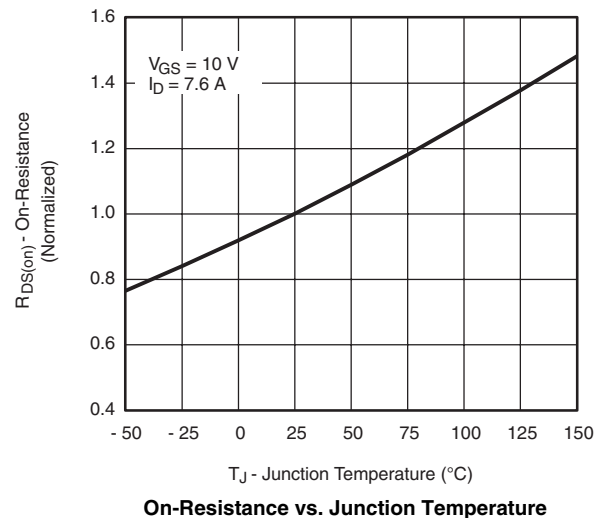
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



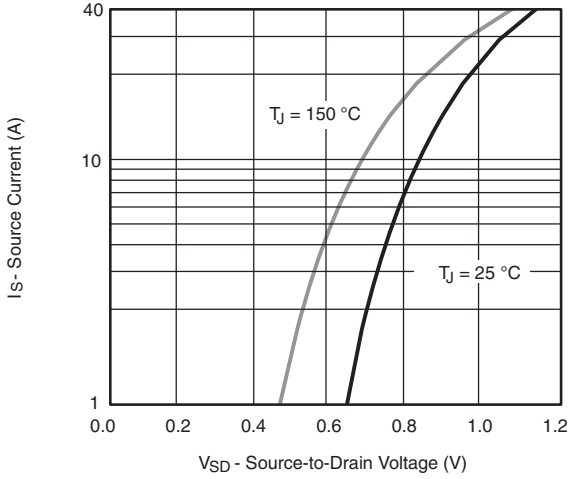
On-Resistance vs. Junction Temperature

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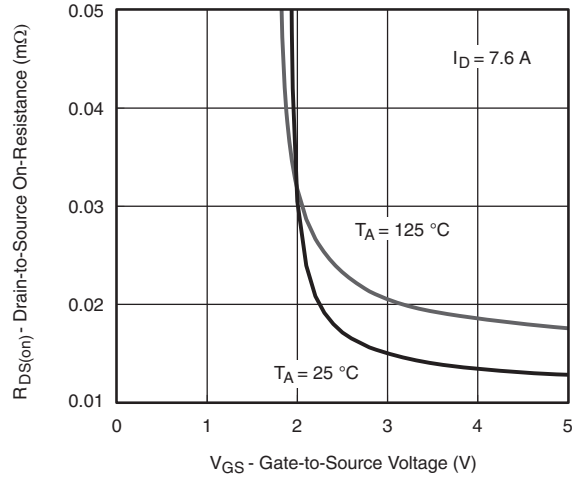
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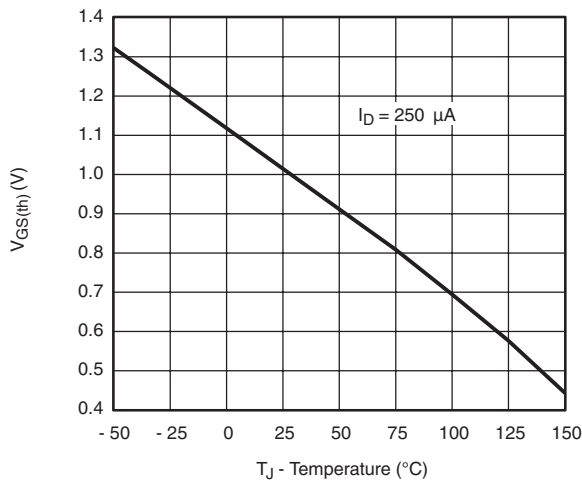
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



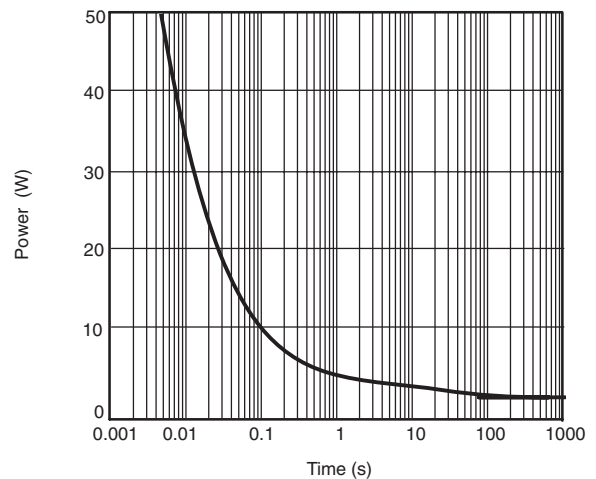
Source-Drain Diode Forward Voltage



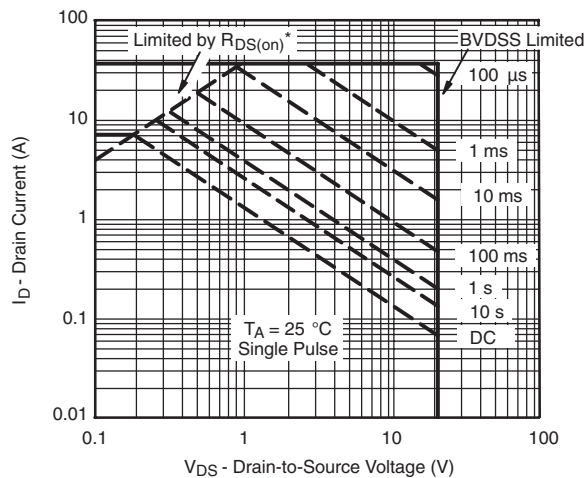
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

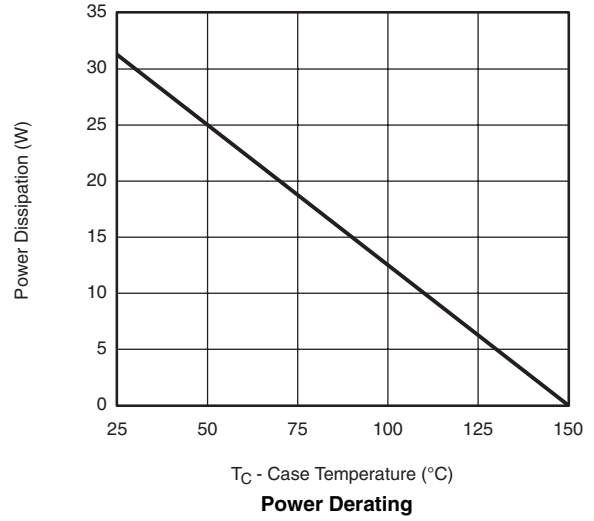
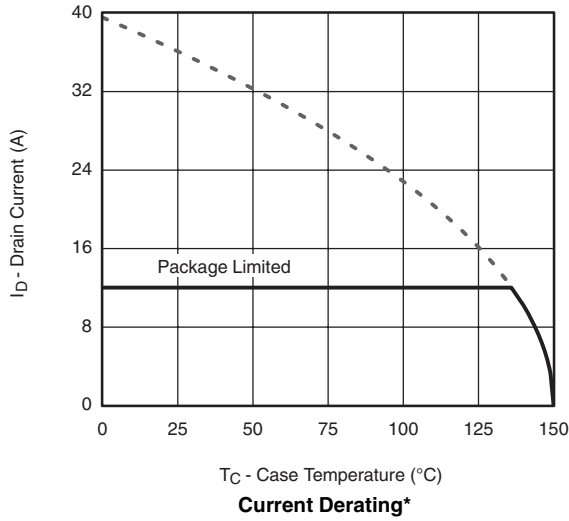


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



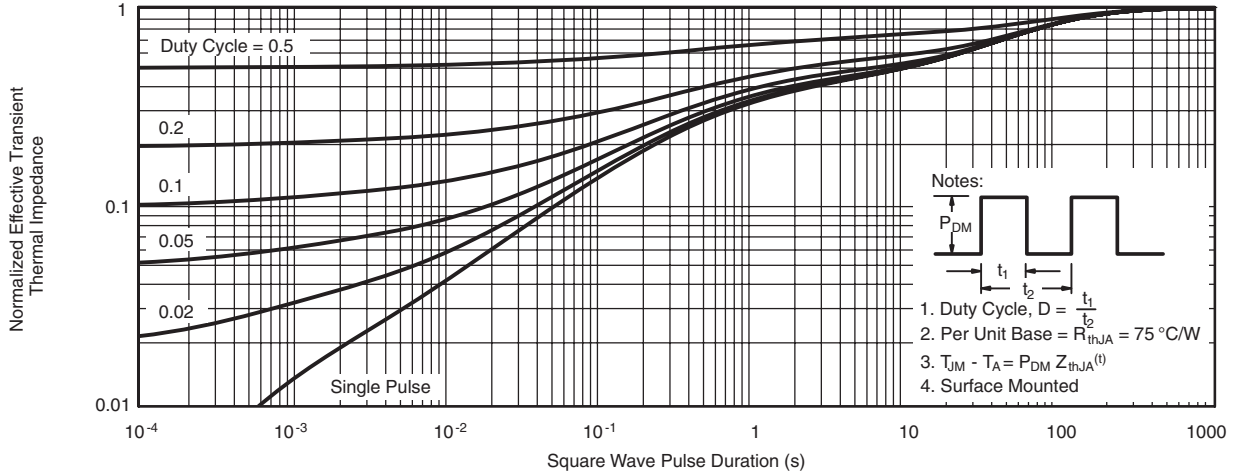
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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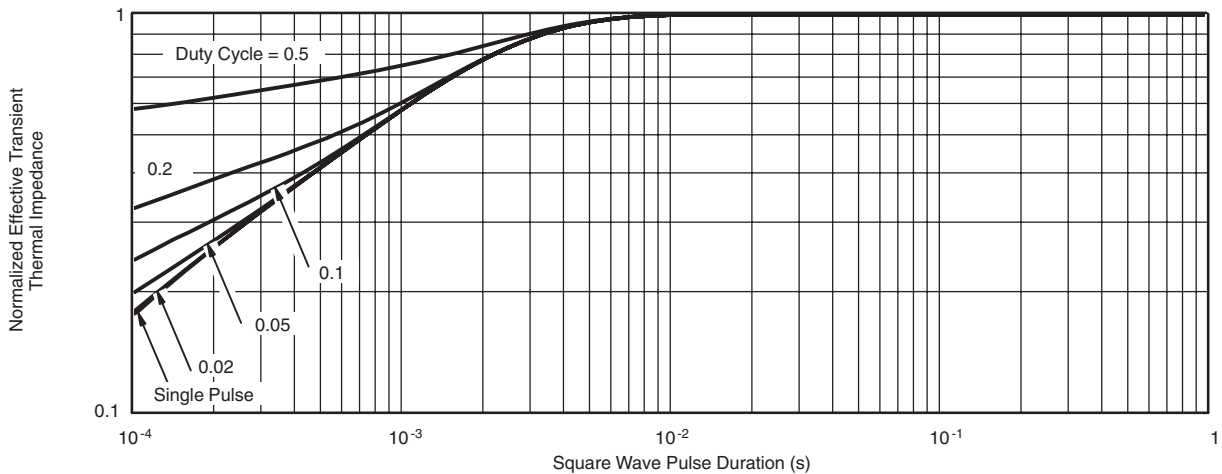
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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