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[SIA443DJ-T1-E3](#)

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New Product

SiA443DJ
Vishay Siliconix

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
- 20	0.045 at $V_{GS} = - 4.5$ V	- 9 ^a	9 nC
	0.063 at $V_{GS} = - 2.5$ V	- 9 ^a	
	0.088 at $V_{GS} = - 1.8$ V	- 9 ^a	

FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance

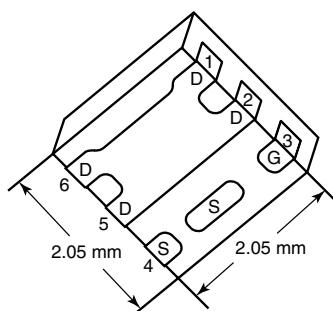


RoHS
COMPLIANT

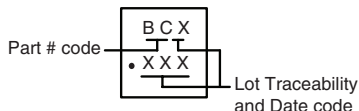
APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices

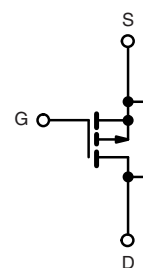
PowerPAK SC-70-6L-Single



Marking Code



Ordering Information: SiA443DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	- 9 ^a	A
	$T_C = 70^\circ\text{C}$	- 9 ^a	
	$T_A = 25^\circ\text{C}$	- 6.7 ^{b, c}	
	$T_A = 70^\circ\text{C}$	- 5.4 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 20	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	- 9 ^a	
	$T_A = 25^\circ\text{C}$	- 2.7 ^{b, c}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	15	W
	$T_C = 70^\circ\text{C}$	9.8	
	$T_A = 25^\circ\text{C}$	3.3 ^{b, c}	
	$T_A = 70^\circ\text{C}$	2.1 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	30	38	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	6.5	8.1	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 80°C/W .

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SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-19.5		mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	ns
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.7\text{ A}$		0.037	0.045	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -3.9\text{ A}$		0.052	0.063	
		$V_{GS} = -1.8\text{ V}, I_D = -1.1\text{ A}$		0.072	0.088	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -4.7\text{ A}$		14		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		750		pF
Output Capacitance	C_{oss}			140		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -6.8\text{ A}$		15	25	nC
Gate-Source Charge	Q_{gs}			9	14	
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g			2.7		
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$		9		Ω
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			40	60	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.9\text{ }\Omega$ $I_D \cong -5.4\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		70	105	ns
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			35	55	
Drain-Source Body Diode Characteristics				75	110	
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			-9	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = -5.4\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -5.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			12	24	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			16		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

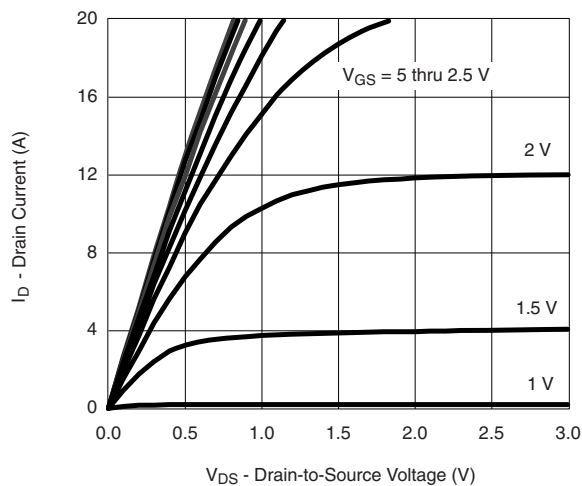
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

New Product

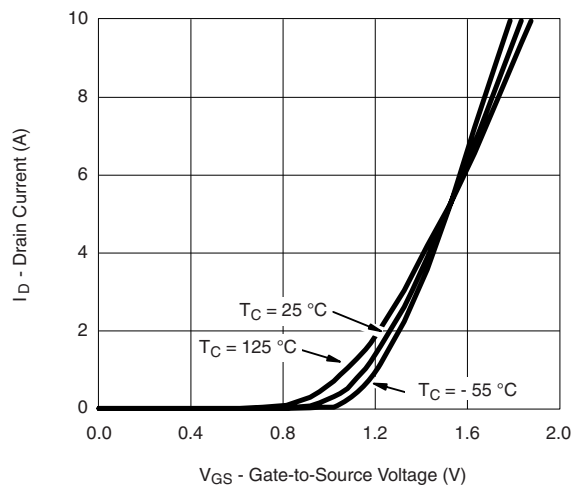


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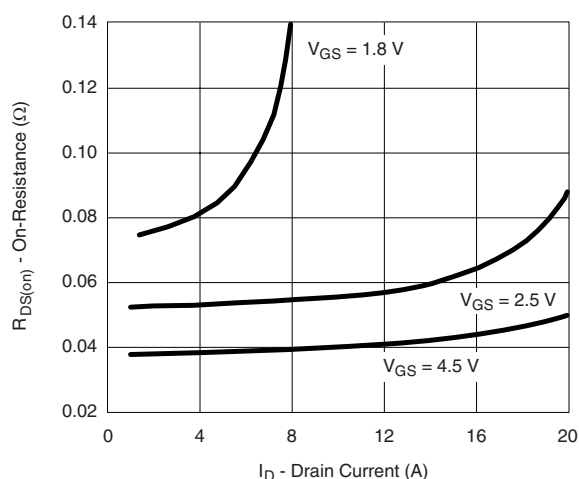
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



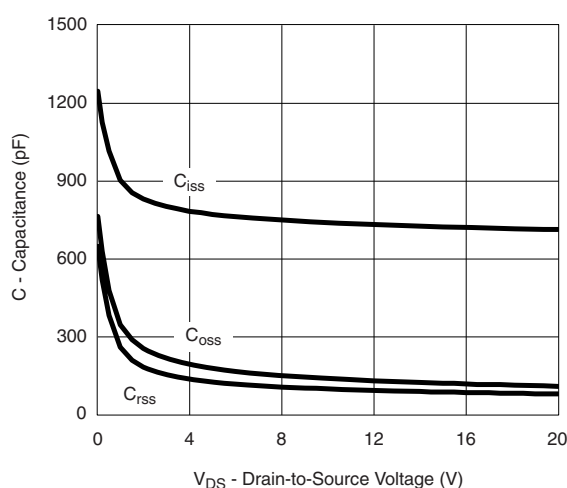
Output Characteristics



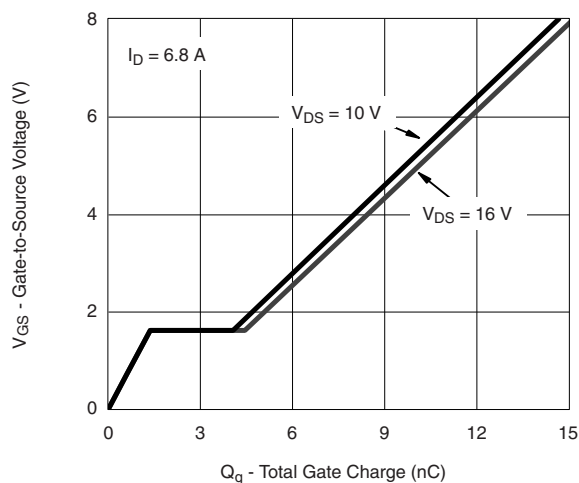
Transfer Characteristics



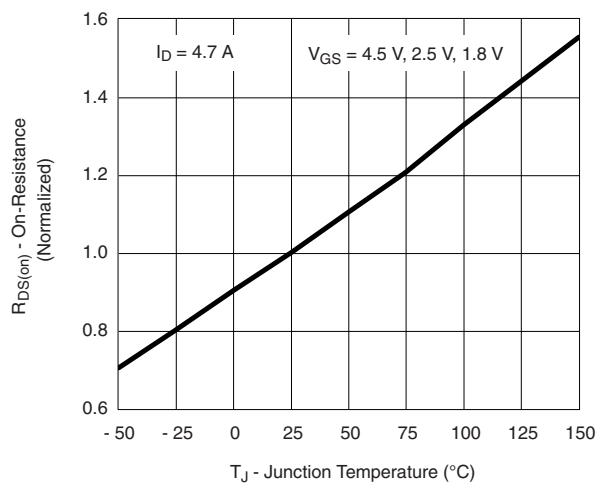
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

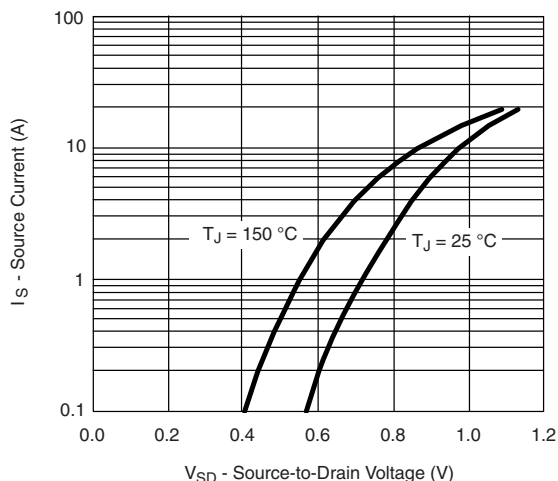
New Product

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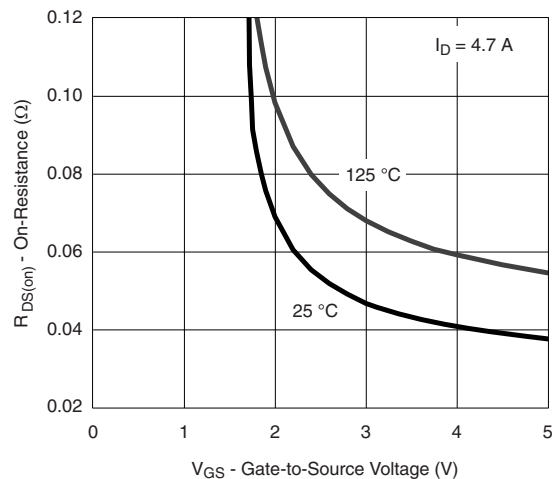
Vishay Siliconix



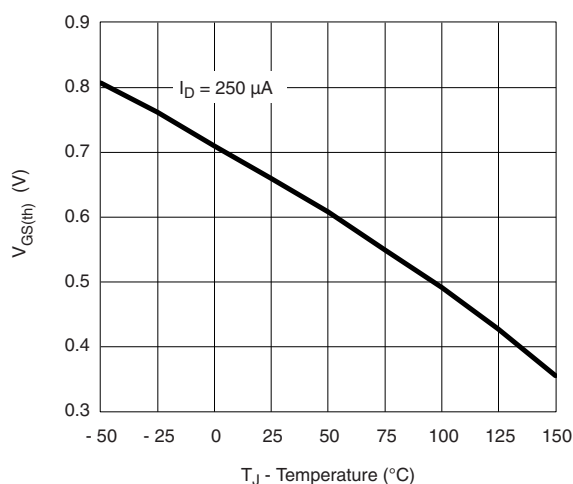
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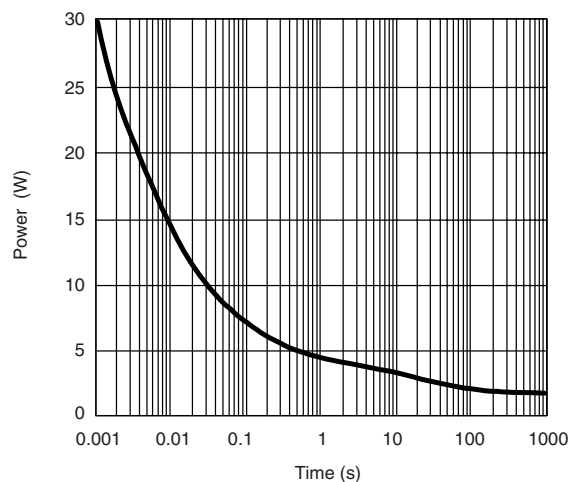
Source-Drain Diode Forward Voltage



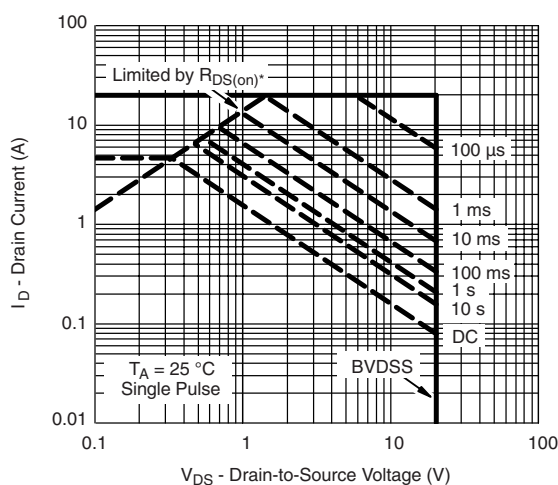
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

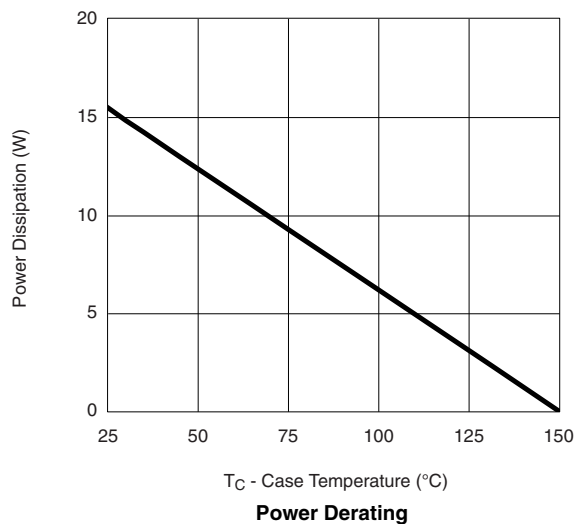
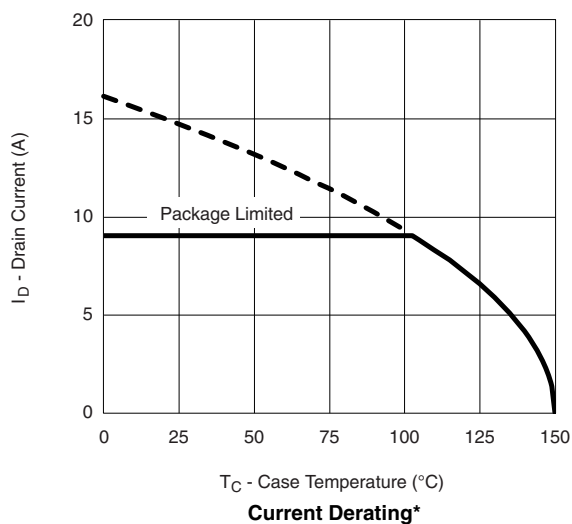
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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

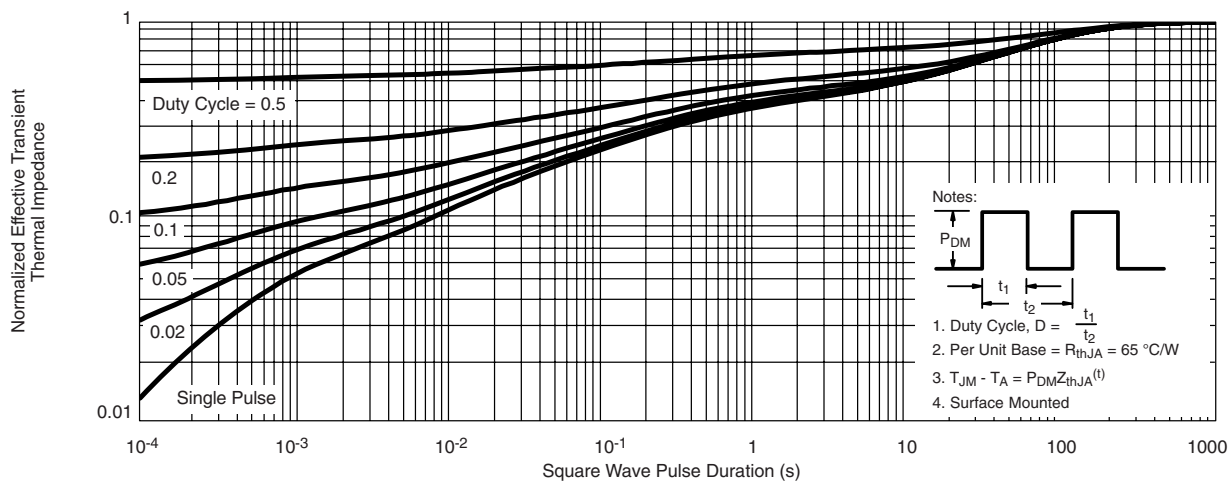
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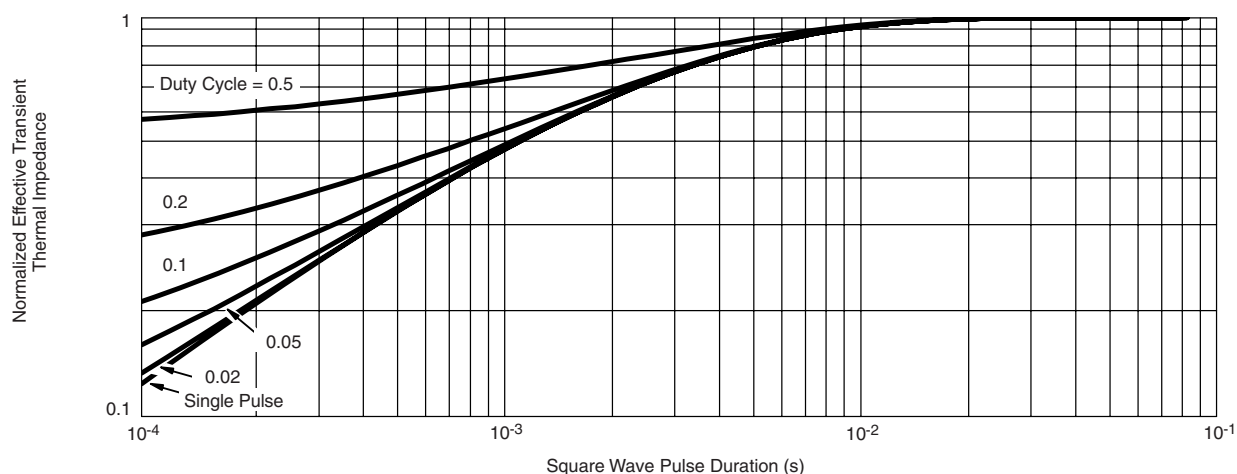
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74474>.



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