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[Vishay/Siliconix](#)
[SIE820DF-T1-E3](#)

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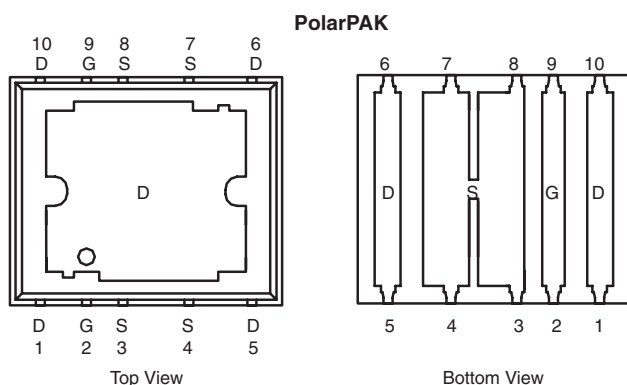


SiE820DF
 Vishay Siliconix

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a		Q _g (Typ.)
		Silicon Limit	Package Limit	
20	0.0035 at V _{GS} = 4.5 V	136	50	43 nC
	0.0064 at V _{GS} = 2.5 V	100	50	

Package Drawing
www.vishay.com/doc?73398



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE820DF-T1-E3 (Lead (Pb)-free)
 SiE820DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

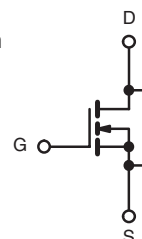
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} WFET Technology for Low Switching Losses
- TrenchFET[®] Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



APPLICATIONS

- VRM
- DC/DC Conversion
- Synchronous Rectification



N-Channel MOSFET
 For Related Documents
www.vishay.com/ppg?74447

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 12	V	
Continuous Drain Current (T _J = 150 °C)	I _D	136 (Silicon Limit)	A	
		50 ^a (Package Limit)		
		50 ^a		
		30 ^{b, c}		
Pulsed Drain Current	I _{DM}	80	A	
		50 ^a		
		4.3 ^{b, c}		
		24 ^{b, c}		
Continuous Source-Drain Diode Current	I _S	50 ^a	A	
		4.3 ^{b, c}		
Single Pulse Avalanche Current	I _{AS}	30	A	
Avalanche Energy	E _{AS}	45	mJ	
Maximum Power Dissipation	P _D	104	W	
		66		
		5.2 ^{b, c}		
		3.3 ^{b, c}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260	°C	

Notes:

- Package limited is 50 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top) ^a	Steady State	R_{thJC} (Drain)	1	1.2	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-4.8			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	0.6	1.4	2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	25			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 18$ A		0.0029	0.0035	Ω
		$V_{GS} = 2.5$ V, $I_D = 13.4$ A		0.0053	0.0064	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 18$ A		106		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		4300		pF
Output Capacitance	C_{oss}		950			
Reverse Transfer Capacitance	C_{rss}		450			
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A		95	143	nC
		$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		43	65	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		11.5		
Gate-Drain Charge	Q_{gd}		10			
Gate Resistance	R_g	$f = 1$ MHz		1.0	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1.0$ Ω $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		35	55	ns
Rise Time	t_r		115	175		
Turn-Off Delay Time	$t_{d(off)}$		105	160		
Fall Time	t_f		30	45		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1.0$ Ω $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω		15	25	
Rise Time	t_r		35	55		
Turn-Off Delay Time	$t_{d(off)}$		55	85		
Fall Time	t_f		10	15		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			50	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 10$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C		101	150	ns
Body Diode Reverse Recovery Charge	Q_{rr}		100	150	nC	
Reverse Recovery Fall Time	t_a		75		ns	
Reverse Recovery Rise Time	t_b		25			

Notes:

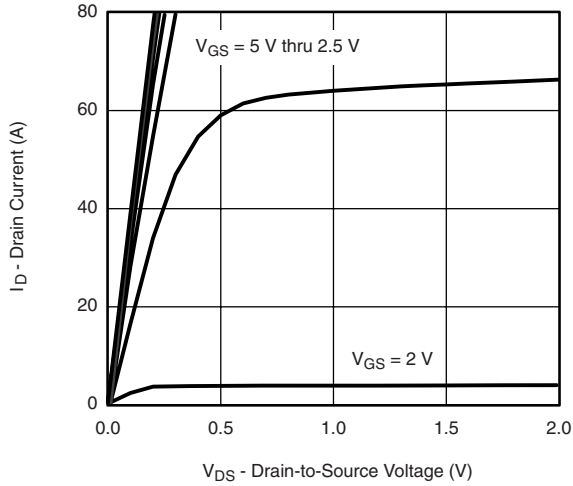
- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

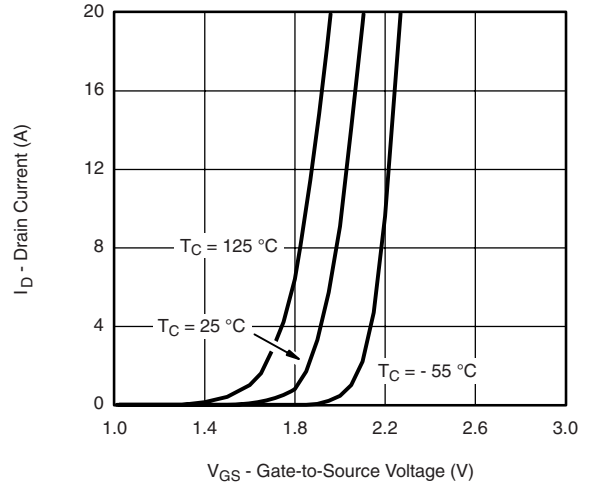


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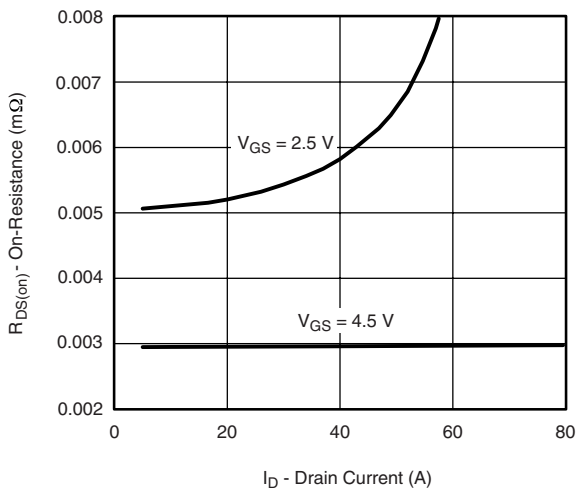
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



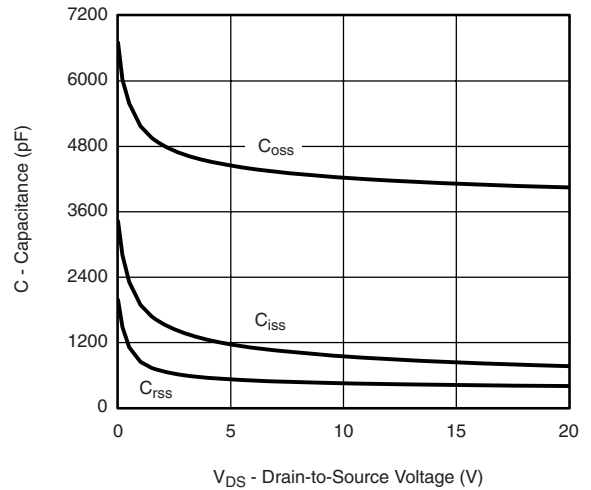
Output Characteristics



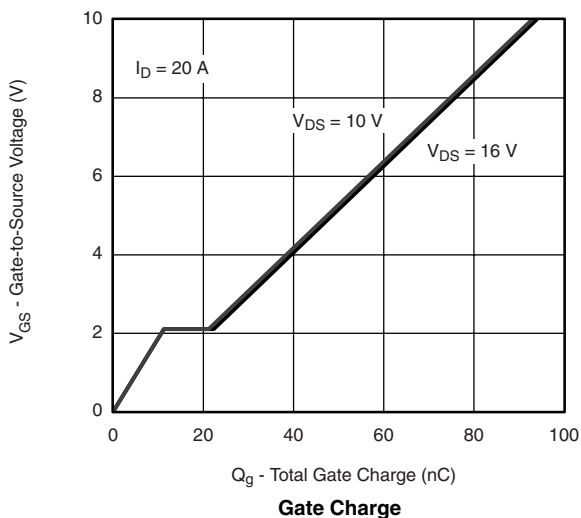
Transfer Characteristics



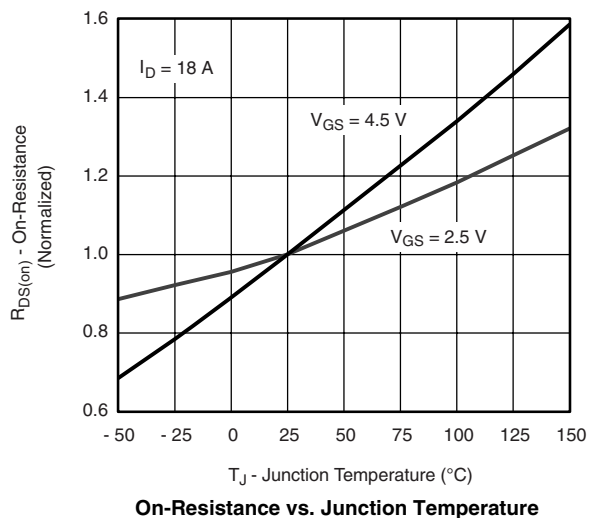
On-Resistance vs. Drain Current



Capacitance



Gate Charge



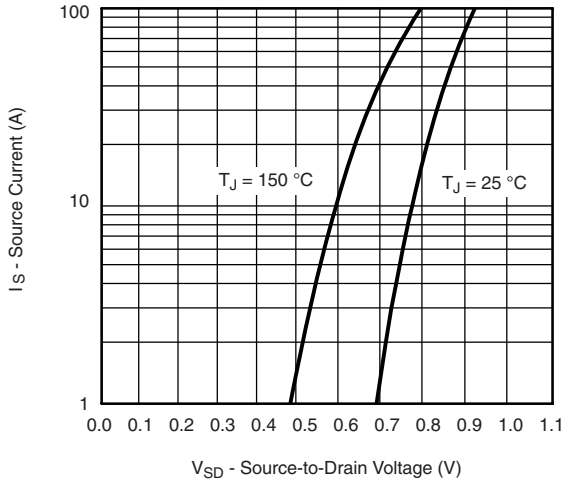
On-Resistance vs. Junction Temperature

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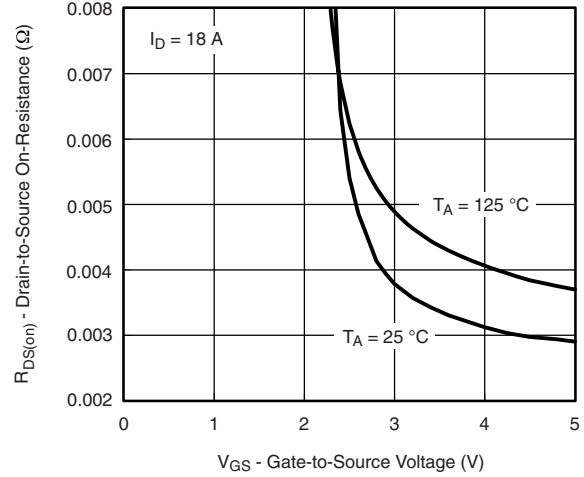
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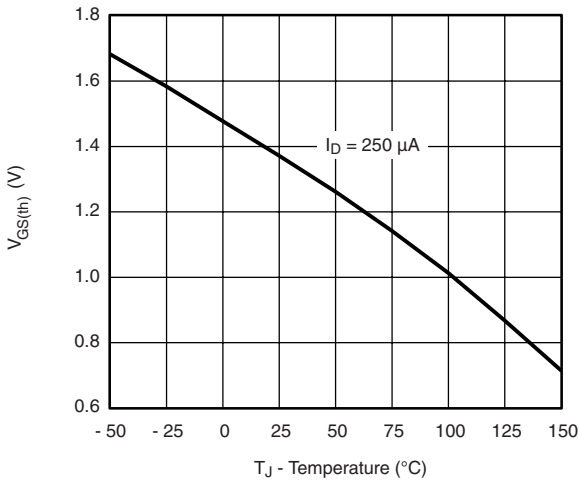
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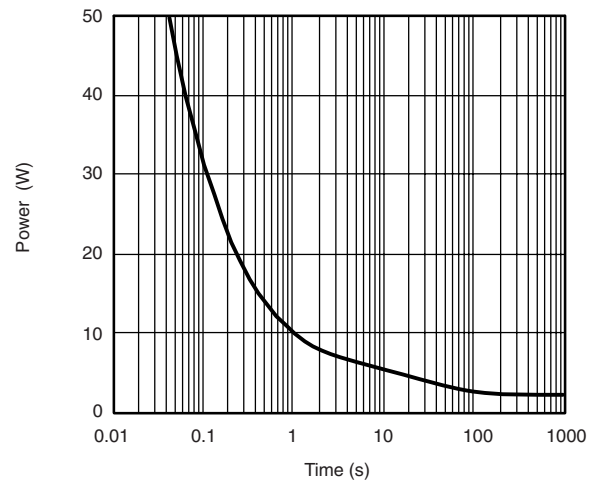
Source-Drain Diode Forward Voltage



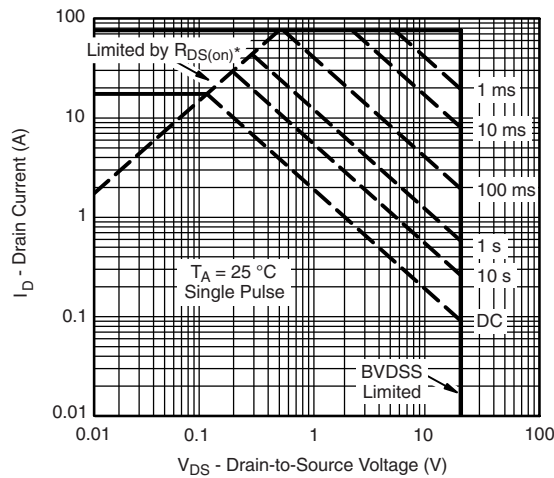
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



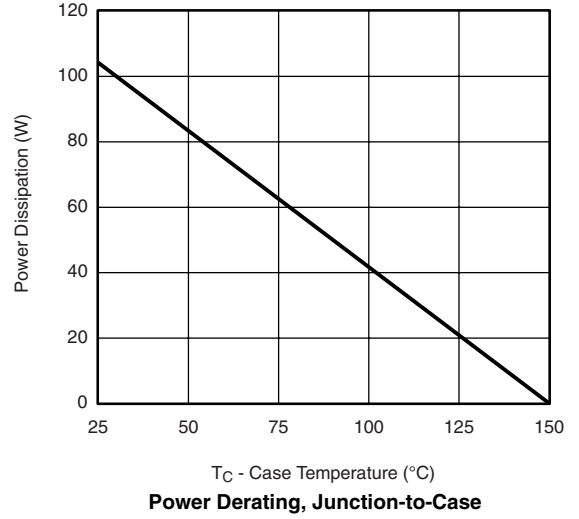
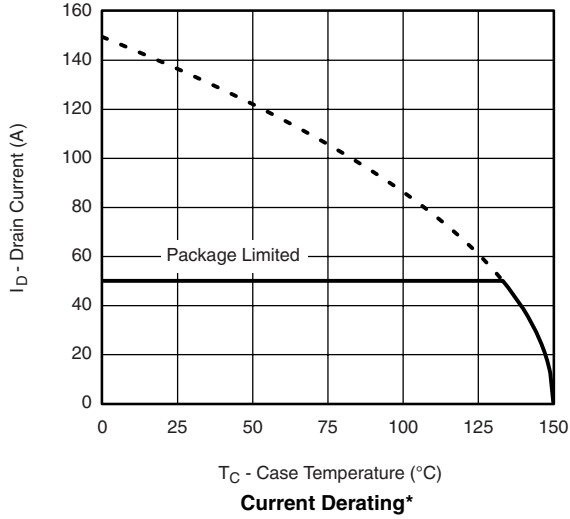
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



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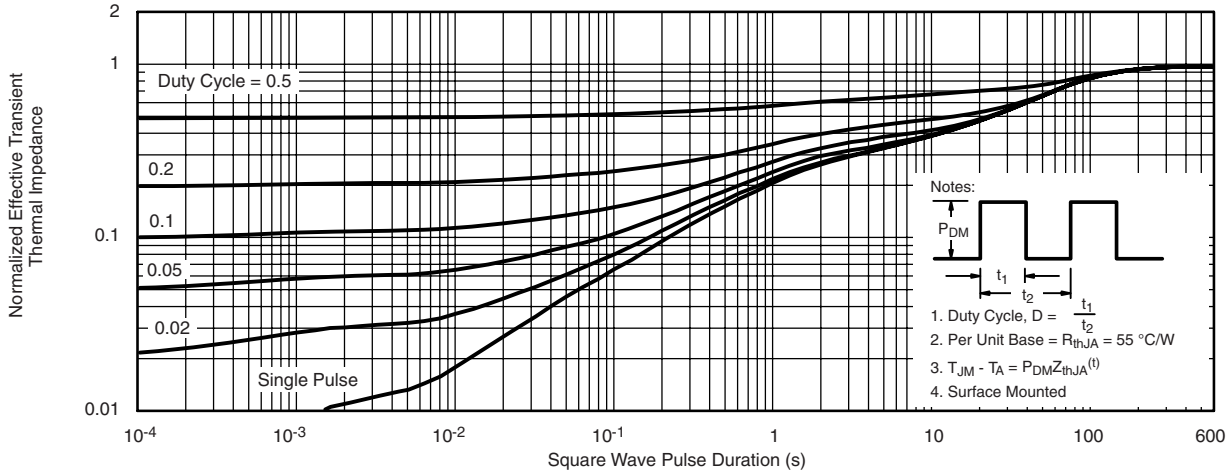
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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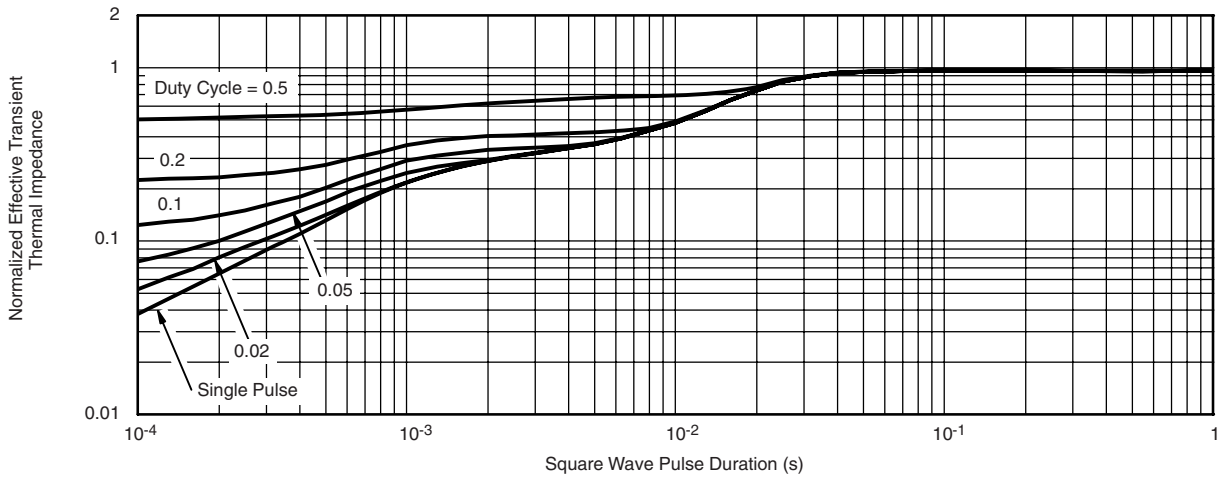
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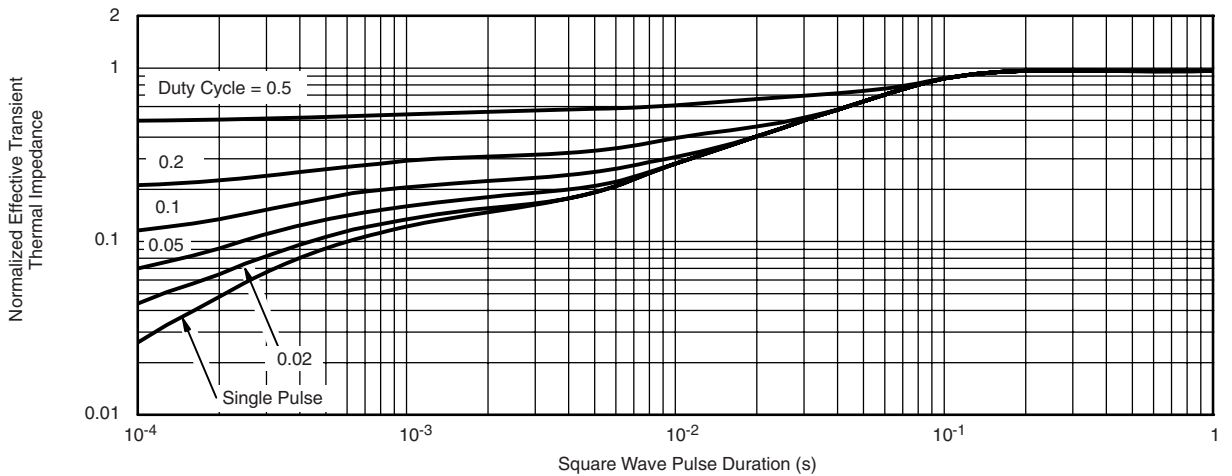
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74447.



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