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Vishay/Siliconix SUM110N04-04-E3

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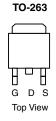
N-Channel 40-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY			
V _{(BR)DSS} (V)	$r_{DS(on)}\left(\Omega\right)$	I _D (A)	
40	$0.0035 \text{ at V}_{GS} = 10 \text{ V}$	110 ^a	

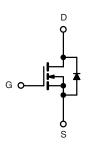
FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature





Ordering Information: SUM110N04-04 SUM110N04-04-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RAT	INGS $T_C = 25 ^{\circ}C$, unless other	rwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	40	V	
Gate-Source Voltage		V _{GS}	20	ľ	
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	l _D	110 ^a	A	
	T _C = 125 °C		107 ^a		
Pulsed Drain Current		I _{DM}	350		
Avalanche Current		I _{AR}	60		
Repetitive Avalanche Energy ^b	L = 0.1 mH	E _{AR}	180	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	В	250 ^c	W	
	T _A = 25 °C ^d	- P _D	3.75] vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	(PCB Mount) ^d	R _{thJA}	40	°C/W	
Junction-to-Case		R _{thJC}	0.6	J/VV	

Notes:

- a. Package limited.
- b. Duty cycle \leq 1 %.
- c. See SOA curve for voltage derating.
- d. When mounted on 1" square PCB (FR-4 material).
- * Pb containing terminations are not RoHS compliant, exemptions may apply.

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Datasheet of SUM110N04-04-E3 - MOSFET N-CH 40V 110A D2PAK

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static		1				
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	40			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA
Zero Gate Voltage Drain Current		V _{DS} = 40 V, V _{GS} = 0 V			1	μΑ
	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			Α
Drain-Source On-State Resistance ^a		V _{GS} = 10 V, I _D = 30 A		0.0028	0.0035	Ω
	r _{DS(on)}	V _{GS} = 10 V, I _D = 30 A, T _J = 125 °C			0.0055	
		V _{GS} = 10 V, I _D = 30 A, T _J = 175 °C			0.006	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	30			S
Dynamic ^b	<u>'</u>				<u>'</u>	
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		6800		pF
Output Capacitance	C _{oss}			1110		
Reverse Transfer Capacitance	C _{rss}			690		
Total Gate Charge ^c	Q_g			140	200	nC
Gate-Source Charge ^c	Q _{gs}	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 110 A		35		
Gate-Drain Charge ^c	Q_{gd}			55		
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 30 \text{ V, } R_L = 0.47 \Omega$ $I_D \cong 110 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 2.5 \Omega$		20	35	ns
Rise Time ^c	t _r			115	175	
Turn-Off Delay Time ^c	t _{d(off)}			75	115	
Fall Time ^c	t _f			85	130	
Source-Drain Diode Ratings and Cha	aracteristics	Γ _C = 25 °C ^b				
Continuous Current	Is				110	^
Pulsed Current	I _{SM}				350	_ A
Forward Voltage ^a	V _{SD}	I _F = 110 A, V _{GS} = 0 V		1.1	1.4	V
Reverse Recovery Time	t _{rr}			50	80	ns
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 110 A, di/dt = 100 A/μs		2	3	Α
Reverse Recovery Charge	Q _{rr}			0.05	0.12	μC

Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

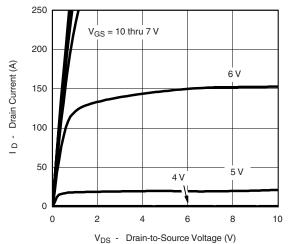
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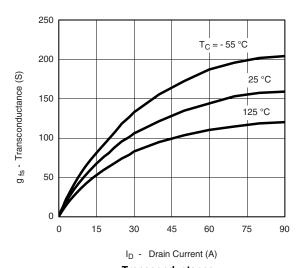


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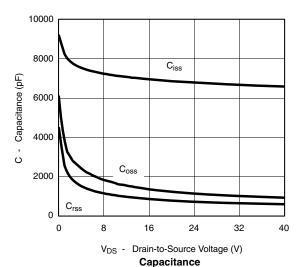
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

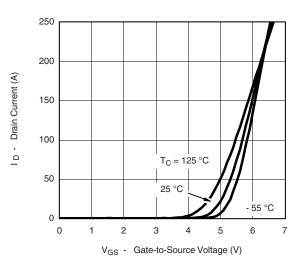




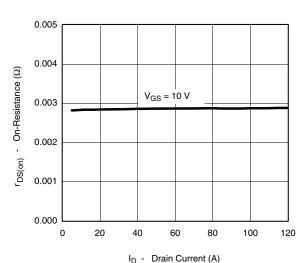


Transconductance

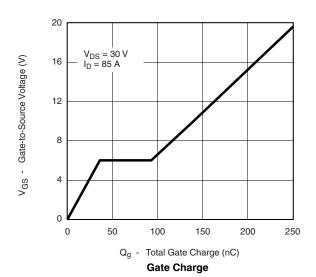




Transfer Characteristics



On-Resistance vs. Drain Current



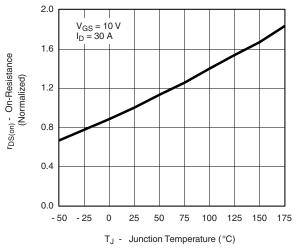
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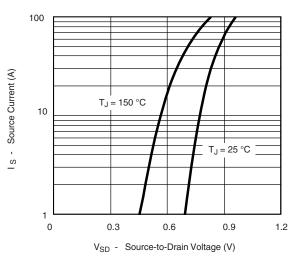
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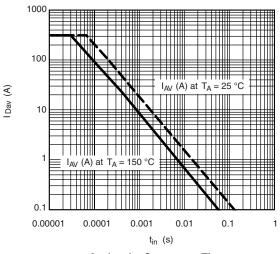




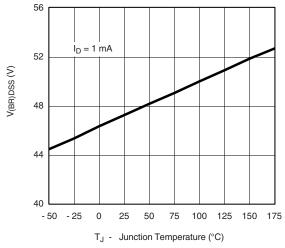
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



Avalanche Current vs. Time



Drain Source Breakdown vs. Junction Temperature

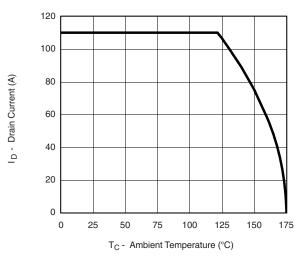
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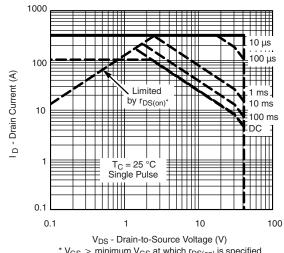


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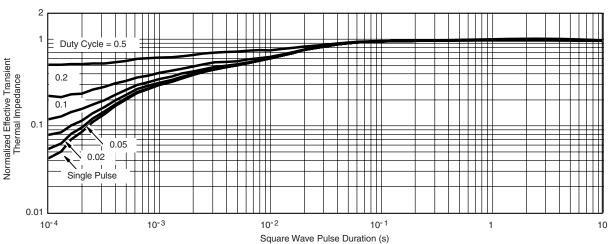
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72077.

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Datasheet of SUM110N04-04-E3 - MOSFET N-CH 40V 110A D2PAK

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