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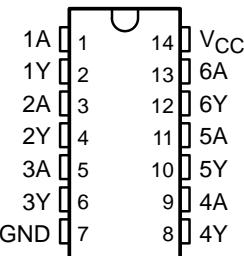
[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

## SN74AHCT14-EP HEX SCHMITT-TRIGGER INVERTER

SCLS492 – JUNE 2003

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200 \text{ pF}$ ,  $R = 0$ )**

**D OR PW PACKAGE  
(TOP VIEW)**



† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### description/ordering information

The SN74AHCT14 contains six independent inverters. This device performs the Boolean function  $Y = \bar{A}$ .

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going ( $V_{T+}$ ) and for negative-going ( $V_{T-}$ ) signals.

### ORDERING INFORMATION

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – D	Tape and reel	SN74AHCT14MDREP	AHCT14MEP
	TSSOP – PW	Tape and reel	SN74AHCT14MPWREP	AHT14EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE  
(each inverter)**

INPUT A	OUTPUT Y
H	L
L	H



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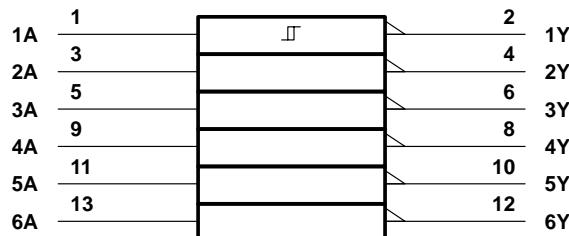
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# SN74AHCT14-EP HEX SCHMITT-TRIGGER INVERTER

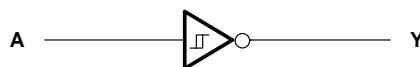
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## logic symbol†



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	86°C/W
	PW package .....
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
T <sub>A</sub>	Operating free-air temperature	-55	125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74AHCT14-EP**  
**HEX SCHMITT-TRIGGER INVERTER**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>T+</sub> Positive-going input threshold voltage		4.5 V	0.9	1.9	0.9	1.9		V
		5.5 V	1	2.1	1	2.1		
V <sub>T-</sub> Negative-going input threshold voltage		4.5 V	0.5	1.5	0.5	1.5		V
		5.5 V	0.6	1.7	0.6	1.7		
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )		4.5 V	0.4	1.4	0.4	1.4		V
		5.5 V	0.4	1.5	0.4	1.5		
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5	4.4			V
	I <sub>OH</sub> = –8 mA	4.5 V	3.94		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1	0.1			V
	I <sub>OL</sub> = 8 mA	4.5 V		0.36	0.44			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2	20	μA		
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		1.35	1.5	mA		
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10	pF		

<sup>†</sup>This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range**  
**V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	4	7	1	8		ns
				4	7	1	8		
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.5	8	1	9		ns
				5.5	8	1	9		

**noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)**

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>	0.9			V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>	-0.7			V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>	4.3			V
V <sub>IH(D)</sub> High-level dynamic input voltage	2.1			V
V <sub>IL(D)</sub> Low-level dynamic input voltage	0.5			V

NOTE 4: Characteristics are for surface-mount packages only.

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

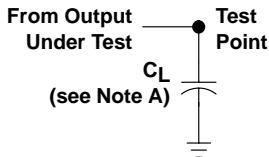
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	12	pF

## SN74AHCT14-EP

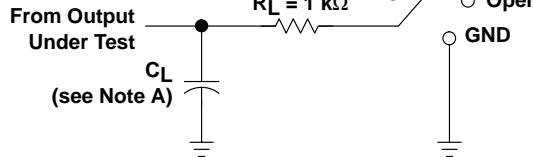
### HEX SCHMITT-TRIGGER INVERTER

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#### PARAMETER MEASUREMENT INFORMATION

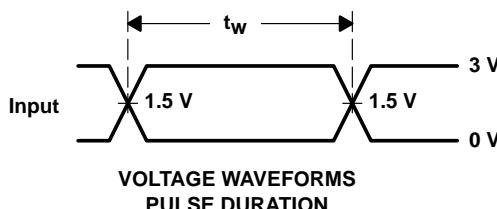


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

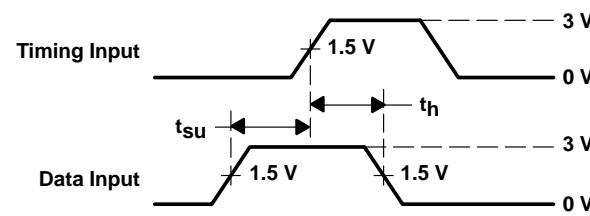


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

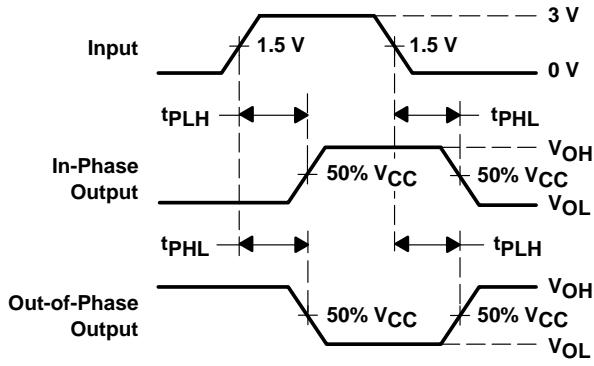
TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND
Open Drain	V <sub>CC</sub>



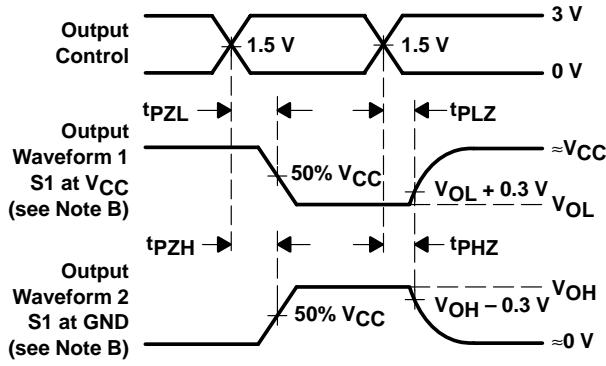
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT14MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AHCT14MEP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT14MPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AHT14EP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
V62/03656-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AHT14EP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
V62/03656-01YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AHCT14MEP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBsolete:** TI has discontinued the production of the device.(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.**TBD:** The Pb-Free/Green conversion plan has not been defined.**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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• Catalog: [SN74AHCT14](#)

• Military: [SN54AHCT14](#)

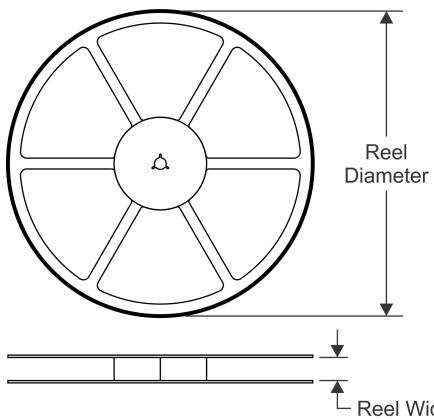
NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

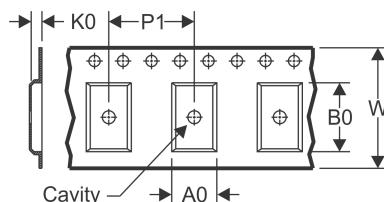
• Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

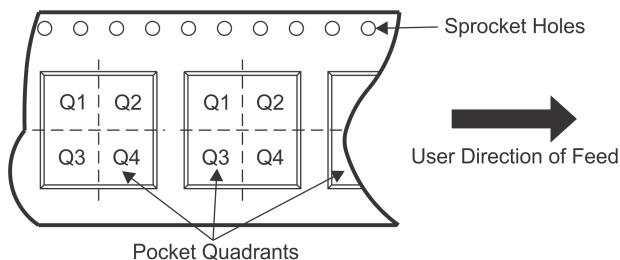


**TAPE DIMENSIONS**



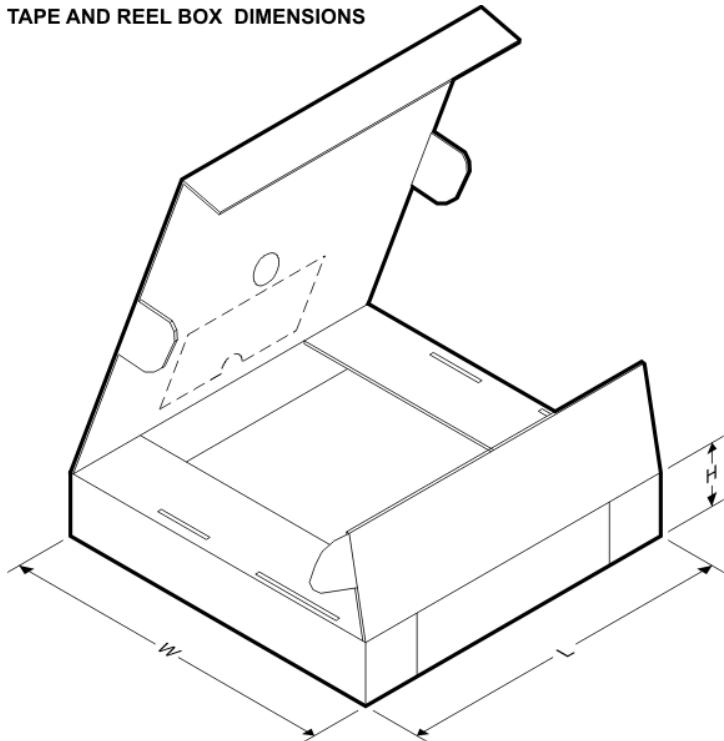
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT14MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT14MDREP	SOIC	D	14	2500	333.2	345.9	28.6

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