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**TRS3232E**

SLLS790A – JUNE 2007 – REVISED JULY 2015

## TRS3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With $\pm 15$ -kV IEC ESD Protection

### 1 Features

- ESD Protection for RS-232 Bus Pins
  - $\pm 15$  kV (HBM)
  - $\pm 8$  kV (IEC61000-4-2, Contact Discharge)
  - $\pm 15$  kV (IEC61000-4-2, Air-Gap Discharge)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates up to 250 kbps
- Two Drivers and Two Receivers
- Low Supply Current: 300  $\mu$ A (Typical)
- External Capacitors:  $4 \times 0.1$   $\mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Pin Compatible to Alternative High-Speed Devices (1 Mbps)
  - SN65C3232E ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
  - SN75C3232E ( $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )

### 2 Applications

- Battery-Powered Systems
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

### 3 Description

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

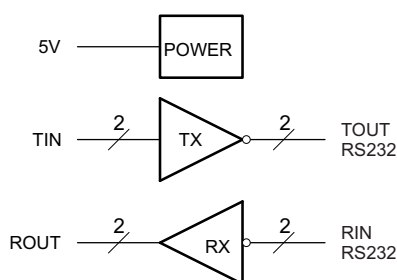
The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/ $\mu$ s driver output slew rate.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS3232ExD	SOIC (16)	9.90 mm $\times$ 3.91 mm
TRS3232ExDB	SSOP (16)	6.20 mm $\times$ 5.30 mm
TRS3232ExDW	SOIC (16)	10.30 mm $\times$ 7.50 mm
TRS3232ExPW	TSSOP (16)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Diagram



## TRS3232E

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (December 2013) to Revision C

Page

• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
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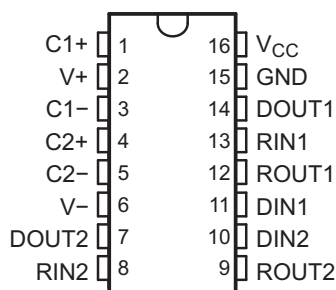
### Changes from Revision A (April 2007) to Revision B

Page

• Updated document to new TI data sheet format .....	1
• Deleted <i>Ordering Information</i> table. ....	1
• Added <i>Thermal Information</i> table. ....	5

## 5 Pin Configuration and Functions

**D, DW, DB or PW Package  
16-Pin SOIC, SSOP or TSSOP  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
C1–	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2–	5	—	Negative lead of C2 capacitor
DIN1	11	I	Logic data input (from UART)
DIN2	10	I	Logic data input (from UART)
DOUT2	7	O	RS232 line data output (to remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
RIN1	13	I	RS232 line data input (from remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
ROUT1	12	O	Logic data output (to UART)
V+	2	O	Positive charge pump output for storage capacitor only
V–	6	O	Negative charge pump output for storage capacitor only
V <sub>CC</sub>	16	—	Supply voltage, connect to external 3-V to 5.5-V power supply

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## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		−0.3	6	V
V <sub>+</sub>	Positive output supply voltage <sup>(2)</sup>		−0.3	7	V
V <sub>−</sub>	Negative output supply voltage <sup>(2)</sup>		0.3	−7	V
V <sub>+</sub> − V <sub>−</sub>	Supply voltage difference <sup>(2)</sup>			13	V
V <sub>I</sub>	Input voltage	Drivers	−0.3	6	V
		Receivers	−25	25	V
V <sub>O</sub>	Output voltage	Drivers	−13.2	13.2	V
		Receivers	−0.3	V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Operating virtual junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins except 7, 8, 14, and 14	±2000
			Pins 7, 8, 14, and 14	±15000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	All pins	±1500
		IEC61000-4-2, Contact Discharge	Pins 7, 8, 14, and 14	±8000
		IEC61000-4-2, Air-Gap Discharge	Pins 7, 8, 14, and 14	±15000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See Figure 7.<sup>(1)</sup>

			MIN	NOM	MAX	UNIT
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver high-level input voltage	DIN	V <sub>CC</sub> = 3.3 V	2	5.5	V
			V <sub>CC</sub> = 5 V	2.4	5.5	
V <sub>IL</sub>	Driver low-level input voltage	DIN	0		0.8	V
V <sub>I</sub>	Receiver input voltage	RIN	−25		25	V
T <sub>A</sub>	Operating free-air temperature	TRS3232EC	0		70	°C
		TRS3232EI	−40		85	

(1) C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TRS3232E				UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	99.3	76.1	72.3	90.9	°C/W
R <sub>θJCTop</sub>	Junction-to-case (top) thermal resistance	20.8	36.7	33.5	36.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	45.1	33.6	37.1	43.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.6	4.2	7.5	4.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	45.1	33.3	37.1	42.9	°C/W
R <sub>θJBot</sub>	Junction-to-case (bottom) thermal resistance	–	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7](#)).<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current No load, V <sub>CC</sub> = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.6 Electrical Characteristics — Driver

over operating free-air temperature range (unless otherwise noted) (see [Figure 7](#)).<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>	–5	–5.4		V
I <sub>IH</sub>	High-level input current V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub>	Low-level input current V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub> <sup>(3)</sup>	Short-circuit output current V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V		±35	±60	mA
r <sub>O</sub>	Output resistance V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.7 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7](#)).<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage I <sub>OH</sub> = –1 mA	V <sub>CC</sub> – 0.6	V <sub>CC</sub> – 0.1		V
V <sub>OL</sub>	Low-level output voltage I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage V <sub>CC</sub> = 3.3 V V <sub>CC</sub> = 5 V		1.5 1.8	2.4 2.4	V
V <sub>IT–</sub>	Negative-going input threshold voltage V <sub>CC</sub> = 3.3 V V <sub>CC</sub> = 5 V	0.6 0.8	1.2 1.5		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )		0.3		V
r <sub>i</sub>	Input resistance V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

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### 6.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 7)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	$R_L = 3\text{ k}\Omega$ , One DOUT switching, $C_L = 1000\text{ pF}$ , see Figure 3	150	250		kbps
$t_{sk(p)}$ Driver pulse skew <sup>(3)</sup>	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , see Figure 4 $C_L = 150\text{ pF}$ to $2500\text{ pF}$ ,		300		ns
$SR(tr)$ Driver slew rate, transition region (see Figure 3)	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $V_{CC} = 3.3\text{ V}$	$C_L = 150\text{ pF}$ to $1000\text{ pF}$		6	V/ $\mu\text{s}$
		$C_L = 150\text{ pF}$ to $2500\text{ pF}$		4	
$t_{PLH}$ Receiver propagation delay time, low- to high-level output	$C_L = 150\text{ pF}$ , see Figure 5			300	ns
$t_{PHL}$ Receiver propagation delay time, high- to low-level output				300	ns
$t_{sk(p)}$ Receiver pulse skew <sup>(3)</sup>				300	ns

(1) Test conditions are  $C1-C4 = 0.1\text{ }\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ;  $C1 = 0.047\text{ }\mu\text{F}$ ,  $C2-C4 = 0.33\text{ }\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

(3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

### 6.9 Typical Characteristics

$V_{CC} = 3.3\text{ V}$

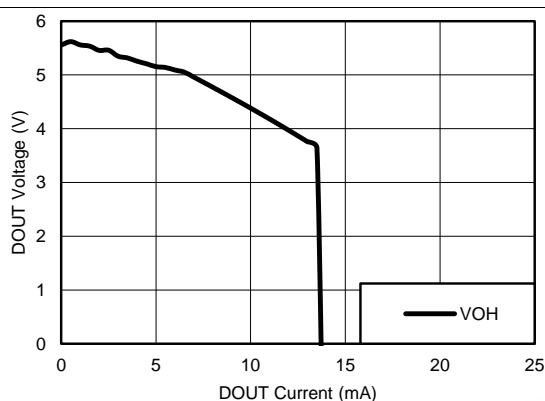


Figure 1. DOUT  $V_{OH}$  vs Load Current, Both Drivers Loaded

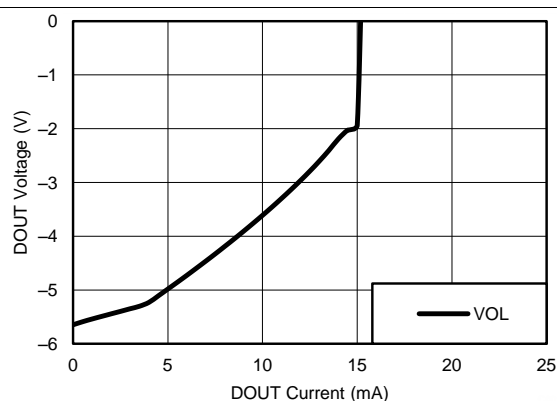
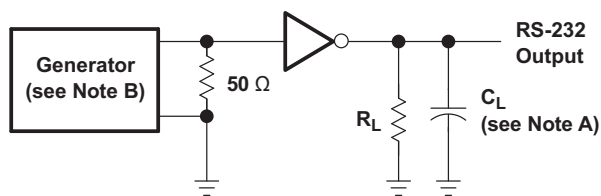


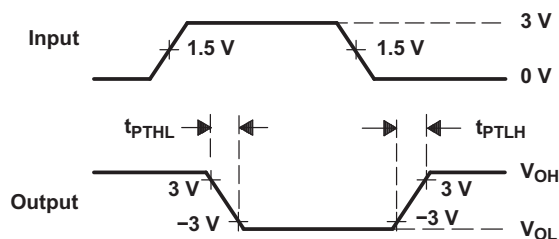
Figure 2. DOUT  $V_{OL}$  vs Load Current, Both Drivers Loaded

## 7 Parameter Measurement Information



TEST CIRCUIT

$$SR(tr) = \frac{6\text{ V}}{t_{PTHL} \text{ or } t_{PTLH}}$$

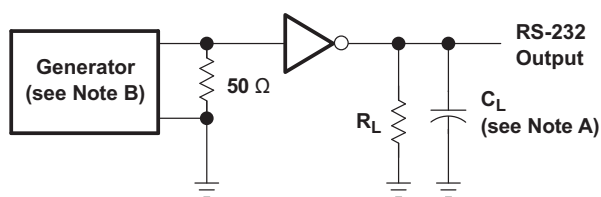


VOLTAGE WAVEFORMS

A.  $C_L$  includes probe and jig capacitance

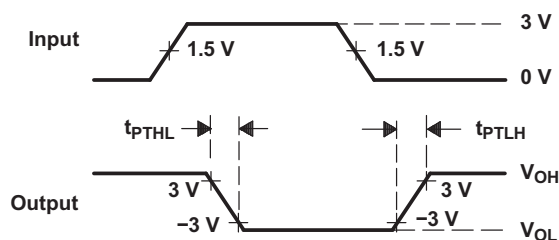
B. The pulse generator has the following characteristics: PRR = 250 kbps,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

**Figure 3. Driver Slew Rate**



TEST CIRCUIT

$$SR(tr) = \frac{6\text{ V}}{t_{PTHL} \text{ or } t_{PTLH}}$$

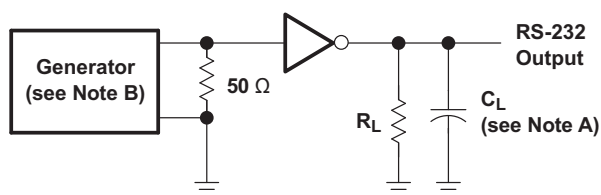


VOLTAGE WAVEFORMS

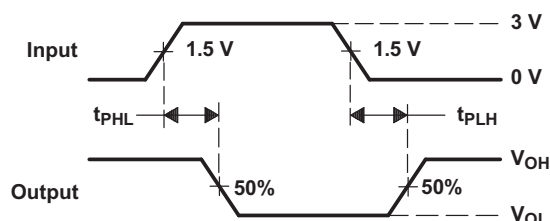
A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

**Figure 4. Driver Pulse Skew**



TEST CIRCUIT



VOLTAGE WAVEFORMS

A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

**Figure 5. Receiver Propagation Delay Times**



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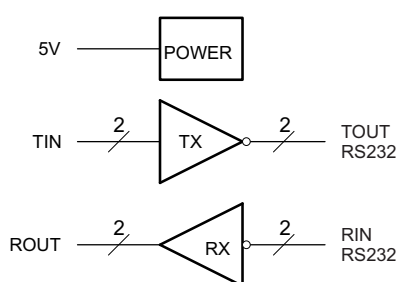
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## 8 Detailed Description

### 8.1 Overview

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/ $\mu$ s driver output slew rate. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

#### 8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

#### 8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

## 8.4 Device Functional Modes

Table 1 and Table 2 list the functional modes of the drivers and receivers of TRS3232E.

**Table 1. Each Driver<sup>(1)</sup>**

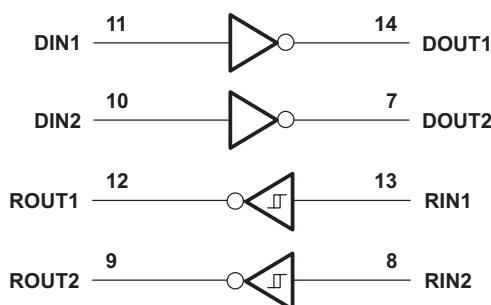
INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

**Table 2. Each Receiver<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off



**Figure 6. Logic Diagram**

### 8.4.1 $V_{CC}$ Powered by 3 V to 5.5 V

The device is in normal operation.

### 8.4.2 $V_{CC}$ Unpowered, $V_{CC} = 0$ V

When TRS3232E is unpowered, it can be safely connected to an active remote RS232 device.

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## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

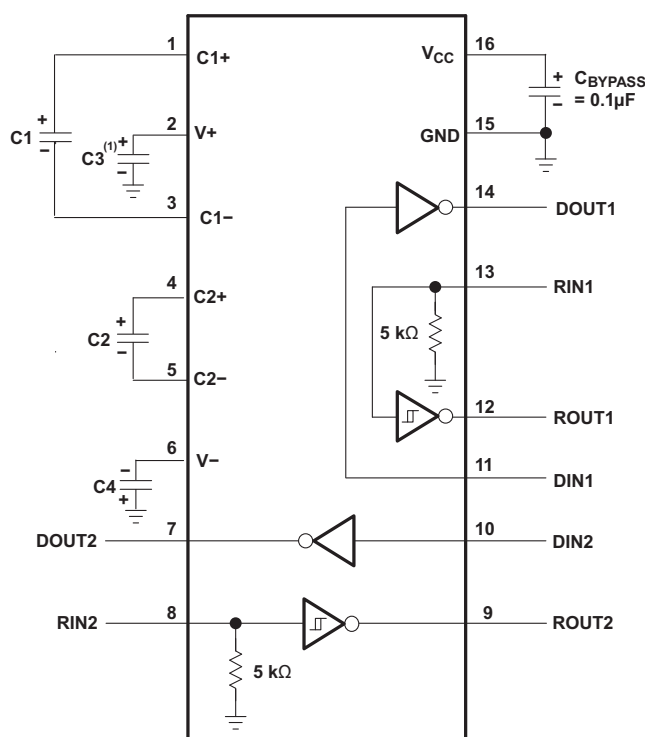
### 9.1 Application Information

The TRS3232E interfaces logic lines from a UART or microcontroller to the voltage and current levels needed for RS232 communication. The TIN inputs will accept 5-V logic with 3.3-V  $V_{CC}$  supply. All baud rates up to 250-kbps are supported.

It is important to use the correct capacitors for the  $V_{CC}$  voltage. This will reduce ripple voltage on the TOUT outputs. If only one driver is needed, the unused driver input should be connected to  $V_{CC}$  or ground.

### 9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable. For proper operation, add capacitors as shown in Table 3.



(1) C3 can be connected to  $V_{CC}$  or GND

Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 7. Typical Operating Circuit and Capacitor Values**

**Table 3.  $V_{CC}$  vs Capacitor Values**

$V_{CC}$	C1	C2, C3, C4
3.3 V $\pm$ 0.3 V	0.1 $\mu$ F	0.1 $\mu$ F
5 V $\pm$ 0.5 V	0.047 $\mu$ F	0.33 $\mu$ F
3 V $\pm$ 5.5 V	0.1 $\mu$ F	0.47 $\mu$ F

### 9.2.1 Design Requirements

The recommended  $V_{CC}$  is 3.3 V or 5 V. 3 V to 5.5 V is also possible.

The maximum recommended bit rate is 250 kbps.

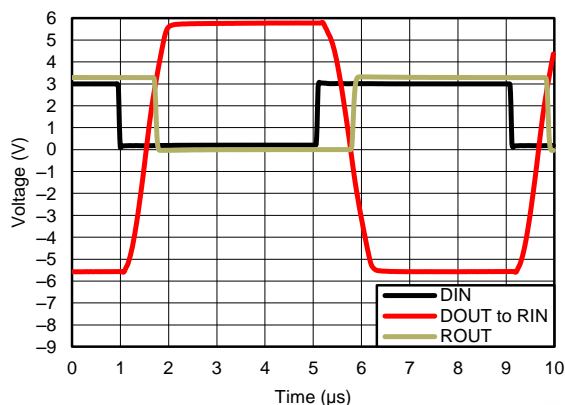
### 9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on  $V_{CC}$  level for best performance.

### 9.2.3 Application Curve

Figure 8 curves are for 3.3-V  $V_{CC}$  and 250-kbps alternative bit data stream.



**Figure 8. 250 kbps Driver to Receiver Loopback Timing Waveform,  
 $V_{CC}$  = 3.3 V**

## TRS3232E

SLLS790A – JUNE 2007 – REVISED JULY 2015

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## 10 Power Supply Recommendations

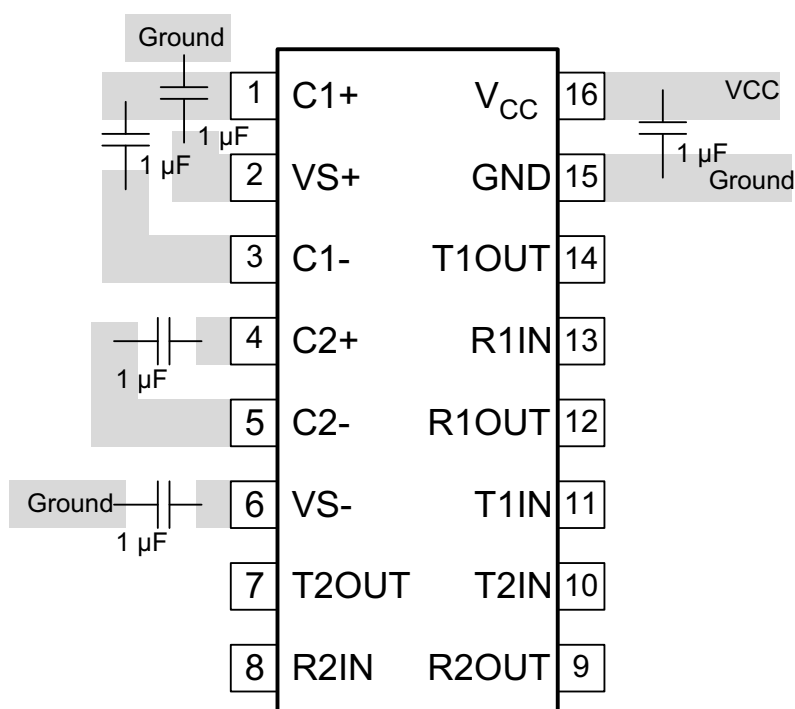
The supply voltage,  $V_{CC}$ , should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using [Table 3](#).

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

### 11.2 Layout Example



**Figure 9. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

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### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	<a href="#">Samples</a>
TRS3232ECDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC	<a href="#">Samples</a>
TRS3232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	<a href="#">Samples</a>
TRS3232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	<a href="#">Samples</a>
TRS3232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232EC	<a href="#">Samples</a>
TRS3232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC	<a href="#">Samples</a>
TRS3232ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC	<a href="#">Samples</a>
TRS3232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32EC	<a href="#">Samples</a>
TRS3232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	<a href="#">Samples</a>
TRS3232EIDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>
TRS3232EIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>
TRS3232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	<a href="#">Samples</a>
TRS3232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	<a href="#">Samples</a>
TRS3232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232EI	<a href="#">Samples</a>
TRS3232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>
TRS3232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>
TRS3232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>



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Datasheet of TRS3232ECDR - IC MULTICH RS232 DVR/RCVR 16SOIC

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### PACKAGE OPTION ADDENDUM

www.ti.com

10-Jun-2014

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**PACKAGE OPTION ADDENDUM**

10-Jun-2014

- 
- Automotive: [TRS3232E-Q1](#)

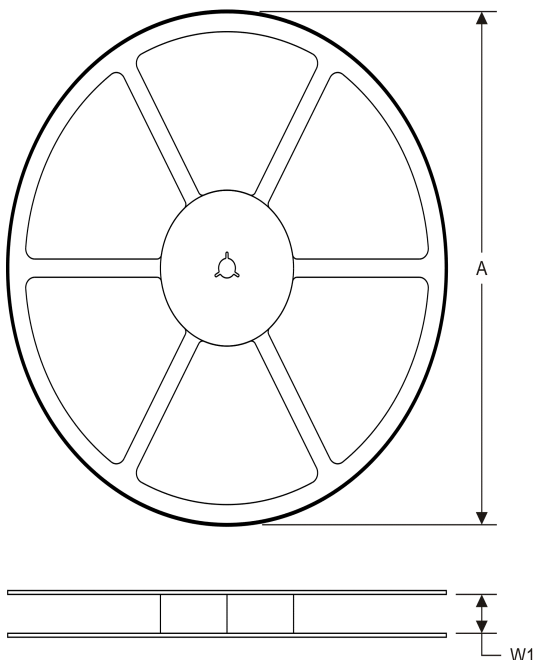
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

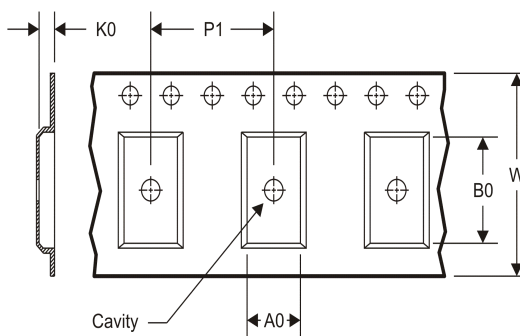
## PACKAGE MATERIALS INFORMATION

### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS



#### TAPE DIMENSIONS



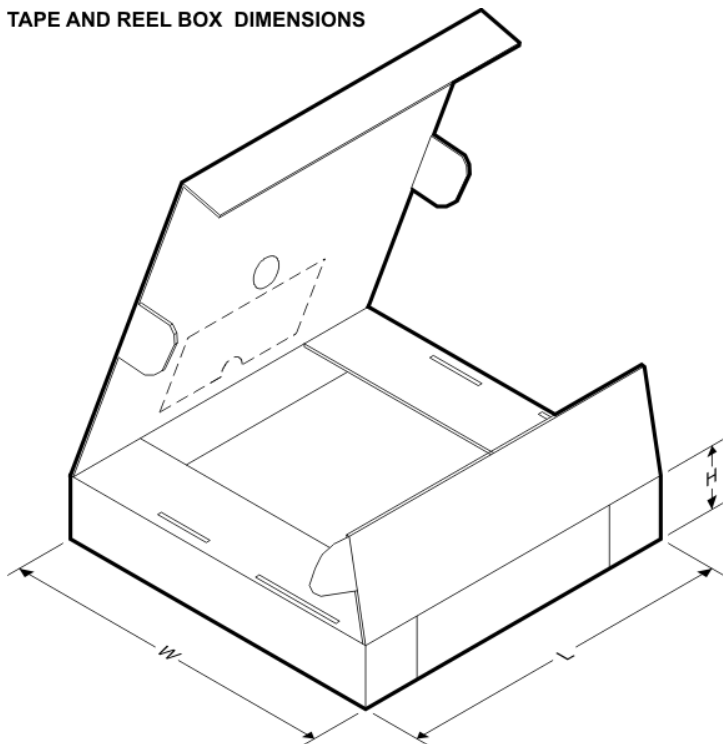
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRS3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRS3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



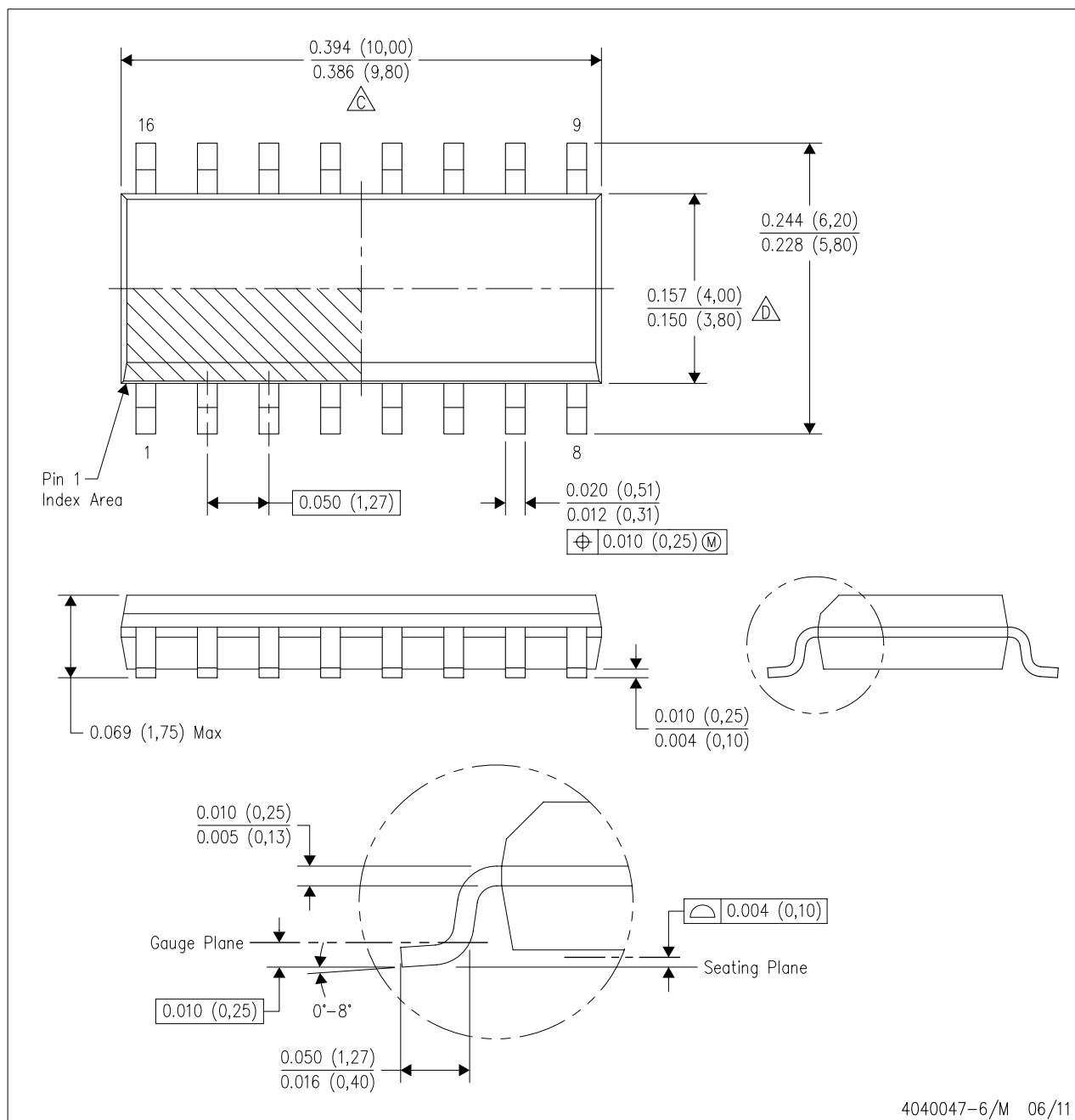
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232ECDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TRS3232ECDR	SOIC	D	16	2500	367.0	367.0	38.0
TRS3232ECDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TRS3232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3232EIDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TRS3232EIDR	SOIC	D	16	2500	367.0	367.0	38.0
TRS3232EIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TRS3232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

## MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



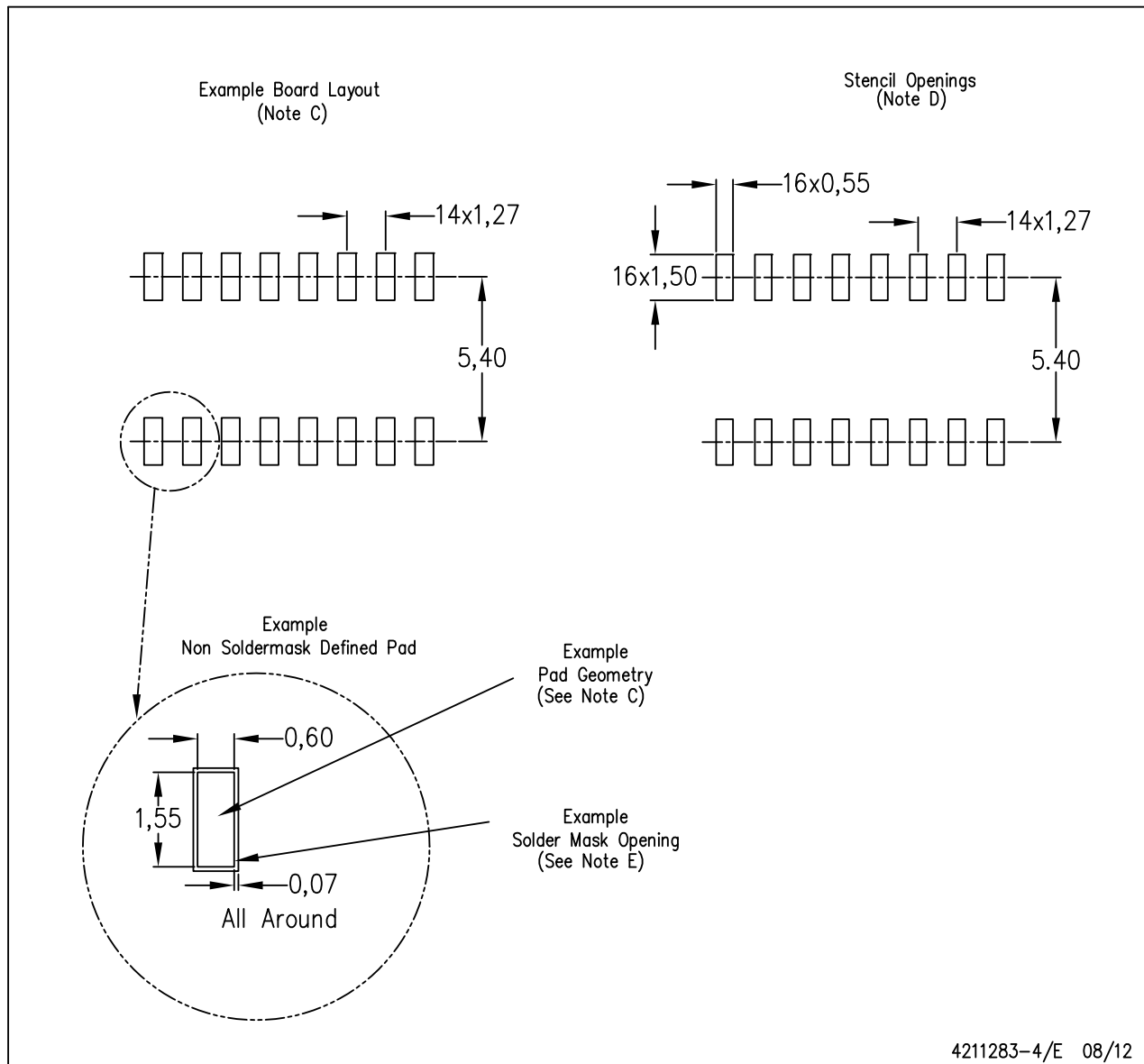
**NOTES:**

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

## LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

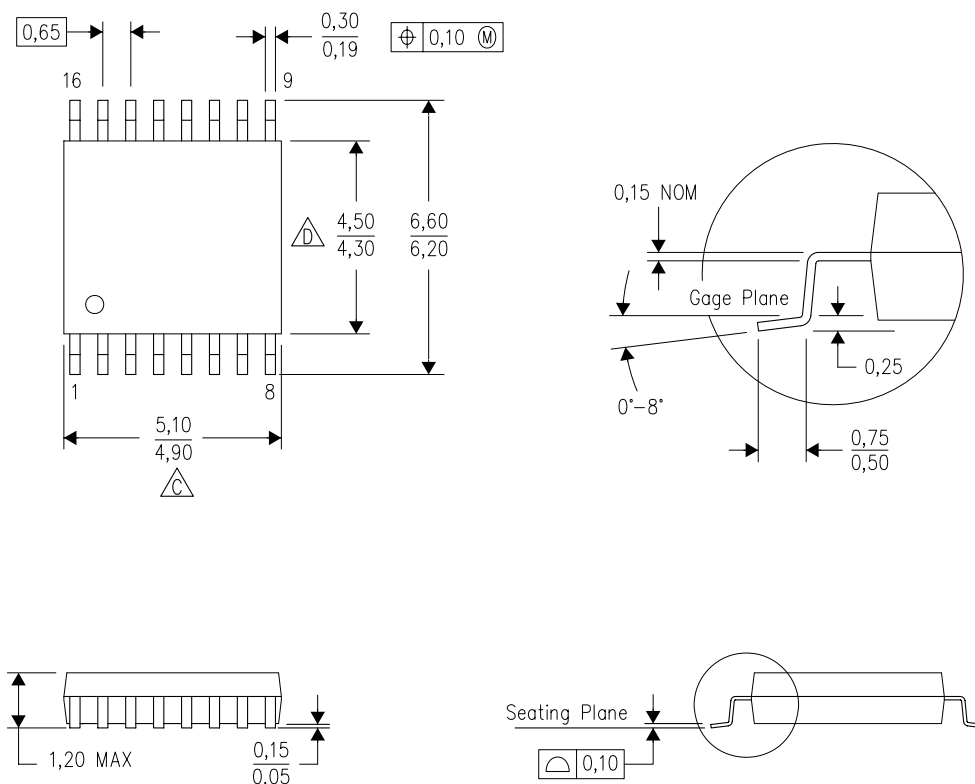


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## MECHANICAL DATA

PW (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



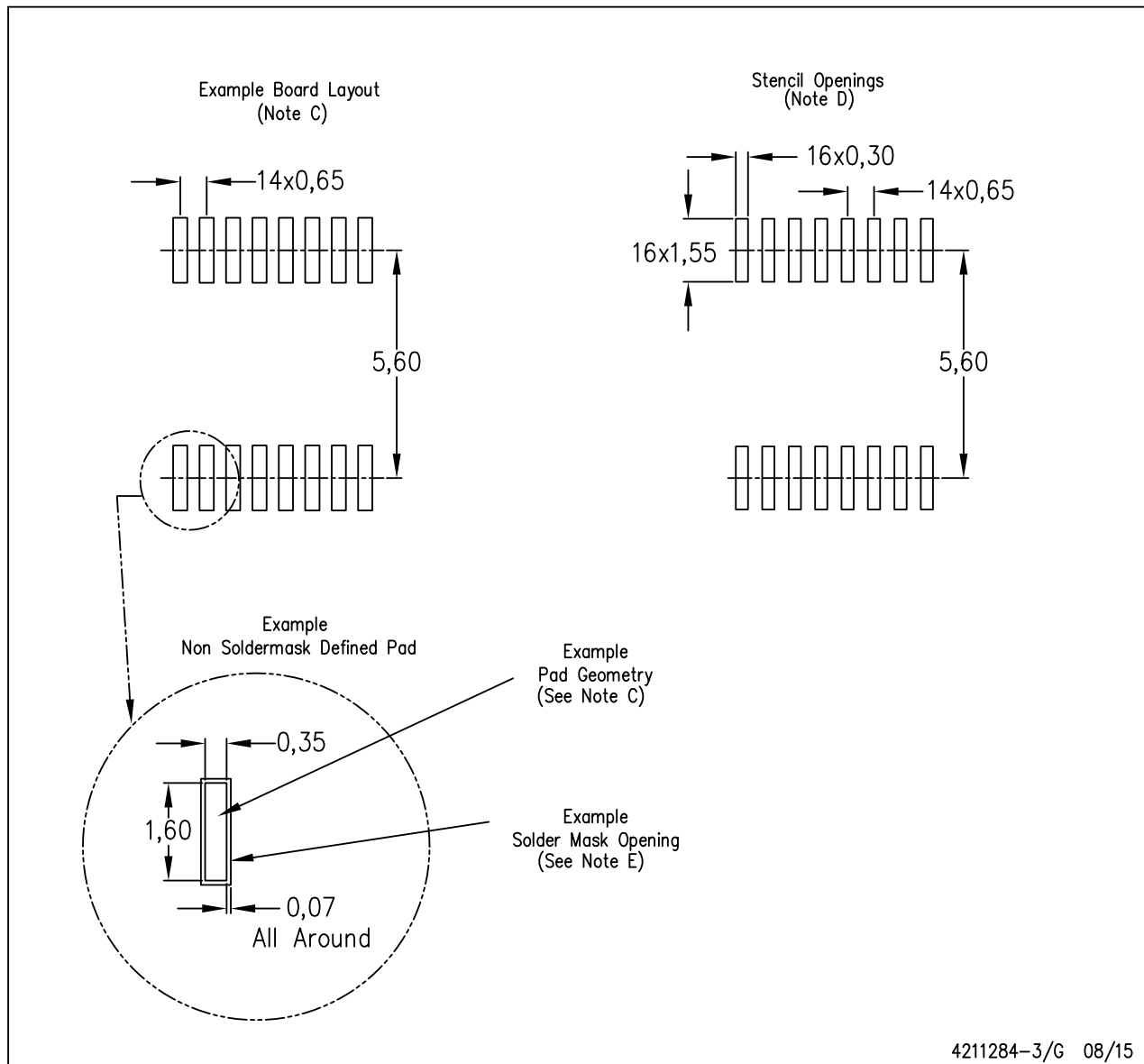
4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

## LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



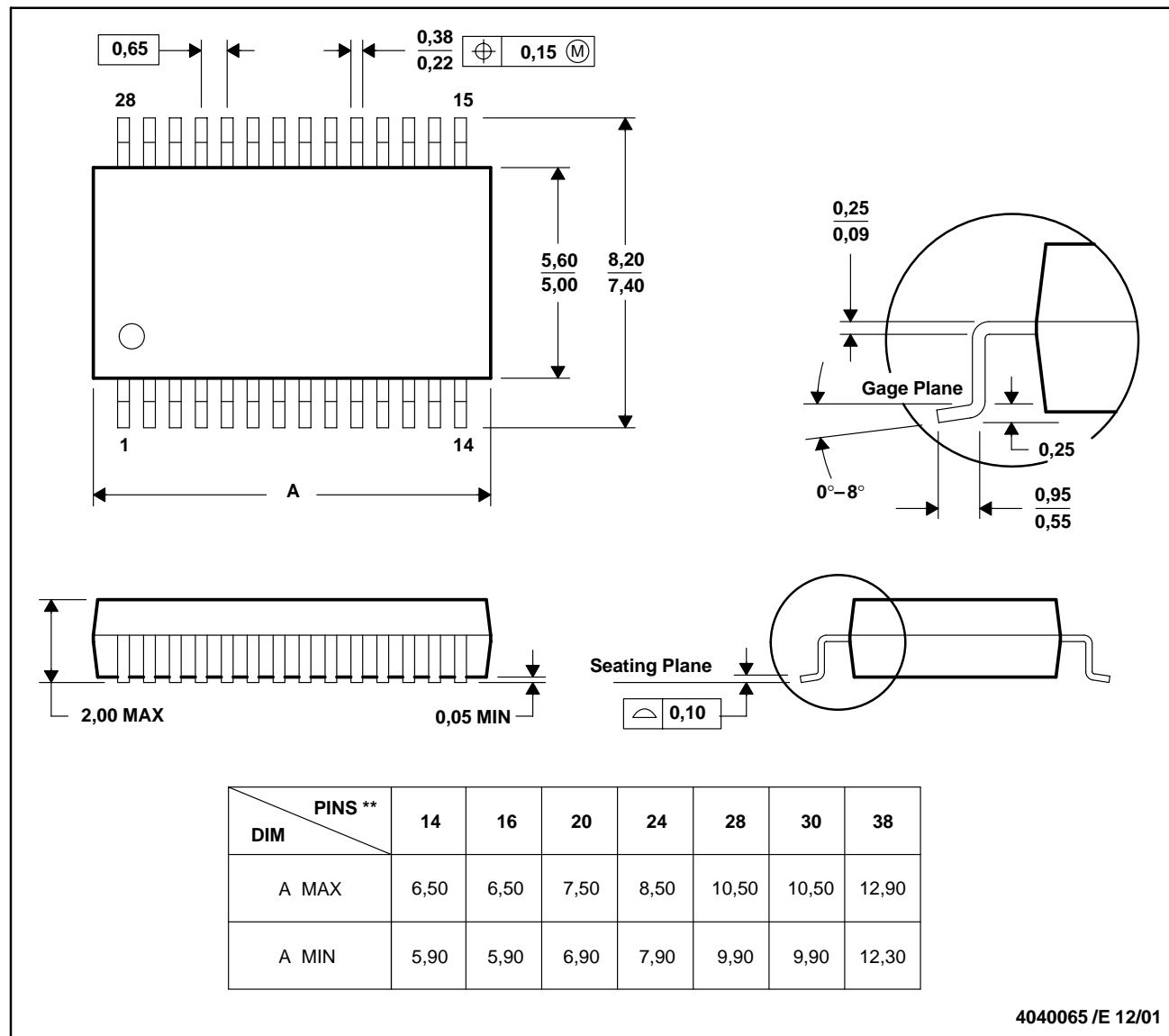
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



**TEXAS  
INSTRUMENTS**

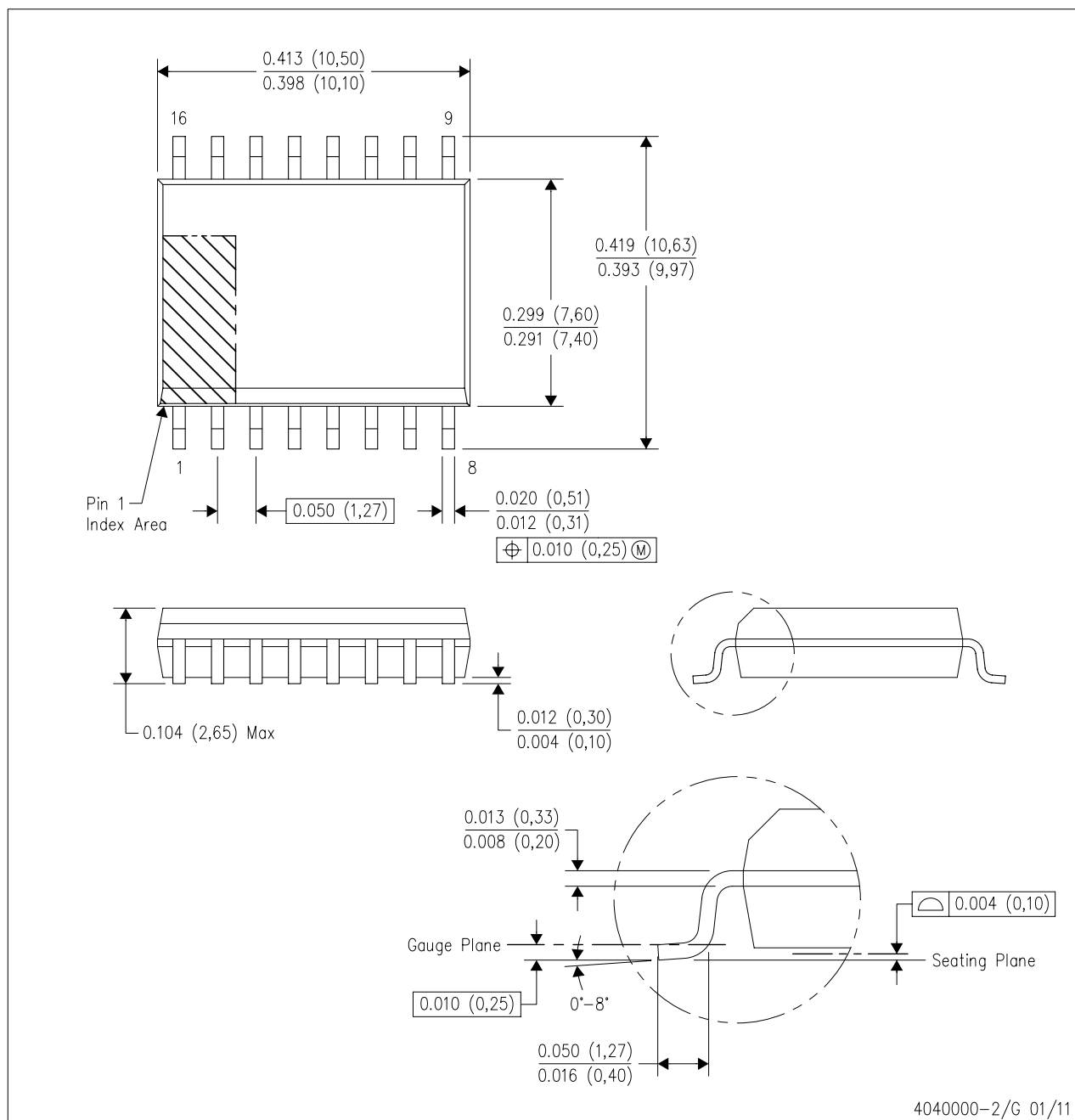
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## MECHANICAL DATA

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



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Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
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