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Technical Note

512Mb Mobile DDR: 95nm to 78nm Product Transition Guide

Introduction

This document describes critical product differences associated with the 512Mb Mobile (LP) DDR SDRAM product as it transitions from 95nm process technology to 78nm process technology. Micron makes every effort to ensure that new replacement products have full functional compatibility with previous products. This is accomplished through design, ATE characterization, and target system validation when possible. It is therefore unlikely that a system that has been designed with a Micron LP DDR SDRAM product will have any problems with a Micron replacement product. Micron does recommend, however, that the target system design be fully evaluated with the final version of the new product prior to conversion.

Part Number Transition

Examples of replacement part numbers are shown in Table 1. These numbers are reflected in the data sheet for the replacement product.

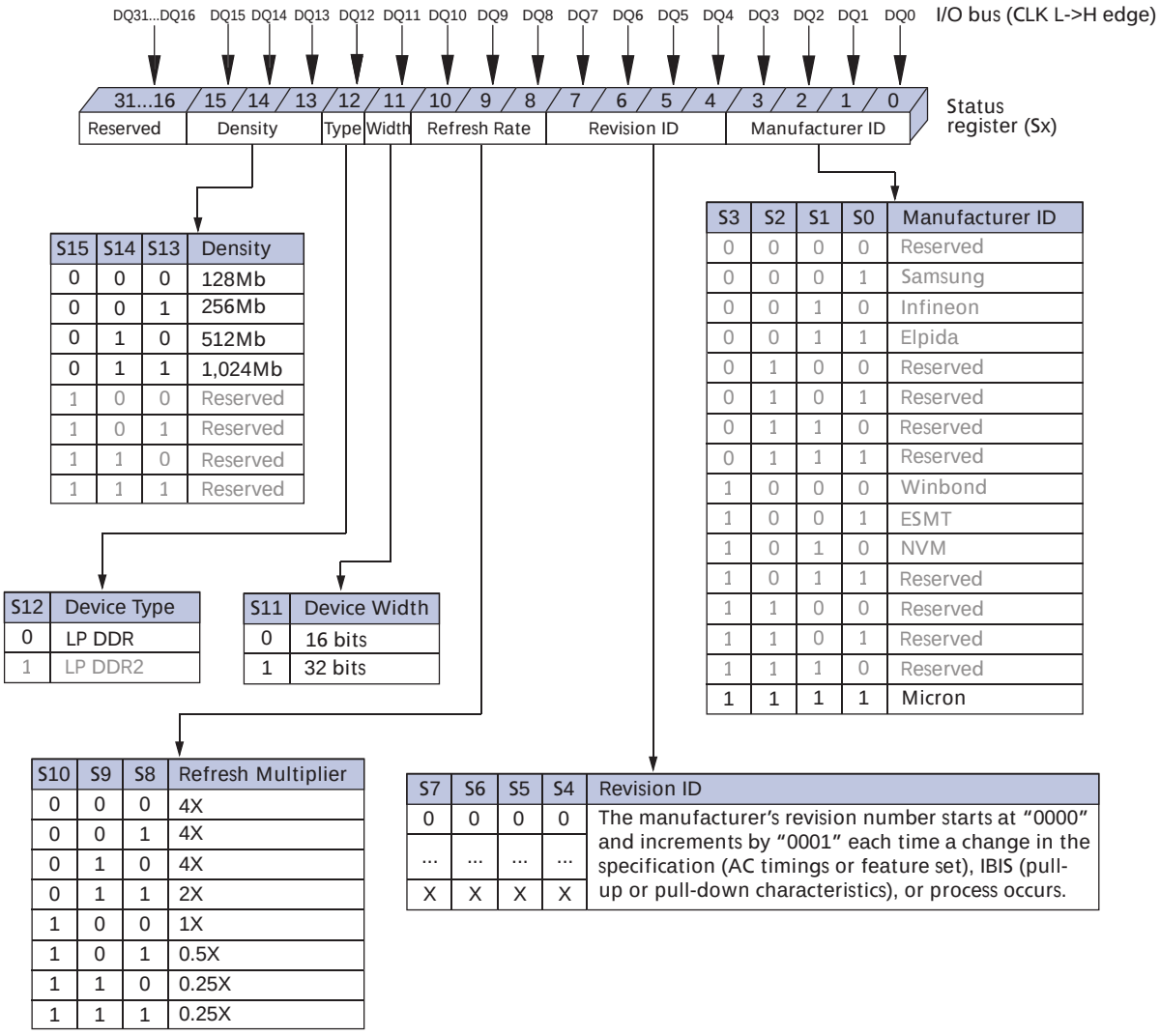
Table 1: Part Number Replacement Examples

95nm Part Number	78nm Part Number
MT46H16M32LFCM-6	MT46H16M32LFCM-6:B
MT46H16M32LFCM-6 IT	MT46H16M32LFCM-6 IT:B
MT46H16M32LFCM-75	MT46H16M32LFCM-6:B
MT46H16M32LFCM-75 IT	MT46H16M32LFCM-6 IT:B
MT46H32M16LFCK-6	MT46H32M16LFBF-6:B
MT46H32M16LFCK-6 IT	MT46H32M16LFBF-6 IT:B
MT46H32M16LFCK-75	MT46H32M16LFBF-6:B
MT46H32M16LFCK-75 IT	MT46H32M16LFBF-6 IT:B

Status Read Register for 78nm Product

The status read register (SRR) has been added to the 78nm product. It is used to read the manufacturer ID, revision ID, refresh multiplier, width, type, and density of the Mobile SDRAM, as shown in Figure 1 on page 2. The information made available from this read-only register can assist the component package manufacturer. It can also be useful for product operation in the target application. The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. Consult the 78nm product data sheet for a full description of the SRR operation.

Figure 1: Status Read Register



S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	1,024Mb
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Reserved
0	0	0	1	Samsung
0	0	1	0	Infineon
0	0	1	1	Elpida
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	NVM
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Micron

S12	Device Type
0	LP DDR
1	LP DDR2

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier
0	0	0	4X
0	0	1	4X
0	1	0	4X
0	1	1	2X
1	0	0	1X
1	0	1	0.5X
1	1	0	0.25X
1	1	1	0.25X

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer's revision number starts at "0000" and increments by "0001" each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
...	...	...	...	
X	X	X	X	

AC Timing and DC Specification Differences

The 78nm product supports the same speed grades as the 95nm product and will meet or exceed all timing parameters. The 78nm product also meets or exceeds all JEDEC-standard LP DDR I/O level parameters as does the 95nm product.

Some DC specifications may vary between the 95nm and 78nm products. Consult the product data sheets for specific values.

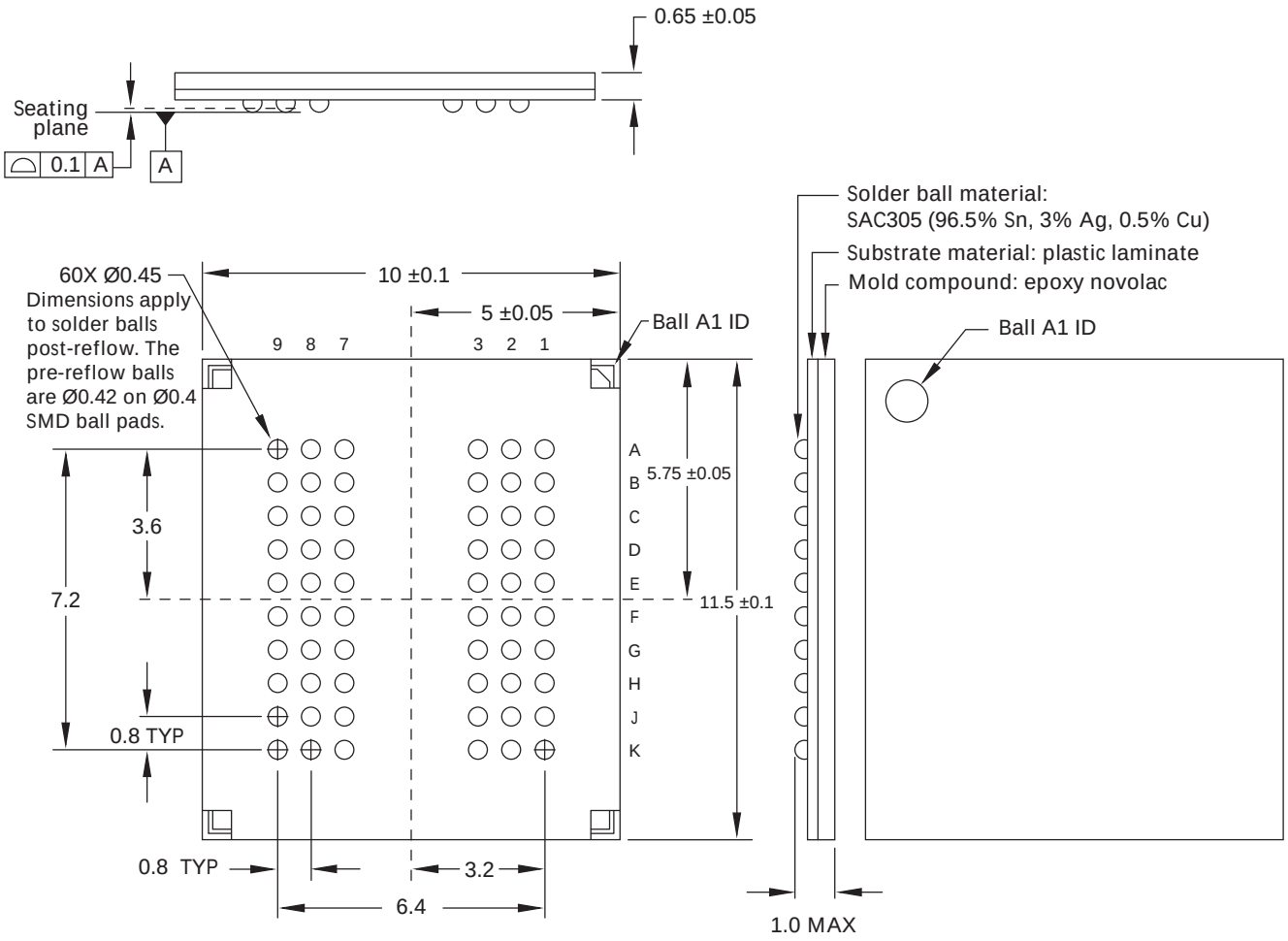
Package Differences

The 95nm, x16 and x32 products use SAC305 package solder ball composition, as shown in Figure 2.

Both the x16 (60-ball) and the x32 (90-ball) packages for the 78nm product use SAC105 solder ball composition. This aligns with the industry trend toward SAC105 composition for enhanced drop test performance. The surface mount conditions for SAC105 are the same as for SAC305.

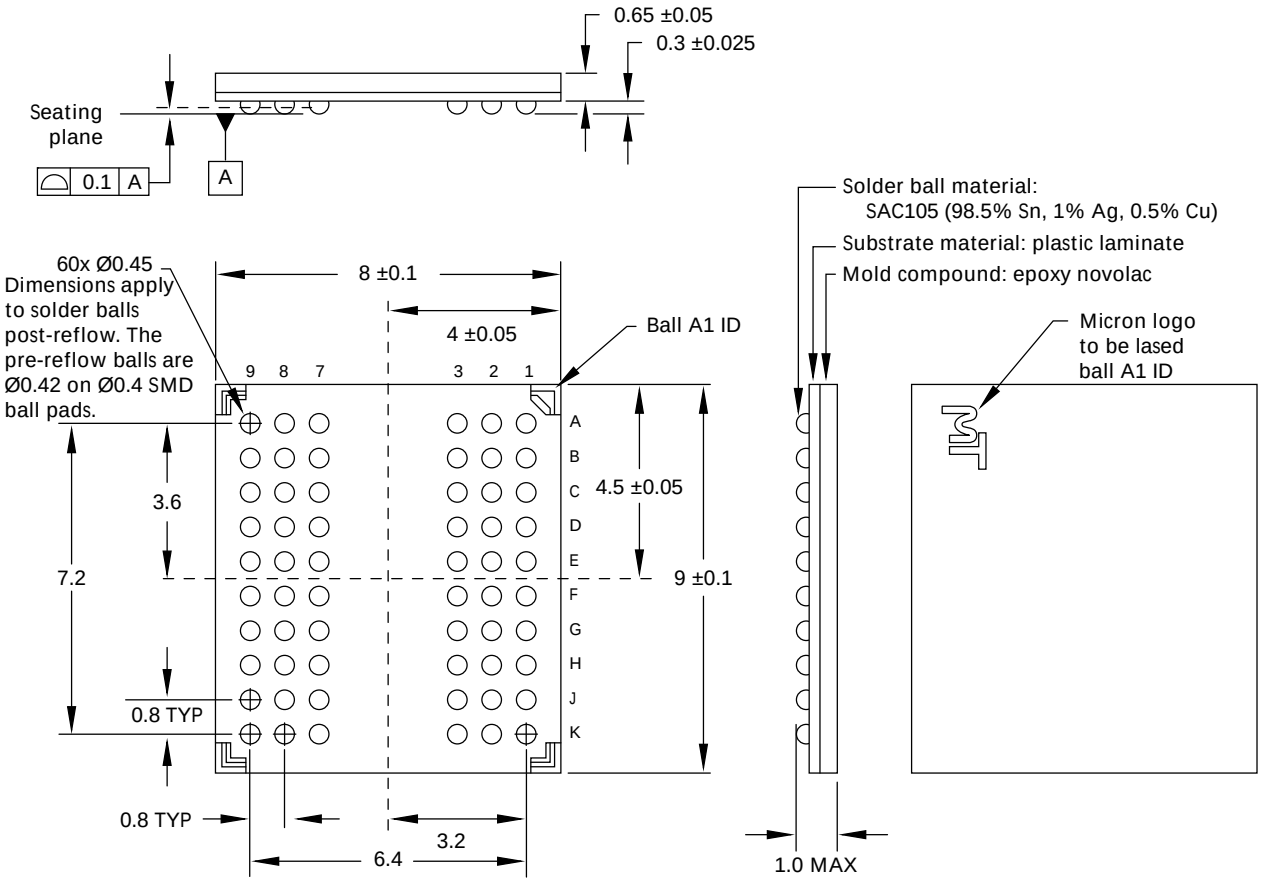
In addition, the 78nm, x16 product offers a smaller, 8mm x 9mm package outline to conserve application board space, as shown in Figure 3 on page 4. The ball assignments for both 78nm packages are JEDEC compliant.

Figure 2: Previous 95nm, x16, 10mm x 11mm, 60-ball VFBGA



Notes: 1. Dimensions are in millimeters.

Figure 3: New 78nm, x16, 8 x 9mm, 60-ball VFBGA



Notes: 1. Dimensions are in millimeters.

Die Bond Pad Order Changes

The 78nm, JEDEC-standard bond pad order is noticeably different from the 95nm bond pad order. An example of the differences for the x16 double-sided configuration is shown in Table 2 on page 5.

The JEDEC pad ordering guidelines do not specify exact placement requirements. Therefore, they do not guarantee bonding compatibility among vendors. Compatibility can be verified by direct comparison of die data sheet bond pad information.

Table 2: Bond Pad Order Comparison[1]

95nm, Double-Sided x16		78nm, Double-Sided x16	
VDD	VDD	VSS	VSS
VSS	VSS	VDD	VDD
VDD	TQ	TEST	TQ
VSS	VDDQ	High-Z	VDDQ
VDD	VSSQ	VSS	VSSQ
BOND_OPT	VDDQ	BOND_OPT	VSSQ
VSS	VSSQ	VDD	VDDQ
CS#	VDD	A4	VDDQ
A0	VSS	A5	VSSQ
A1	DQ15	A6	DQ15
A2	DQ14	A7	DQ14
A3	VDDQ	A8	DQ13
A4	VSSQ	A9	DQ12
A5	DQ13	A11	VSSQ
A6	DQ12	A12	VDDQ
CKE	DQ11	VDD	DQ11
CAS#	DQ10	VSS	DQ10
RAS#	VDDQ	CKE	DQ9
VDD	VSSQ	WE#	DQ8
VSS	DQ9	CAS#	VDDQ
BA1	DQ8	RAS#	VSSQ
BA0	UDQS	CS#	UDQS
WE#	UDM	BA1	UDM
A7	VDD	BA0	VSS
A8	BOND_OPT	A10/AP	VDD
A9	VSS	A0	CK
A10	VSS	A1	CK#
A11	CK#	A2	VDD
A12	CK	A3	VSS
VSS	VDD	VDD	LDM
VDD	VSS	VSS	LDQS
VSS	CK#	VDD	VSSQ
VDD	CK	VSS	VDDQ
High-Z	VDD		DQ7
VSS	VSS		DQ6
VDD	VDD		DQ5
	LDM		DQ4
	LDQS		VDDQ
	DQ7		VSSQ
	DQ6		DQ3
	DQ5		DQ2
	DQ4		DQ1
	DQ3		DQ0
	DQ2		VSSQ
	DQ1		VDDQ
	DQ0		VDDQ
	VSS		VSSQ
	VDD		VSSQ
	VSSQ		VDDQ
	VDDQ		VDD
	VSSQ		VSS
	VDDQ		
	TEST		
	High-Z		
	VSS		

Notes: 1. Blue cells indicate bond pad order differences.

For high-speed applications that use the single-sided configuration, special bonding recommendations are provided in the part-specific die data sheet.

Summary

Micron periodically offers product performance improvements through process node migration. This is the case with the product transition from 95nm to 78nm. Designers should consult product data sheets for detailed information on product differences before proceeding with product transitions.

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