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ADP1828LC-EVALZ

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ANALOG DEVICES

5 A Evaluation Board for Step-Down DC-to-DC Controller

EVAL-ADP1828LC

EVALUATION BOARD DESCRIPTION

This data sheet describes the design, operation, and test results of the ADP1828 5 A evaluation board. The input range for this evaluation board is 5.5 V to 13.2 V, and the output voltage is 1.8 V with a maximum load current of 5 A. For this design, a switching frequency (f_{SW}) of 600 kHz is chosen to achieve a good balance between efficiency and the sizes of the power components.

ADP1828 DEVICE DESCRIPTION

The ADP1828 is a synchronous PWM voltage mode buck controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The ADP1828 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, as well as general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. It operates from an input voltage of 3 V to 18 V with an internal LDO that generates a 5 V output for a V_{IN} of 5.5 V to 18 V.

The ADP1828 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, or at any frequency between 300 kHz and 600 kHz if a resistor is used. The frequency can also be synchronized to an external clock up to 2× the switching frequency. The clock output can be used for synchronizing the ADP1828 or another part, such as the ADP1829, thus eliminating the need for an external clock source. The ADP1828 includes soft start protection (to limit inrush current from the input supply during startup), reverse current protection during soft start for a precharged output, voltage tracking, power good, as well as an adjustable lossless current-limit scheme utilizing external MOSFET sensing. The ADP1828 is offered in a 20-lead QSOP package.

DIGITAL PICTURE OF THE BOARD

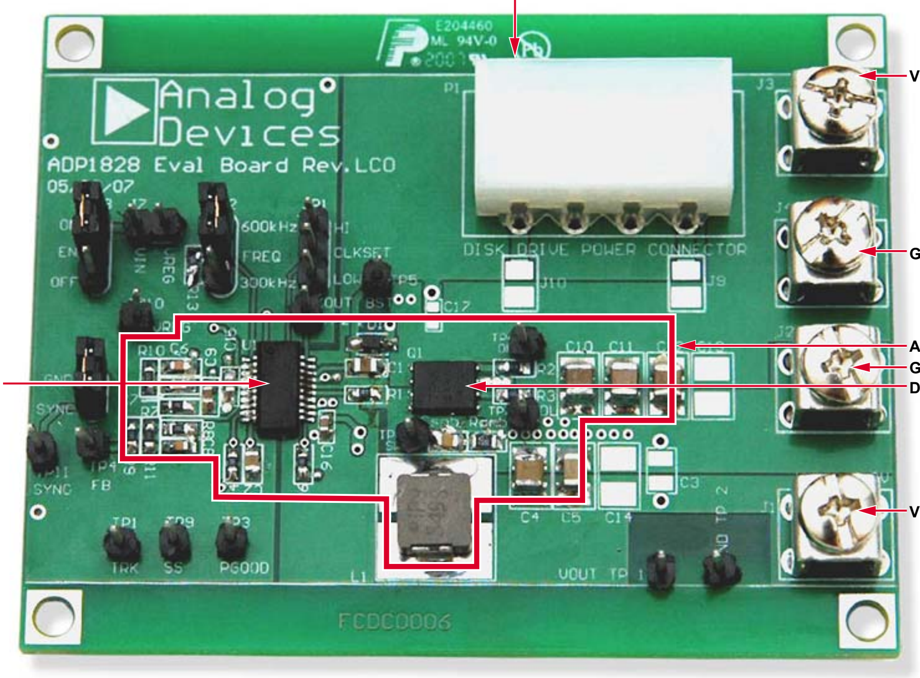

Figure 1. ADP1828 5 A Evaluation Board

Rev. 0

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REVISION HISTORY

8/07—Revision 0: Initial Version

COMPONENT DESIGN

For information about selecting power components and calculating component values, see the ADP1828 data sheet.

INPUT CAPACITOR

Ceramic capacitors have very low ESR (in the order of 1 mΩ or 2 mΩ) and have large ripple current rating. For a 5 A output with a V_{IN} of 6 V to13.2 V and a V_{OUT} of 1.8 V, three 22 µF ceramic capacitors (22 µF/16 V/X5R/1210) are adequate.

INDUCTOR SELECTION

For this design, a 1.8 µH inductor (FDV0630-1R8M from Toko Inc.) is selected. This is a compact, low-cost inductor with an iron powder core, which generally has more core power loss but at a lower cost than the ones with ferrite cores.

OUTPUT CAPACITOR SELECTION

The output voltage ripple can be approximated as follows:

$$\Delta V_{OUT} = \Delta I_L \sqrt{ESR^2 + \left(\frac{1}{8 f_{SW} C_{OUT}}\right)^2 + (4 f_{SW} ESL)^2} \quad (1)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the output capacitor.
ESL is the equivalent series inductance of the output capacitor.

A minimum capacitance at the output is needed to achieve a fast load-step response and a reasonable overshoot voltage. The minimum capacitance can be calculated as

$$C_{OUT,min1} = \frac{\Delta I_{LOAD}{}^2 L}{2 V_{OUT} \Delta V_{up}} \quad (2)$$

$$C_{OUT,min2} = \frac{\Delta I_{LOAD}{}^2 L}{2(V_{IN} - V_{OUT}) \Delta V_{down}} \quad (3)$$

where:
ΔI_{LOAD} is the step load.
ΔV_{up} is the output voltage overshoot when the load is stepped down.
ΔV_{down} is the output voltage overshoot when the load is stepped up.
V_{IN} is the input voltage.
$C_{OUT,min1}$ is the minimum capacitance according to the overshoot voltage ΔV_{up}.
$C_{OUT,min2}$ is the minimum capacitance according to the overshoot voltage ΔV_{down}.

Select an output capacitance that is greater than both $C_{OUT,\,min1}$ and $C_{OUT,\,min2}$.

In this design, multilayer ceramic capacitors (MLCCs) are used. Because MLCCs have very low ESR and ESL, the output ripple is dominated by the bulk capacitance. Two output ceramic capacitors (100 µF/6.3 V/X5R/1210 and 47 µF/6.3 V/X5R/1206) have been selected to satisfy a 5 A step load. Keep in mind that the effective capacitance of the ceramic capacitor decreases as the bias voltage increases.

MOSFET SELECTION

In general, select the high-side MOSFET with fast rise and fall times and low input capacitance. Fast rise and fall times and low input capacitance are especially important for circuits with low duty cycles because switching loss is high. Select the low-side MOSFET with low R_{DSON}. Switching speed is not critical because there is no switching loss in the low-side MOSFET. A small amount of power is lost in the body diode of the low-side MOSFET during the dead time.

For this evaluation board, a dual FET in a PowerPAK® SO-8 (Si7958DP from Vishay) has been selected. The PowerPAK SO-8 has a low thermal resistance, θ_{JA}, and is adequate for handling a 5 A output. An alternative is to use two single MOSFETs in standard SO-8 packages. Furthermore, for an output current less than 3 A, a dual FET in a standard SO-8 package is usually adequate.

SOFT START

The soft start period is given by the following equation:

$$C_{SS} = 8.015 \times t_{SS} \quad (4)$$

where:
C_{SS} is the soft start capacitance in microfarads.
t_{SS} is the soft start period in seconds.

A C_{SS} of 150 nF, which yields a 19 ms soft start period, is chosen for this design.

CURRENT LIMIT

The external current-limit resistor can be calculated by the following equation:

$$R_{CL} = \frac{\left(I_{LIMIT} + \frac{\Delta I_L}{2}\right) R_{DSON} - 38 \text{ mV}}{42 \text{ µA}} \quad (5)$$

where:
I_{LIMIT} is the output limit current.
ΔI_L is the ripple current in the inductor.
R_{DSON} is the on resistance of the low-side MOSFET.
−38 mV is the CSL threshold voltage.

ΔI_L can be approximated by

$$\Delta I_L = \frac{V_{OUT}(1 - D)}{f_{SW} \times L} \quad (6)$$

where:
D is the duty cycle.
L is the inductance of the inductor.

In this design, R_{DSON} of the MOSFET Si7958DP is 20 mΩ with a VGS of 4.5 V. Because L is chosen to be 1.8 µH, ΔI_L is calculated to be 1.4 A. If I_{LIMIT} is set to 6.5 A, RCL is calculated to be 2.88 kΩ. A standard value of 2.87 kΩ is chosen. Keep in mind that R_{DSON}

of the MOSFET can vary by more than 25% from part to part, and by more than 50% over the temperature range; therefore, the actual current limit can vary by more than 50% from part to part over the temperature range. For more information on this topic, see the ADP1828 data sheet.

SWITCHING NOISE AND OVERSHOOT REDUCTION

An RC snubber can be added between SW and PGND to reduce noise and ringing at the SW node and at the drains of the external MOSFETs. In this design, an RC snubber is added with an R_{SNUB} of 3.01 Ω and a C_{SNUB} of 1.2 nF. Gate resistors can be added to reduce overshoot voltage at the drains of the MOSFETs. For more information, see the ADP1828 data sheet.

COMPENSATION DESIGN

Type III compensation is used in this design because all output capacitors all ceramic with very low ESR. For information on calculating the compensation component values, refer to the ADP1828 data sheet.

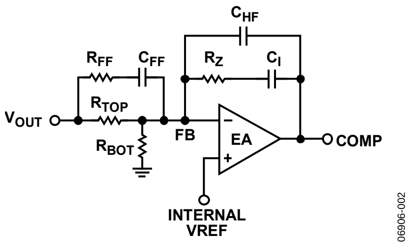

Figure 2. Type III Compensation

The compensation values for this evaluation board have been optimized as follows:

R_{FF} = 422 Ω
C_{FF} = 1 nF
R_Z = 7.5 kΩ
C_I = 3.9 nF
C_{HF} = 33 pF
R_{TOP} = 20 kΩ
R_{BOT} = 10 kΩ

TEST RESULTS

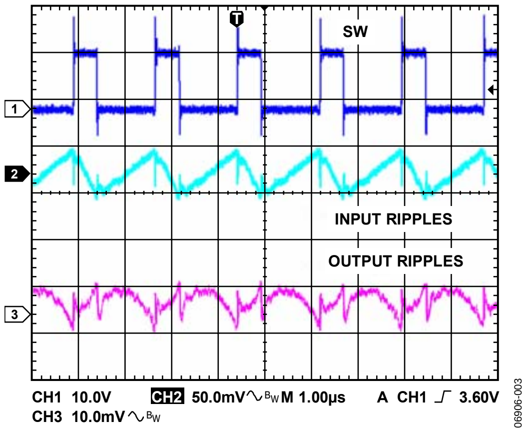

Figure 3. Output Ripple, V_{IN} = 12 V, Load = 5 A

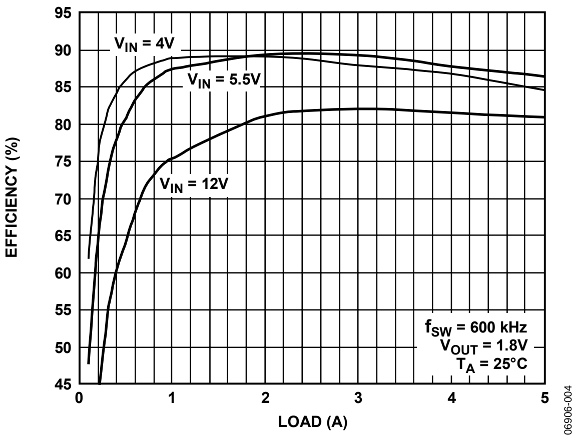

Figure 4. Efficiency vs. Load Current

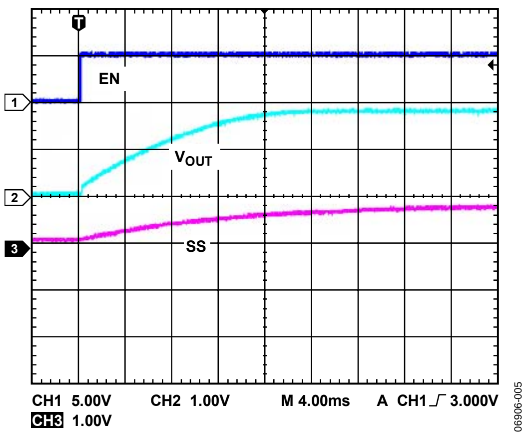

Figure 5. Soft Start, V_{IN} = 12 V

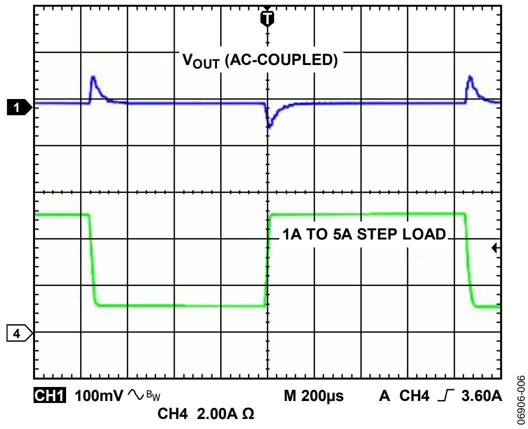

Figure 6. Load Transient, V_{IN} = 12 V, Load = 1 A to 5 A

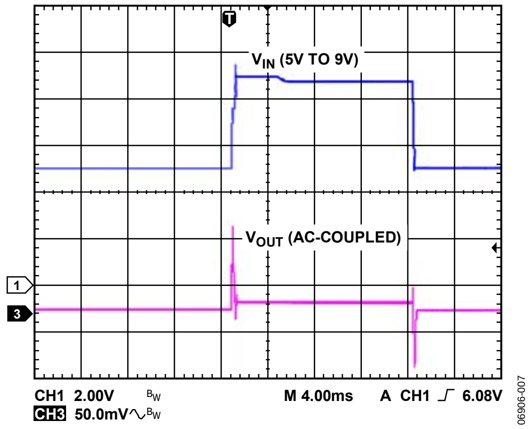

Figure 7. Line Transient, V_{IN} = 5 V to 9 V, No Load

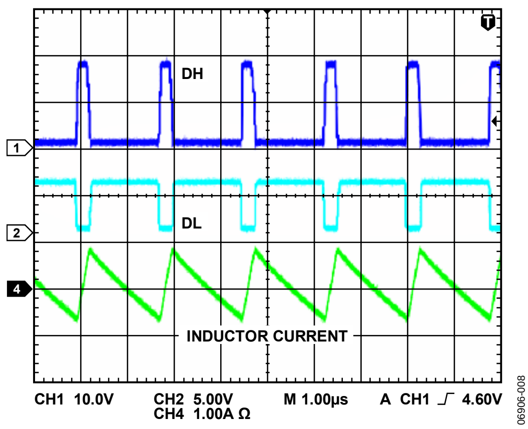

Figure 8. Inductor Current Waveform, V_{IN} = 12 V, No Load

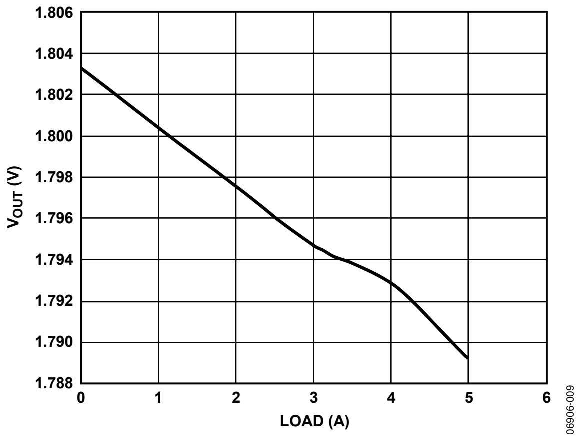

Figure 9. Load Regulation, V_{IN} = 12 V

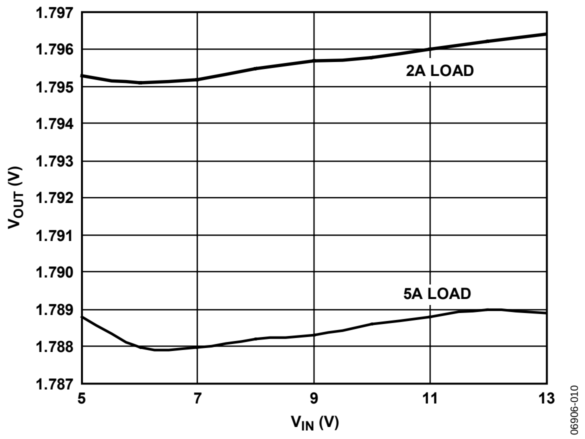

Figure 10. Line Regulation

EVALUATION BOARD OPERATING INSTRUCTIONS

1. Connect Jumper JP3 to the on position to enable the ADP1828.
2. Do not connect Jumper J7 (V_{IN} to VREG).
3. Connect Jumper JP2 (FREQ) to the 600 kHz position.
4. Connect Jumper J8 (SYNC) to GND (that is, if SYNC is not used). If SYNC is used, connect SYNC to an external clock or CLKOUT from another ADP1828.
5. Connect Jumper JP1 (CLKSET) to high, which sets CLKOUT to 2× the internal oscillator frequency and in phase with the oscillator, or to low, which sets CLKOUT to 1× the oscillator frequency and 180° out of phase.
6. Connect the positive terminal of the input power supply to the input terminal, J3.
7. Connect the load to the V_{OUT} terminal, J1.

Table 1. Jumper Descriptions

Jumper	Description	Function
JP1	CLKSET. Clock set input.	CLKSET = high sets CLKOUT to 2 × f_{OSC} CLKSET = low sets CLKOUT to 1 × f_{OSC}
JP2	Frequency selection. Connect to VREG for f_{SW} = 600 kHz.	VREG: f_{SW} = 600 kHz GND: f_{SW} = 300 kHz
JP3	EN. Connect to the on position to enable the ADP1828.	EN = on enables ADP1828 EN = off disables ADP1828
J7	VREG to V_{IN}. Do not connect this jumper when V_{IN} is greater than 5.5 V.	Short VREG to V_{IN} when V_{IN} is less than 5.5 V
J8	SYNC. Connect SYNC to GND if the SYNC function is not used. If SYNC is used, connect SYNC to an external clock or to the CLKOUT of another ADP1828.	Synchronization
J9	12 V supply from the disk drive connector. Short this jumper if the 12 V input supply comes from the disk drive connector. Do not short J9 and J10 at the same time.	12 V supply from disk drive
J10	5 V supply from the disk drive connector. Short this jumper if the 5 V input supply comes from the disk drive connector. Do not short J9 and J10 at the same time.	5 V supply from disk drive

Table 2. Evaluation Board Operating Conditions

Parameter	Condition
V_{IN}	Input range 5.5 V to 13.2 V.
V_{OUT}	V_{OUT} = 1.8 V at 5 A maximum output current.
f_{SW}	Switching frequency is set to 600 kHz.
Maximum Step Load	This design can handle a 0 A to 5 A step load at the output. The output capacitance can be reduced if a 5 A step load is not required.

Table 3. Temperature of the Power Components[1, 2]

ADP1828	Inductor (Toko FDV0630-1R8M)	MOSFETs (Vishay Si7958DP)
50°C	60°C	60°C

[1] After the evaluation board ran for 30 minutes at a 5 A load, the surface temperatures of the power components were measured with an infrared thermometer.
[2] V_{IN} = 12 V, T_A = 25°C.

Table 4. Miscellaneous Information

Parameter	Comment
Switching Frequency, f_{SW}	The switching frequency, f_{SW}, is set to 600 kHz (Jumper JP2) on the evaluation board. If a different f_{SW} is needed, the compensation and the power components need to be recalculated. If a f_{SW} other than 300 kHz or 600 kHz is desired, a resistor, R13, can be soldered onto the PCB to select any frequency between 300 kHz and 600 kHz.
Dual Power MOSFETs: Q1A and Q1B	The footprint for the dual power MOSFETs is laid out to fit both the PowerPAK SO-8 and the standard SO-8 package so that the user can easily replace the on-board PowerPAK with a standard SO-8 package.
Inductor	The footprint for the inductor is laid out to fit inductors that are smaller or larger than the on-board inductor, Toko FDV0630.
VREG and V_{IN}	For input voltages less than 5.5 V, the user can connect Jumper J7 by shorting VREG to V_{IN}.
Snubber Circuit	A snubber RC circuit, R_{SNUB} and C_{SNUB}, is laid out on the evaluation board to help reduce switching noise and ringing at the SW node. The user can remove this RC snubber or try different RC values for a particular application. Keep in mind that the RC snubber dissipates power and slightly reduces the overall efficiency, generally in the range of 0.1% to 0.5%.
Gate Resistors	The dummy 0 Ω gate resistors, R2 and R3, at DH and DL, respectively, are provided on the evaluation board for reducing overshoot voltage at the drains of the external MOSFETs. The user can change these 0 Ω resistors to different values (generally in the range of 1 Ω to 5 Ω) to achieve the desired reduction in overshoot voltage. Keep in mind that the gate resistor dissipates power and slightly reduces the overall efficiency.
Capacitor C17	A ceramic capacitor, C17, is placed very close to the drain of the high-side MOSFET. This capacitor, typically 0.1 µF to 1 µF, helps to reduce input impedance during high frequency transients. C17 is not assembled on the evaluation board. The user can add this capacitor if needed for a particular application.
Voltage Divider	If a different output voltage other than 1.8 V is desired, the user needs to change the voltage feedback divider, R7 and R8, and rework the compensation component values and the input and output capacitances.

EVALUATION BOARD SCHEMATIC

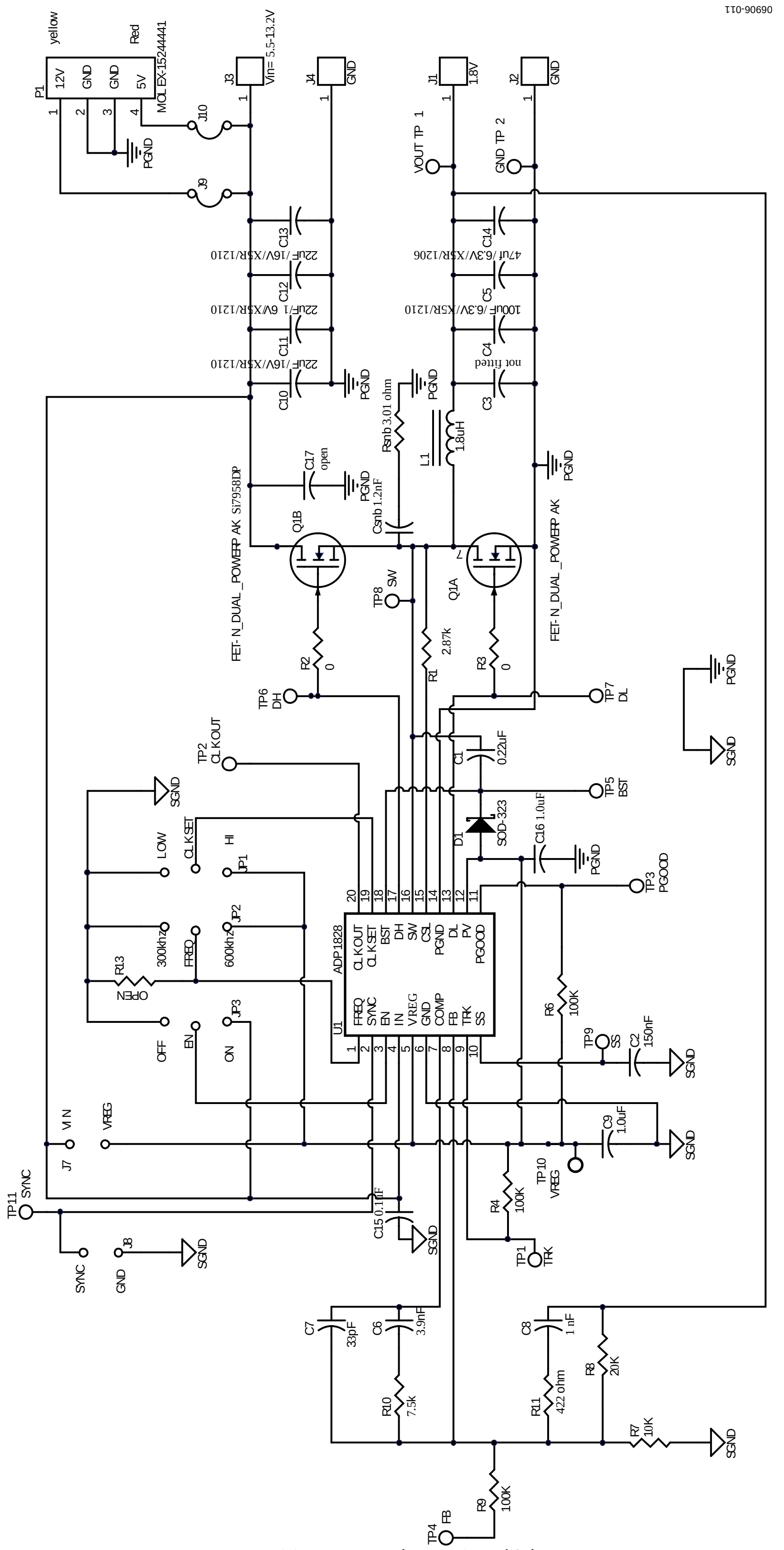

Figure 11. ADP1828 5 A Evaluation Board Schematic

EVAL-ADP1828LC

EVALUATION BOARD LAYOUT

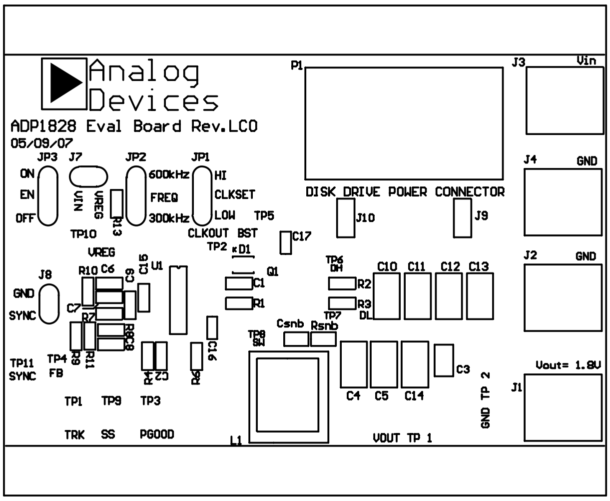

Figure 12. Silkscreen Layer

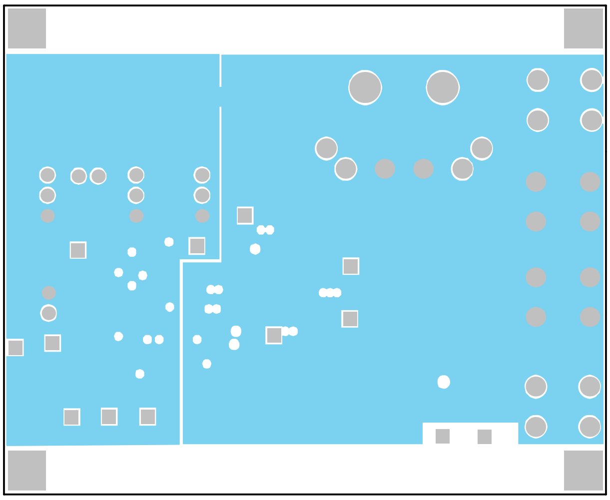

Figure 15. Third Layer (GND Layer)

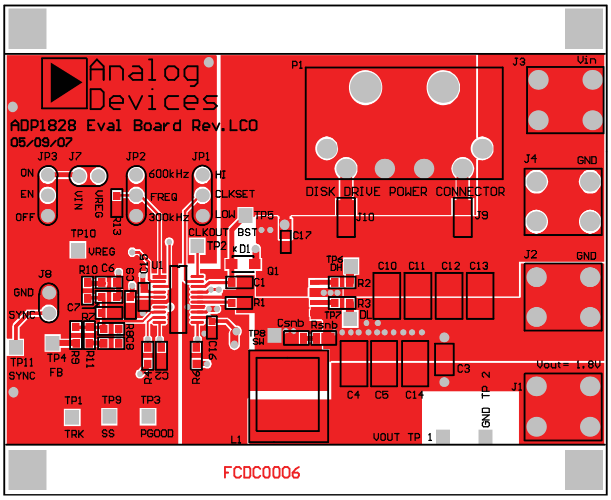

Figure 13. Top Layer

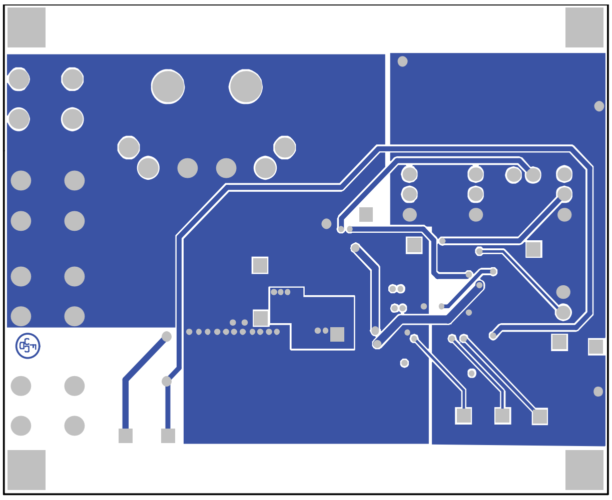

Figure 16. Bottom Layer

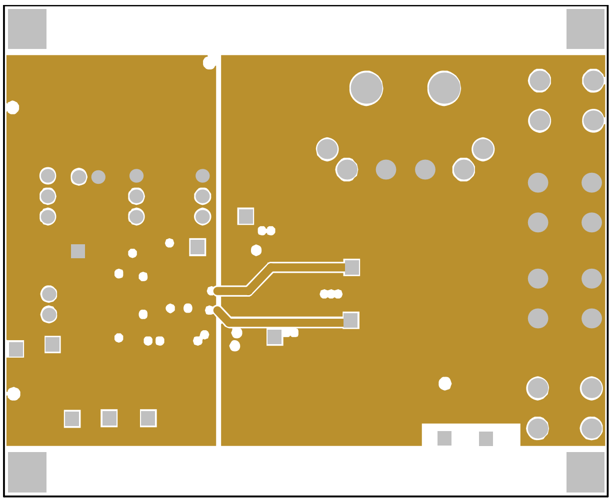

Figure 14. Second Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Component Listing

Item	Qty	Designator	Description	Manufacturer	Part No.
1	3	C10, C11, C12	Capacitor, ceramic, 22 μF, 16 V, X5R, 1210	Murata	GRM32ER61C226KE20
2	1	C4	Capacitor, ceramic, 100 μF, 6.3 V, X5R, 1210	Murata	GRM32ER60J107ME20
3	1	C5	Capacitor, ceramic, 47 μF, 6.3 V, X5R, 1206	Murata	GRM31CR60J476ME20
4	1	C2	Capacitor, ceramic, 150 nF, 16 V, X7R, 0603	Vishay	VJ0603Y154KXJA
5	1	C15	Capacitor, ceramic, 0.1 μF, 6.3 V, X5R, 0603	Vishay	VJ0603Y104MXQ
6	1	C1	Capacitor, ceramic, 0.22 μF, 10 V, X5R, 0603	Taiyo Yuden Murata	TMK107BJ224MA-T GRM188R61A224KA61
7	4	R2, R3, R5, R12	Resistor (dummy), 0 Ω, 1/10 W, 1%, 0603	Vishay	CRCW06030R00F
8	1	R8	Resistor, 20 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06032002F
9	1	R7	Resistor, 10 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031002F
10	1	R11	Resistor, 422 Ω, 1/10 W, 1%, 0603/0402	Vishay	CRCW06034220F
11	1	R10	Resistor, 7.5 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06037501F
12	3	R4, R6, R9	Resistor, 100 kΩ, 1/10 W, 1%, 0603	Vishay	CRCW06031003F
13	1	R1	Resistor, 2.87 kΩ, 1/10 W, 1%, 0603 (current-limit resistor)	Vishay	CRCW06032801F
14	1	Rsnb	Resistor, 3.01 Ω, 0805	Vishay	CRCW08053R01F
15	1	Csnb	Capacitor, ceramic, 1.2 nF, 0805	Vishay	VJ0603Y122KXXA
16	1	C8	Capacitor, ceramic, 1 nF, 0603	Vishay	VJ0603Y102KXXA
17	1	C7	Capacitor, ceramic, 33 pF, 0603	Vishay	VJ0603A330KXXA
18	1	C6	Capacitor, ceramic, 3.9 nF, 0603	Vishay	VJ0603Y392KXXA
19	2	C9, C16	Capacitor, ceramic, 1.0 μF, 10 V, X5R, 0603	Taiyo Yuden Murata	LMK107BJ105MK-T GRM185R61A105KE36
20	1	L1	Inductor, 1.8 μH, 18 mΩ, 6.6 A, iron powder core (Alternative: 2.0 μH, 16 mΩ, 6.5 A, flat wire)	Toko (Würth Elektronik)	FDV0630-1R8M (744310200)
21	1	D1	Schottky diode, 30 V, V_F = 0.5 V @ 30 mA, SOD-323	Vishay	BAT54WS
22	1	Q1A, Q1B	Transistor, N-MOSFET, 40 V, PowerPAK SO-8, 20 mΩ @ 4.5 V	Vishay	Si7958DP
23	1	P1	Disk drive power connector	Molex Inc.	15244441
24	3	JP1, JP2, JP3	3-terminal jumpers, 0.1" spacing	Any	
25	1	J8	2-terminal jumper, 0.1" spacing	Any	
26	13	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, VOUT TP 1, GND TP 2	Test points for VREG, SW, DH, DL, TRK, SS, PGOOD, BST, FB, SYNC, CLKOUT, GND, VOUT	Any	40 mil (1 mm) through hole
27	1	U1	DUT, 10-lead QSOP	Analog Devices	ADP1828

ORDERING GUIDE

Model	Description
ADP1828LC-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

EB06906-0-8/07(0)