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DS21458DK Quad T1/E1/J1 Transceiver Design Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21458DK is an easy-to-use evaluation board for the DS21458 quad T1/E1/J1 transceiver. The DS21458DK is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS21458DK comes complete with a DS21458 quad SCT, transformers, termination resistors, configuration switches, line-protection circuitry, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status. An on-board FPGA contains mux logic to connect framer ports to one another or to the DK2000 in a variety of configurations.

Each DS21458DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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DESIGN KIT CONTENTS

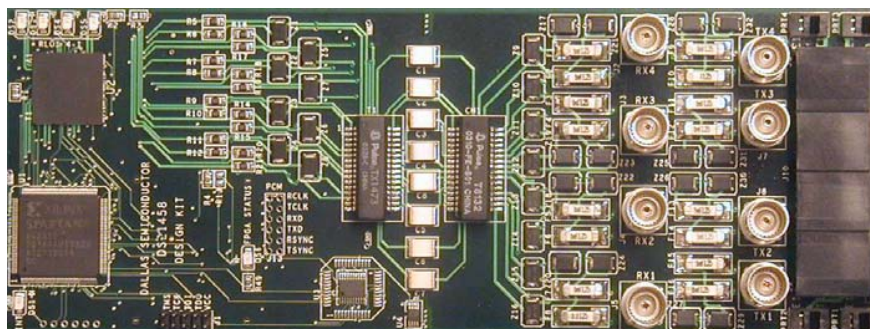
DS21458DK Design Kit Daughter Card
DK101 Low-Cost Motherboard
CD ROM
ChipView Software
DS21458DK Data Sheet
DK101 Data Sheet
DS21458 Data Sheet

FEATURES

- Demonstrates Key Functions of DS21458 Quad T1/E1/J1 Transceiver
- Includes DS21458 Quad LIU, Transformers, BNC and RJ45 Network Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21458 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal and Interrupt Status
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with all Connectors, Jumpers, and LEDs
- Network Interface Protection for Overvoltage and Overcurrent Events

ORDERING INFORMATION

PART	DESCRIPTION
DS21458DK	DS21458 Design Kit Daughter Card (with included DK101 Motherboard)



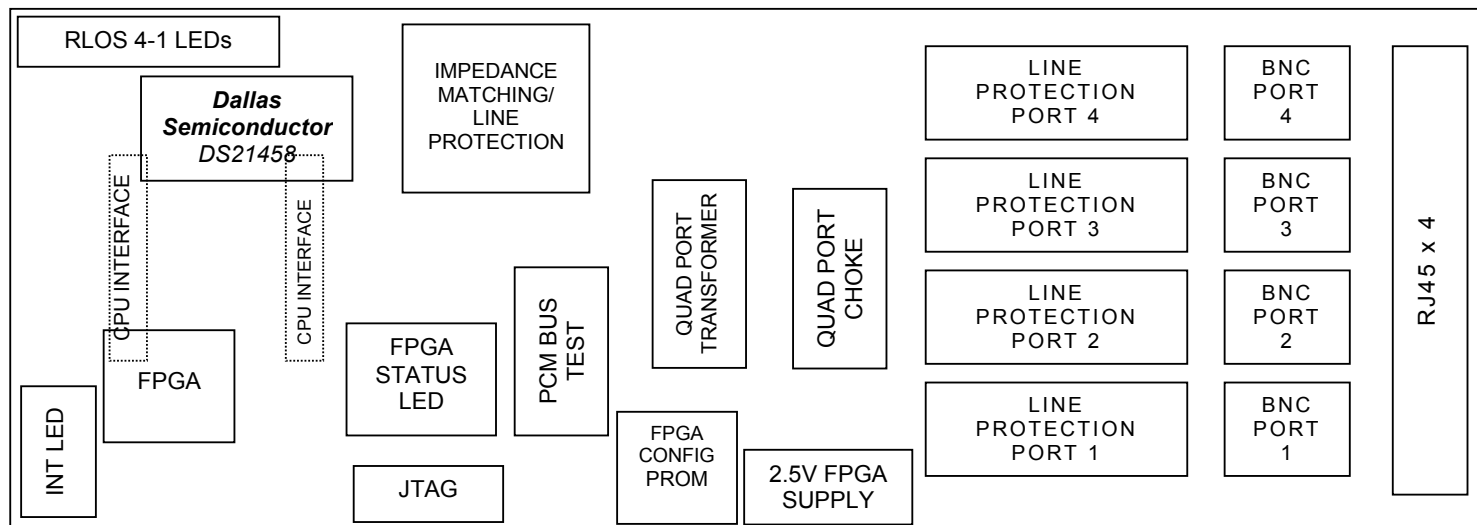
DS21458DK, Quad T1/E1/J1 Transceiver Design Kit Daughter Card

COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C8	8	0.22μF, 50V ceramic capacitors	Panasonic	PCF1152CT-ND
C9, C10, C12, C18, C22–C33, C35, C38–C43	23	0.1μF 10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C11, C13–C15	4	0.1μF 10%, 25V ceramic capacitors (1206)	Panasonic	ECJ-3VB1E104K
C16, C17, C19–C21, C34, C36, C45, C46	9	1μF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C37, C44	2	10μF 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CH1	1	Quad-port choke	Pulse Engineering	T8132
DS1	1	LED, red, SMD	Panasonic	LN1251C
DS2–DS6	5	LED, green, SMD	Panasonic	LN1351C
F1–F16	16	1.25A, 250V fuses, SMT	Teccor	F1250T
J1	1	10-pin connectors, dual row, vertical	Digi-Key	S2012-05-ND
J2–J9	8	5-pin BNC connectors, vertical	Cambridge	CP-BNCPC-004
J10	1	8-pin, 4-port jack Right-angle RJ45	Molex	43223-8140
J11, J12	2	50-pin sockets, SMD, dual row, vertical	Samtec	TFM-125-02-S-D-LC
J13	1	12-pin connector, dual row, vertical Not populated	Digi-Key	S2012-06-ND
J14	1	1Mbit flash-based configuration memory	Xilinx	XCF01SV020C
PRT1–PRT4	4	6-pin through-hole slide switches DPDT	Tyco	SSA22
R1, R2, R4, R26, R39, R41, R45	7	10kΩ 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ103V
R3, R27	2	1.0kΩ 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ102V
R5–R12, R14–R21, R48	17	0Ω 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R13, R47	2	Not populated	Panasonic	Not populated
R22–R25	4	51.1Ω 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEY51R1V
R29–R36	8	61.9Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R40, R42–R44, R46, R49	6	330Ω 5%, 1/10W MF resistors (0805)	Panasonic	ERA-6GEY331V
T1	1	SMT 32-pin octal T1/E1 transformer, transmit/receive, 1:2	Pulse Engineering	TX1473
U1	1	2.5V FPGA Spartan (Xilinx) 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U2	1	3.3V T1/E1/J1 quad transceiver 0°C to +70°C, 256-pin BGA	Dallas Semiconductor	DS21458
U3	1	1M PROM for FPGA 44-pin TQFP	Xilinx	Not populated
U4	1	8-pin μMAX, SO 2.5V or Adj	Maxim	MAX1792EUA25
Z1–Z8	8	50A, 6V Sidactor DO214 SMD	Teccor	P0080SAMC
Z9–Z16	8	500A, 25V Sidactor DO214 SMD	Teccor	P0300SCMC
Z17–Z32	16	500A, 170V Sidactor DO214 SMD	Teccor	P1800SCMC

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BOARD FLOORPLAN



BASIC CONFIGURATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS21458DK QuickView data sheet for these files.

Hardware Configuration

Using the DK101 Processor Board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector is unused. Additionally, the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception of the flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

Using the DK2000 Processor Board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply may be connected to connector J2.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

General

- Upon power-up, the RLOS LEDs (green) will not be lit, the INT LED (red) will not be lit, but the FPGA Status LED (green) will be lit.
- When operating in E1 mode, slide SW1–SW4 to E1 Mode (grounding the BNC shell). When operating in T1 mode, slide SW1–SW4 to T1 Mode.

Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA that is on the DS21458 daughter card.
- The definition file for this FPGA is named DS21458DC_FPGA.def. See [Table 2](#) for the FPGA Register Map definitions. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the *Basic Configuration* section.

Quick Setup (Demo Mode)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Demo Mode.
- The program will request a configuration file. Select among the displayed files, which are DS2155_E1_DSNCOM_DRVR.cfg or DS2155_T1_DSNCOM_DRVR.cfg.
- The Demo Mode screen will appear. Upon external loopback the RLOS indicators will turn green.
- Note: Demo Mode interacts with the device driver, which resides in the DK101/DK2000 firmware. The current implementation of this driver is for one device. As such, the demo mode will only interact with Port 1. With minor changes, the device driver is extendible to N devices.

Quick Setup (Register View)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will request a definition file. Select DS21458DC_FPGA.def through the Links section. This will also load DS21458DC.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS21458.
- Predefined Register settings for several functions are available as initialization files.
 - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
 - Load the INI file DS21458_T1_BERT_ESF.ini.
 - After loading the INI file, the following may be observed:
 - o The RLOS LEDs turns green upon external loopback.
 - o All four ports of the DS21458 begin transmitting a Daly pattern. When external loopback is applied, the BERT bit count registers BBC1 to BBC3 and BEC1 to BEC3 may be updated by clearing and setting BC1.LC and clicking the 'Read All' button.

ADDRESS MAP

DK101 daughter card address space begins at 0x81000000

DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space (shown above).

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	FPGA	Board identification and clock/signal routing
0X1000 to 0X10ff	T1/E1/J1 Transceiver #1	DS21458 T1/E1/J1 transceiver, port 1
0X1100 to 0X11ff	T1/E1/J1 Transceiver #2	DS21458 T1/E1/J1 transceiver, port 2
0X1200 to 0X12ff	T1/E1/J1 Transceiver #3	DS21458 T1/E1/J1 transceiver, port 3
0X1300 to 0X13ff	T1/E1/J1 Transceiver #4	DS21458 T1/E1/J1 transceiver, port 4

Registers in the FPGA can be easily modified using the ChipView host-based user-interface software along with the definition file named "DS21458DC_FPGA.def."

FPGA REGISTER MAP

Table 2. FPGA Register Map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read Only	BOARD ID
0X0002	XBIDH	Read Only	HIGH NIBBLE EXTENDED BOARD ID
0X0003	XBIDM	Read Only	MIDDLE NIBBLE EXTENDED BOARD ID
0X0004	XBIDL	Read Only	LOW NIBBLE EXTENDED BOARD ID
0X0005	BREV	Read Only	BOARD FAB REVISION
0X0006	AREV	Read Only	BOARD ASSEMBLY REVISION
0X0007	PREV	Read Only	PLD REVISION
0X0011	MCSR	Control	DS21458 MCLK Pin Source
0X0012	TCSR	Control	DS21458 TCLK Pin Source
0X0013	SYSCCLKT	Control	DS21458 TSYSCLK Pin Setting
0X0014	SYSCCLKR	Control	DS21458 RSYSCLK Pin Setting
0X0015	SYNC1	Control	DS21458 TSYNC Source
0X0016	SYNC2	Control	DS21458 TSSYNC Source
0X0017	SYNC3	Control	DS21458 RSYNC Source
0X0018	TSERS	Control	TSER Source
0X0019	PRSER	Control	PCM RSER Source
0X001A	PSYNC	Control	PCM RSYNC/TSYNC Source
0X001B	PCLK	Control	PCM RCLK/TCLK Source

ID REGISTERS

BID: BOARD ID (Offset = 0X0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0X0007)

PREV is read only and displays the current PLD firmware revision.

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CONTROL REGISTERS

Register Name: **MCSR**

Register Description: **DS21458 MCLK Pin Source**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MSRCB	MSRCA
Default	—	—	—	—	—	—	1	1

Bit 0: DS21458 Port 1 and 3 MCLK Source (MSRCA)

0 = Connect MCLK 1 (controls port 1 and 3) to the 1.544MHz clock

1 = Connect MCLK 1 (controls port 1 and 3) to the 2.048MHz clock

Bit 1: DS21458 Port 2 and 4 MCLK Source (MSRCA)

0 = Connect MCLK 2 (controls port 2 and 4) to the 1.544MHz clock

1 = Connect MCLK 2 (controls port 2 and 4) to the 2.048MHz clock

Register Name: **TCSR**

Register Description: **DS21458 TCLK Pin Source**

Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21458 Port 1 TCLK Source (T1S0, T1S1)

The source for TCLK 1 is Defined as shown in Table 3.

Bit 2 to 3: DS21458 Port 2 TCLK Source (T2S0, T2S1)

The source for TCLK 2 is Defined as shown in Table 3.

Bit 4 to 5: DS21458 Port 3 TCLK Source (T3S0, T3S1)

The source for TCLK 3 is Defined as shown in Table 3.

Bit 6 to 7: DS21458 Port 4 TCLK Source (T4S0, T4S1)

The source for TCLK 3 is Defined as shown in Table 3.

Table 3. TCLKx Source Definition

TxS1, TxS0	TCLK CONNECTION
00	Drive TCLK _x with the 1.544MHz clock
01	Drive TCLK _x with the 2.048MHz clock
10	Drive TCLK _x with RCLK _x
11	N/A

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Register Name: **SYCLKT**

Register Description: **DS21458 TSYCLK Pin Setting**

Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	R4S1	R4S0	R3S1	R3S0	R2S1	R2S0	R1S1	R1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21458 Port 1 TSYCLK Source (R1S0, R1S1)

The source for TSYCLK 1 is Defined as shown in Table 4.

Bit 2 to 3: DS21458 Port 2 TSYCLK Source (R2S0, R2S1)

The source for TSYCLK 2 is Defined as shown in Table 4.

Bit 4 to 5: DS21458 Port 3 TSYCLK Source (R3S0, R3S1)

The source for TSYCLK 3 is Defined as shown in Table 4.

Bit 6 to 7: DS21458 Port 4 TSYCLK Source (R4S0, R4S1)

The source for TSYCLK 4 is Defined as shown in Table 4.

Table 4. TSYCLK_x Source Definition

RxS1, RxS0	TSYCLK _x CONNECTION
00	Drive TSYCLK _x with the 1.544MHz clock
01	Drive TSYCLK _x with the 2.048MHz clock
10	Drive TSYCLK _x with 8.192MHz clock
11	Drive TSYCLK _x with DS21458 Port _x BPCLK

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Register Name: **SYSCCLKR**

Register Description: **DS21458 RSYSCCLK Pin Setting**

Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21458 Port 1 RSYSCCLK Source (T1S0, T1S1)

The source for RSYSCCLK 1 is Defined as shown in Table 5.

Bit 2 to 3: DS21458 Port 2 RSYSCCLK Source (T2S0, T2S1)

The source for RSYSCCLK 2 is Defined as shown in Table 5.

Bit 4 to 5: DS21458 Port 3 RSYSCCLK Source (T3S0, T3S1)

The source for RSYSCCLK 3 is Defined as shown in Table 5.

Bit 6 to 7: DS21458 Port 4 RSYSCCLK Source (T4S0, T4S1)

The source for RSYSCCLK 4 is Defined as shown in Table 5.

Table 5. RSYSCCLKx Source Definition

TxS1, TxS0	RSYSCCLK _x CONNECTION
00	Drive RSYSCCLK _x with the 1.544MHz clock
01	Drive RSYSCCLK _x with the 2.048MHz clock
10	Drive RSYSCCLK _x with 8.192MHz clock
11	Drive RSYSCCLK _x with DS21458 Port _x BPCLK

Register Name: **TSYNC1**

Register Description: **DS21458 TSYNC Pin Source**

Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

Bit 0: DS21458 Port 1 TSYNC Source (T1SRC)

0 = TSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 1 with RSYNC 1

Bit 1: DS21458 Port 2 TSYNC Source (T2SRC)

0 = TSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 2 with RSYNC 2

Bit 2: DS21458 Port 3 TSYNC Source (T3SRC)

0 = TSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 3 with RSYNC 3

Bit 3: DS21458 Port 4 TSYNC Source (T4SRC)

0 = TSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 4 with RSYNC 4

Note: When driving TSYNC_x with RSYNC_x the corresponding DS21458 port should be configured such that TSYNC_x is an input (IOCR1.1 = 0) and RSYNC_x is an output (IOCR1.4 = 0).

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Register Name: **SYNC2**

Register Description: **DS21458 TSSYNC Pin Source**

Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

Bit 0: DS21458 Port 1 TSSYNC Source (T1SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 1 with RSYNC 1

Bit 1: DS21458 Port 2 TSSYNC Source (T2SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 2 with RSYNC 2

Bit 2: DS21458 Port 3 TSSYNC Source (T3SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 3 with RSYNC 3

Bit 3: DS21458 Port 4 TSSYNC Source (T4Source)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 4 with RSYNC 4

Note: When driving TSSYNcx with RSYNCx the corresponding DS21458 port should be configured such that RSYNCx is an output (IOCR1.4 = 0).

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Register Name: **SYNC3**

Register Description: **DS21458 RSYNC Pin Setting**

Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	RSOR1	RSOR0	—	—	R4IO	R3IO	R2IO	R1IO
Default	0	0	—	—	0	0	0	0

Bit 0: DS21458 Port 1 RSYNC Setting (R1IO)

0 = RSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 1 with RSYNC_x as shown in Table 6

Bit 1: DS21458 Port 2 RSYNC Setting (R2IO)

0 = RSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 2 with RSYNC_x as shown in Table 6

Bit 2: DS21458 Port 3 RSYNC Setting (R3IO)

0 = RSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC_x as shown in Table 6

Bit 3: DS21458 Port 4 RSYNC Setting (R4IO)

0 = RSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC_x as shown in Table 6

Note: When driving RSYNC_y with RSYNC_x the corresponding DS21458 port should be configured such that RSYNC_x is an output (IOCR1.4 = 0) and RSYNC_y is an input (IOCR1.4 = 1).

Table 6. RSYNC_x Function Definition

RSOR1, RSOR0	MASTER RSYNC DESIGNATION
00	RSYNC 1 is used to drive other RSYNC pins (providing R _x IO = 1)
01	RSYNC 2 is used to drive other RSYNC pins (providing R _x IO = 1)
10	RSYNC 3 is used to drive other RSYNC pins (providing R _x IO = 1)
11	RSYNC 4 is used to drive other RSYNC pins (providing R _x IO = 1)

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Register Name: **TSERS**

Register Description: **DS21458 TSER Pin Source**

Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21458 Port 1 TSER Source (T1S0, T1S1)

The source for TSER 1 is Defined as shown in Table 7.

Bit 2 to 3: DS21458 Port 2 TSER Source (T2S0, T2S1)

The source for TSER 2 is Defined as shown in Table 7.

Bit 4 to 5: DS21458 Port 3 TSER Source (T3S0, T3S1)

The source for TSER 3 is Defined as shown in Table 7.

Bit 6 to 7: DS21458 Port 4 TSER Source (T4S0, T4S1)

The source for TSER 4 is Defined as shown in Table 7.

Table 7. TSERx Source Definition

TxS1, TxS0	TSER _x CONNECTION
00	Tri-state TSER _x (weak pulldown)
01	Drive TSER _x with RSER _x
10	Drive TSER _x with PCM_TXD bus (DK2000 only)
11	N/A

Register Name: **PRSER**

Register Description: **PCM RSER Source**

Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	R1EN	R1EN	R1EN	R1EN
Default	—	—	—	—	0	0	0	0

Bit 0 to 1: PCM RSER Source (R1EN)

0 = Do not drive DS21458 Port 1 RSER onto PCM_RSER

1 = Logically OR DS21458 Port 1 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 2 to 3: DS21458 Port 2 TSER Source (T2S0, T2S1)

0 = Do not drive DS21458 Port 2 RSER onto PCM_RSER

1 = Logically OR DS21458 Port 2 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 4 to 5: DS21458 Port 3 TSER Source (T3S0, T3S1)

0 = Do not drive DS21458 Port 3 RSER onto PCM_RSER

1 = Logically OR DS21458 Port 3 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 6 to 7: DS21458 Port 4 TSER Source (T4S0, T4S1)

0 = Do not drive DS21458 Port 4 RSER onto PCM_RSER

1 = Logically OR DS21458 Port 4 RSER with selected other RSER pins and drive onto PCM_RSER

Note: PRSER register is for use with the DK2000 only.

DS21458DK, Quad T1/E1/J1 Transceiver Design Kit Daughter Card

Register Name: **PSYNC**

Register Description: **PCM RSYNC/TSYNC Source**

Register Offset: **0x001A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	T2SR	T1SR	—	—	R2SR	R1SR
Default	—	—	0	0	—	—	0	0

Bit 0 to 1: PCM_RSYNC Source

R2SR, R1SR	PCM_RSYNC SOURCE
00	PCM_RSYNC is driven by DS21458 port 1 RSYNC
01	PCM_RSYNC is driven by DS21458 port 2 RSYNC
10	PCM_RSYNC is driven by DS21458 port 3 RSYNC
11	PCM_RSYNC is driven by DS21458 port 4 RSYNC

Bit 4 to 5: PCM_TSYNC Source

T2SR, T1SR	PCM_TSYNC SOURCE
00	PCM_TSYNC is driven by DS21458 port 1 TSYNC
01	PCM_TSYNC is driven by DS21458 port 2 TSYNC
10	PCM_TSYNC is driven by DS21458 port 3 TSYNC
11	PCM_TSYNC is driven by DS21458 port 4 TSYNC

Note: PSYNC register is for use with the DK2000 only.

DS21458DK, Quad T1/E1/J1 Transceiver Design Kit Daughter Card

Register Name: **PCLK**

Register Description: **PCM RCLK/TCLK Source**

Register Offset: **0x001B**

Bit #	7	6	5	4	3	2	1	0
Name	—	TCM	T2SR	T1SR	—	RCM	R2SR	R1SR
Default	—	0	0	0	—	0	0	0

Bit 0 to 2: PCM_RCLK Source

RCM,R2SR, R1SR	PCM_RCLK SOURCE
000	PCM_RCLK is driven by DS21458 port 1 RCLK
001	PCM_RCLK is driven by DS21458 port 2 RCLK
010	PCM_RCLK is driven by DS21458 port 3 RCLK
011	PCM_RCLK is driven by DS21458 port 4 RCLK
100	PCM_RCLK is driven by DS21458 port 1 BPCLK
101	PCM_RCLK is driven by DS21458 port 2 BPCLK
110	PCM_RCLK is driven by DS21458 port 3 BPCLK
111	PCM_RCLK is driven by DS21458 port 4 BPCLK

Bit 4 to 5: PCM_TCLK Source

TCM,T2SR, T1SR	PCM_TCLK SOURCE
000	PCM_TCLK is driven by source used for DS21458 port 1 TCLK
001	PCM_TCLK is driven by source used for DS21458 port 2 TCLK
010	PCM_TCLK is driven by source used for DS21458 port 3 TCLK
011	PCM_TCLK is driven by source used for DS21458 port 4 TCLK
100	PCM_TCLK is driven by DS21458 port 1 BPCLK
101	PCM_TCLK is driven by DS21458 port 2 BPCLK
110	PCM_TCLK is driven by DS21458 port 3 BPCLK
111	PCM_TCLK is driven by DS21458 port 4 BPCLK

Note: PCLK register is for use with the DK2000 only.

FPGA CONTROL EXAMPLES

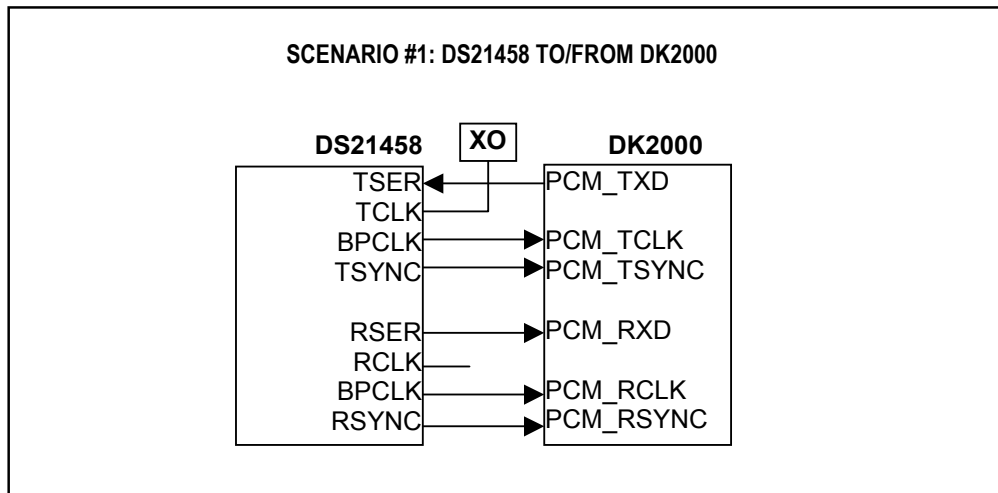


Table 8. FPGA Configuration for Scenario #1 (Port 1, T1 Mode)

REGISTER	SETTING	COMMENT
MCSR	0X01	Drive DS21458 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X00	Drive TCLK with 1.544MHz
SYSCLKT	0X00	Drive TSYSCLK with 1.544MHz
SYSCLKR	0X00	Drive RSYSCLK with 1.544MHz
SYNC1	0X00	Tri-state FPGA driver pin for DS21458 TSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21458 RSYNC
TSERS	0X02	Drive DS21458 TSER1 with data from PCM bus
PRSER	0X01	Drive DS21458 RSER1 onto PCM bus
PSYNC	0X00	PCM RSYNC and PCM TSYNC are provided by DS21458 port 1 RSYNC and TSYNC (respectively)
PCLK	0X44	PCM RCLK and TCLK are driven by port 1 BPCLK

FPGA CONTROL EXAMPLES (continued)

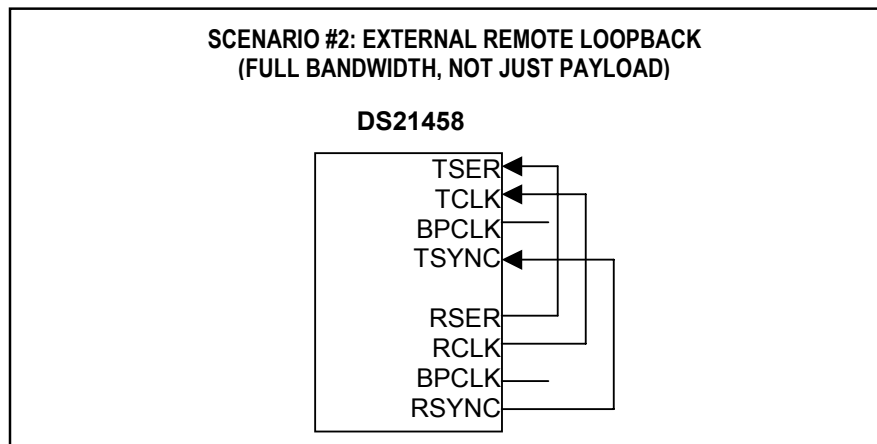


Table 9. FPGA Configuration for Scenario #2 (Port 1, T1 Mode)

REGISTER	SETTING	COMMENT
MCSR	0X01	Drive DS21458 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X02	Drive TCLK1 with RCLK1
SYSCLKT	0X00	Drive TSYSClk with 1.544MHz
SYSCLKR	0X00	Drive RSYSClk with 1.544MHz
SYNC1	0X01	Drive TSYNC1 with RSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21458 RSYNC
TSERS	0X01	Drive DS21458 TSER1 with data from RSER1
PRSER	N/A	Unused
PSYNC	N/A	Unused
PCLK	N/A	Unused

Table 10. DS21458 Partial Configuration for Scenario #2 (Port 1, T1 Mode)

REGISTER	SETTING	COMMENT
IOCR1	TSIO = 0; RSIO = 0	TSYNC is an input, RSYNC is an output
ESCR	TESE = 0; RESE = 0	Bypass Rx and Tx elastic stores
CCR1	TCSS1 = 0; TCSS2 = 0	TCLK is driven by TCLK pin

DS21458DK, Quad T1/E1/J1 Transceiver Design Kit Daughter Card

DS21458 INFORMATION

For more information about the DS21458, please consult the DS21458 data sheet available on our website at www.maxim-ic.com/DS21458. Software downloads are also available for this design kit.

DS21458DK INFORMATION

For more information about the DS21458DK, including software downloads, please consult the DS21458DK data sheet available on our website at www.maxim-ic.com/DS21458DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS21458DK schematics are featured at the end of this document.

DS21458 DESIGN KIT

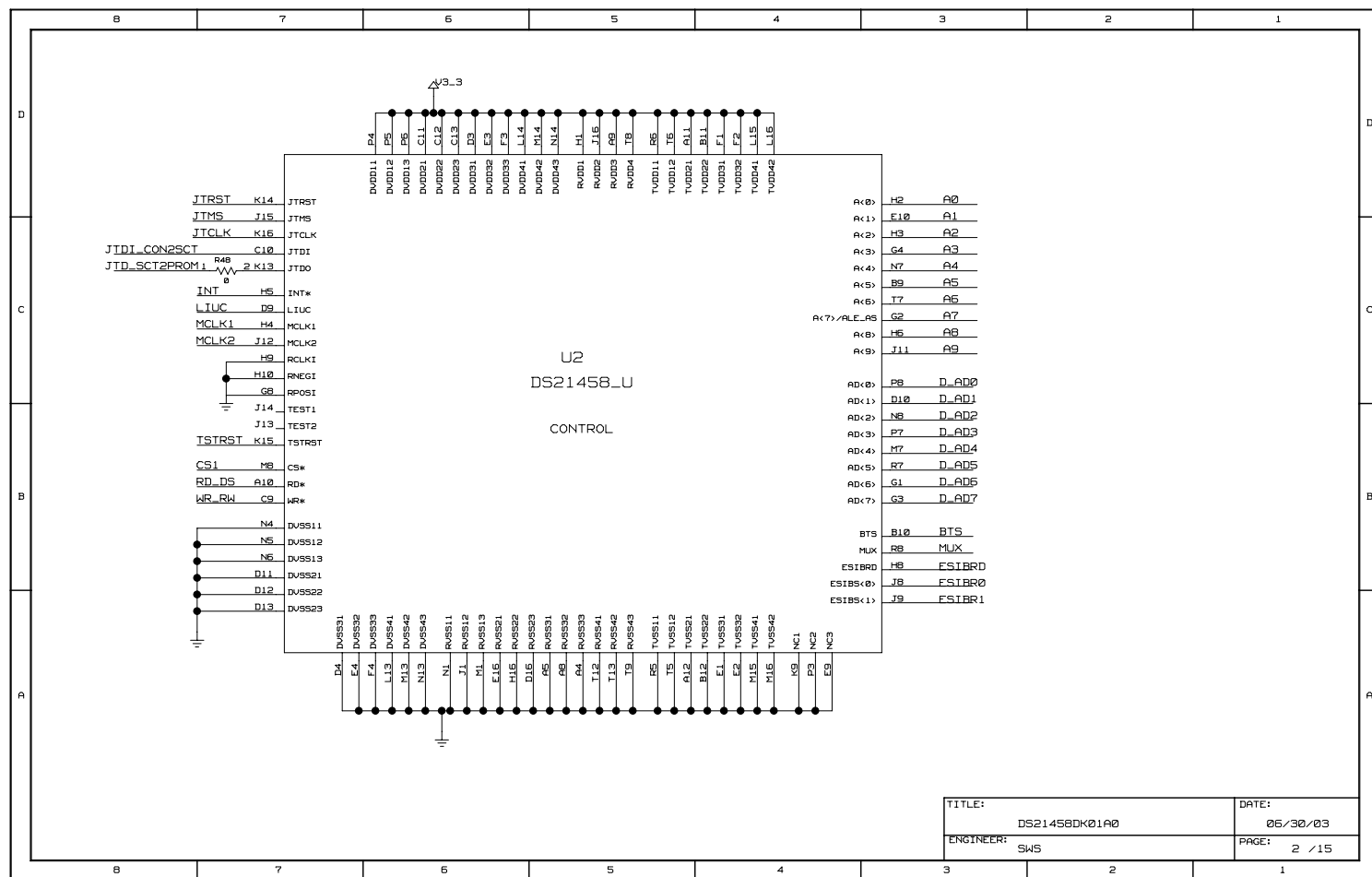
REVISIONS: (MODIFICATION FROM DS21055 BOARD)

CONTENTS

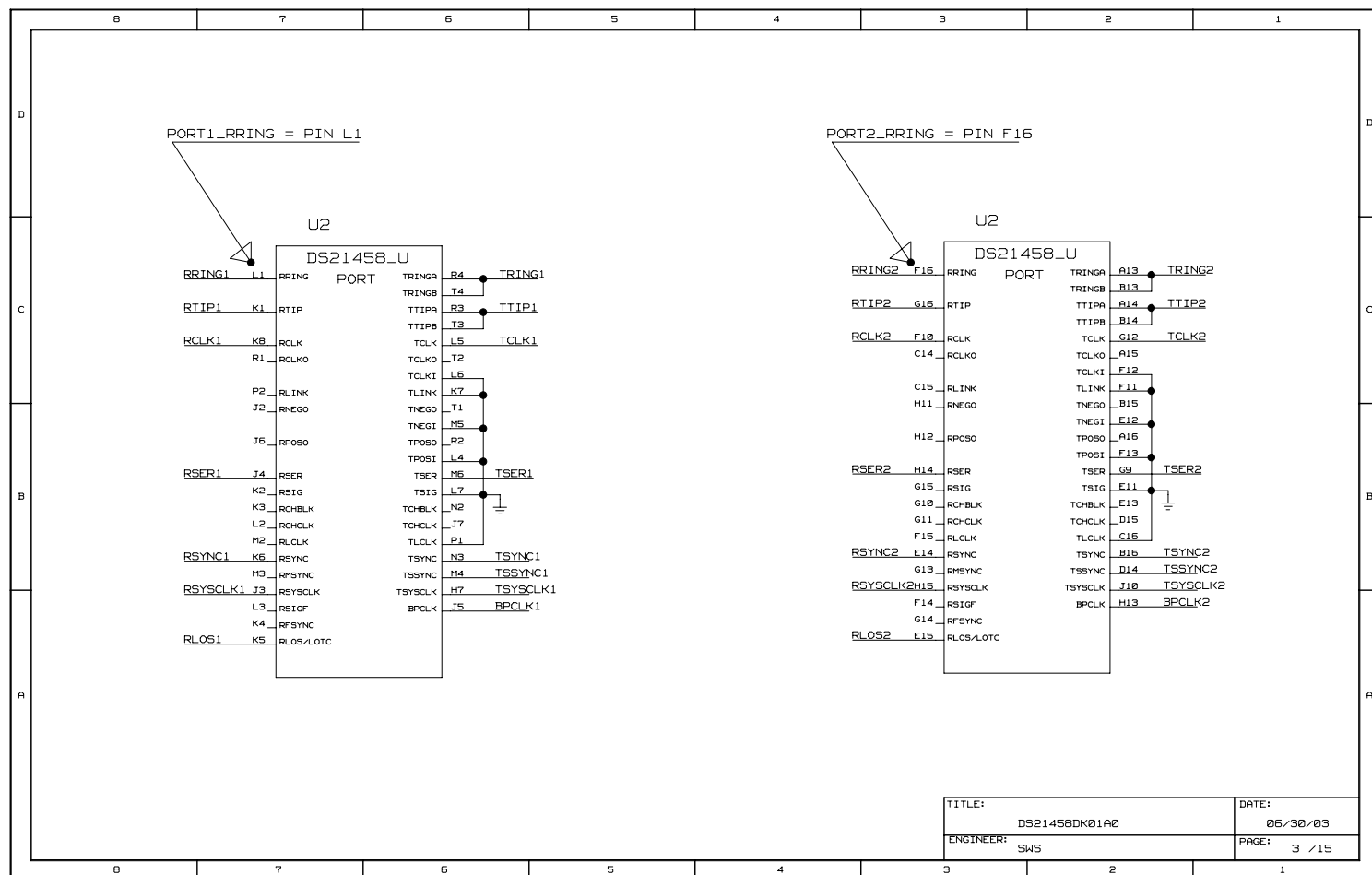
1. COVER PAGE
2. DS21458 CONTROL AND BACKPLANE
3. PORT 1 AND 2 TX / RX SYSTEM SIDE
4. PORT 3 AND 4 TX / RX SYSTEM SIDE
5. PORT 1 TX / RX ANALOG PATHS
6. PORT 2 TX / RX ANALOG PATHS
7. PORT 3 TX / RX ANALOG PATHS
8. PORT 4 TX / RX ANALOG PATHS
9. DAUGHTER CARD ADDRESS DATA BUS CONNECTION
10. FPGA CROSS CONNECT FOR RX / TX SIGNALS
11. FPGA AND CONFIG PROM CONTROL
12. FPGA CLOCK AND DATABUS
13. SUPPLY DECOUPLING
14. SIGNAL CROSS-REFERENCE
15. COMPONENT CROSS-REFERENCE

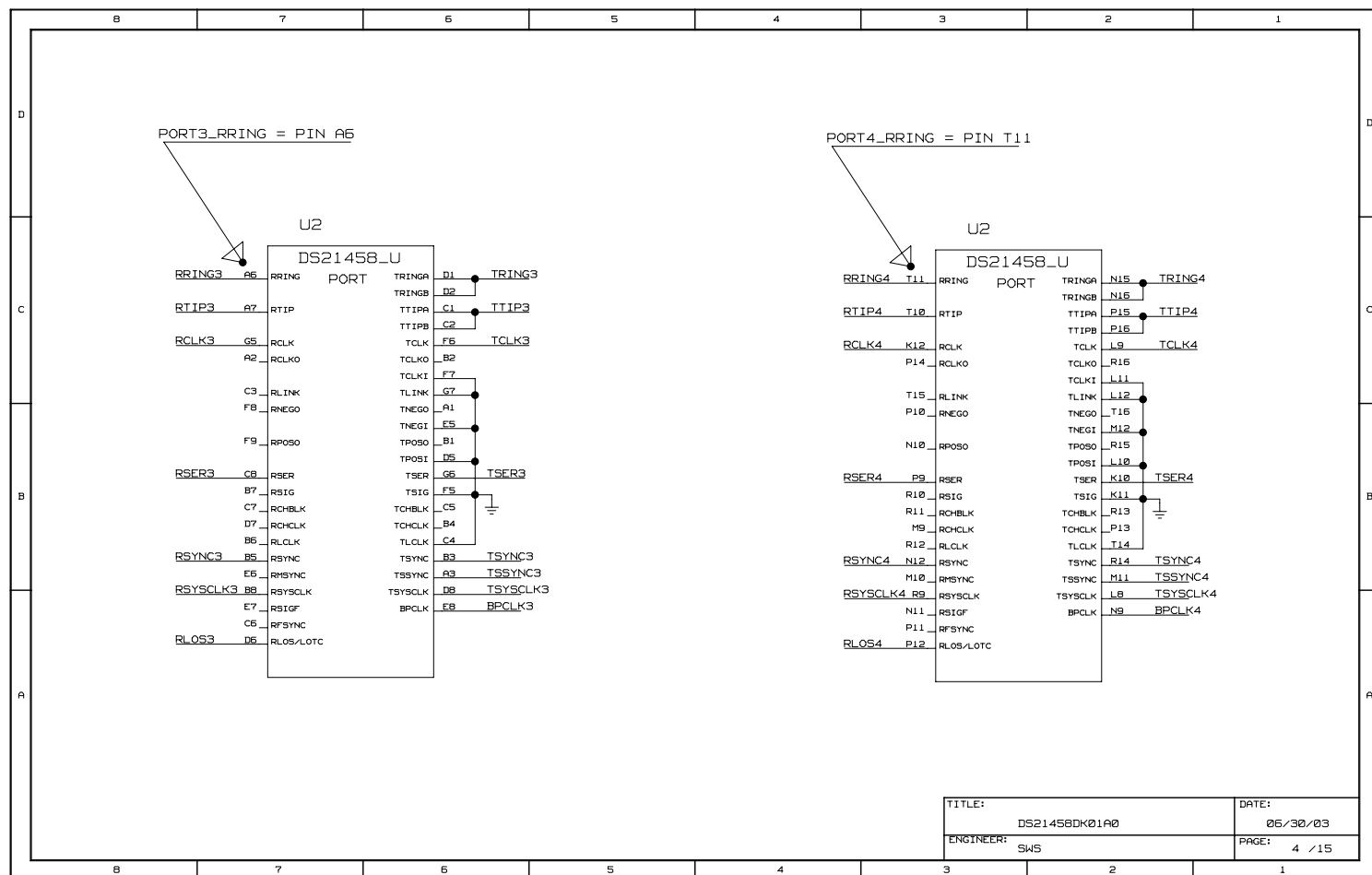
1. ESIBRD CONNECTIONS CHANGE FROM 4X TO 1X (ONLY PULLDOWNS REMAIN)
2. ADDED AB AND A9 TO DS21458 AND FPGA, REMOVED CS2-4
3. REMOVED RLOS FPGA CONNECTION, RLOS LED IS NOW DRIVEN BY THE SCT
4. REMOVED SERIAL CONFIG PROM, REPLACED WITH XILINK FLASH BASED CONFIG PROM
5. RAN PIN SWAP ON XILINK PART TO ACCOMMODATE PIN DIFFERENCES BETWEEN DS21458 AND DS21055
6. REMOVED TEST POINTS IN JTAG CHAIN
7. REMOVED CONNECTION BETWEEN 2.5V SUPPLY MONITOR AND FPGA INIT PIN
8. REMOVED CONNECTION BETWEEN CPU RESET AND FPGA PROGRAM PIN
-FPGA RESET IS NOW DRIVEN BY INTERNAL STATE MACHINE
9. CHANGED SWITCH NAMES FOR PORT 1-4 FROM SW PREFIX TO PRT PREFIX
10. ADDED T1 E1 DESIGNATION TO SWITCHES FOR PORT 1-4
11. CHANGED SILKSCREEN ON JTAG CONNECTOR

TITLE:	DS21458DK01A0	DATE:	05/30/03
ENGINEER:	SWS	PAGE:	1 / 15

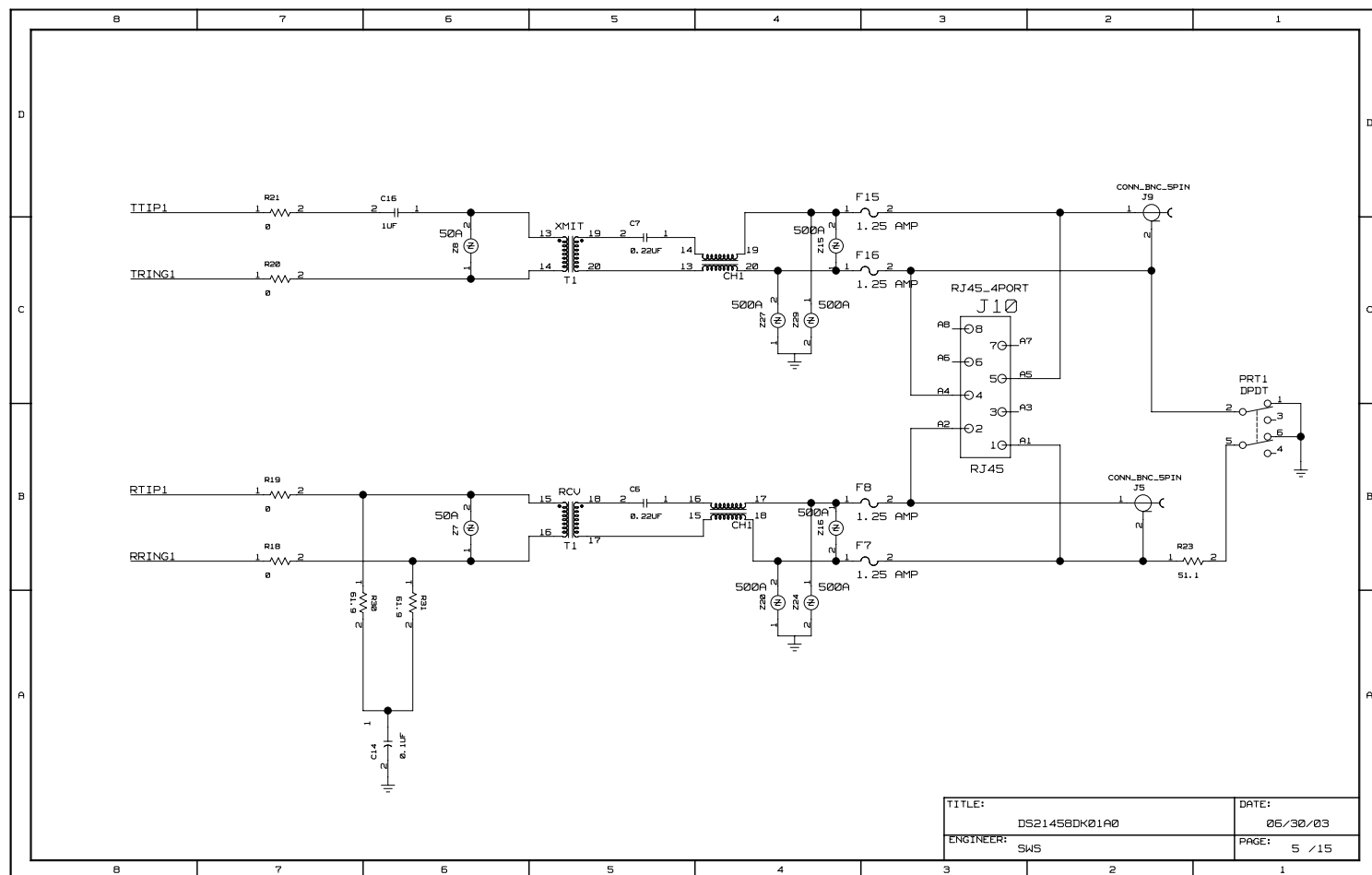


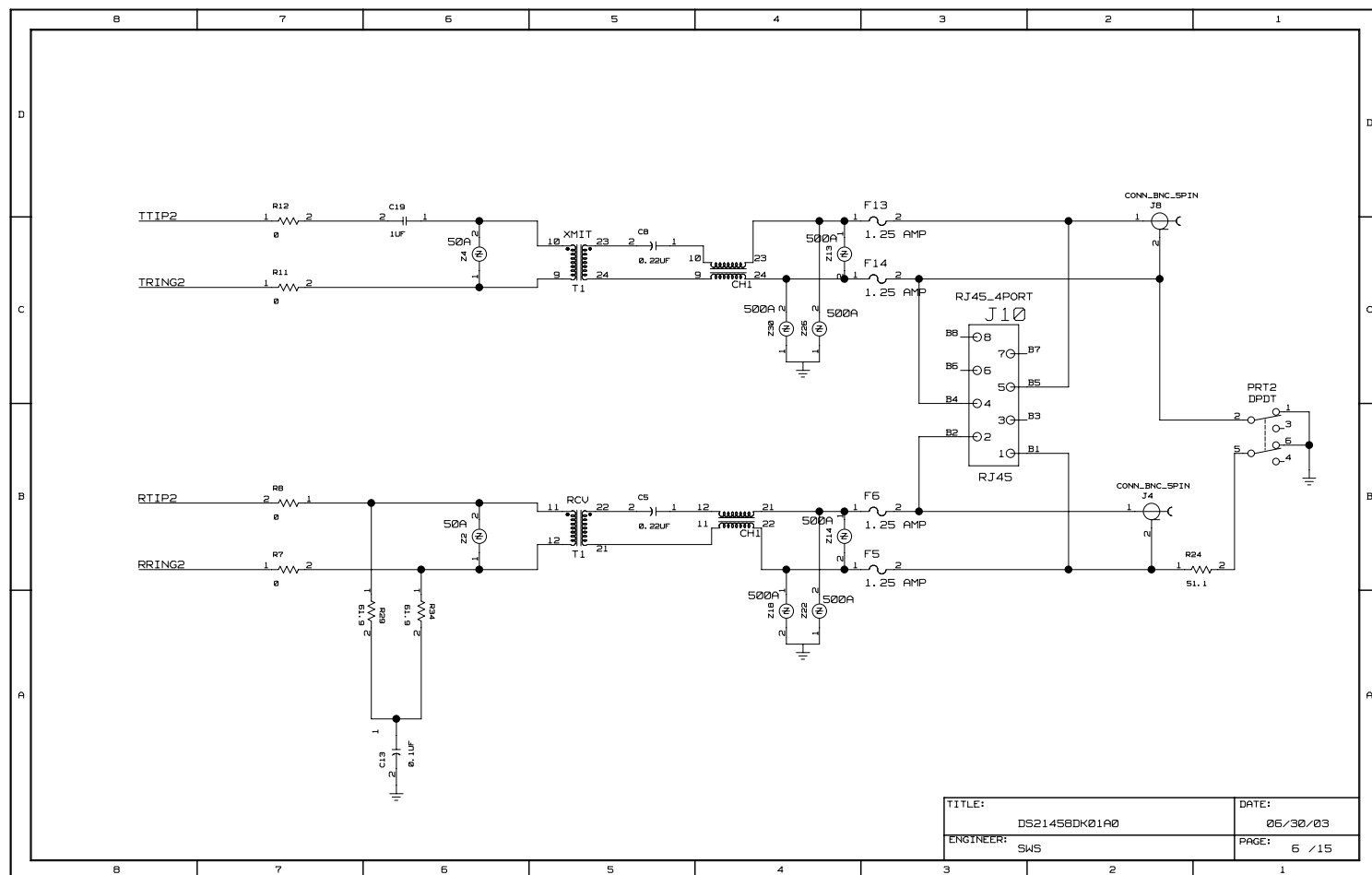
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ENGINEER:	SWS	PAGE:	2 / 15



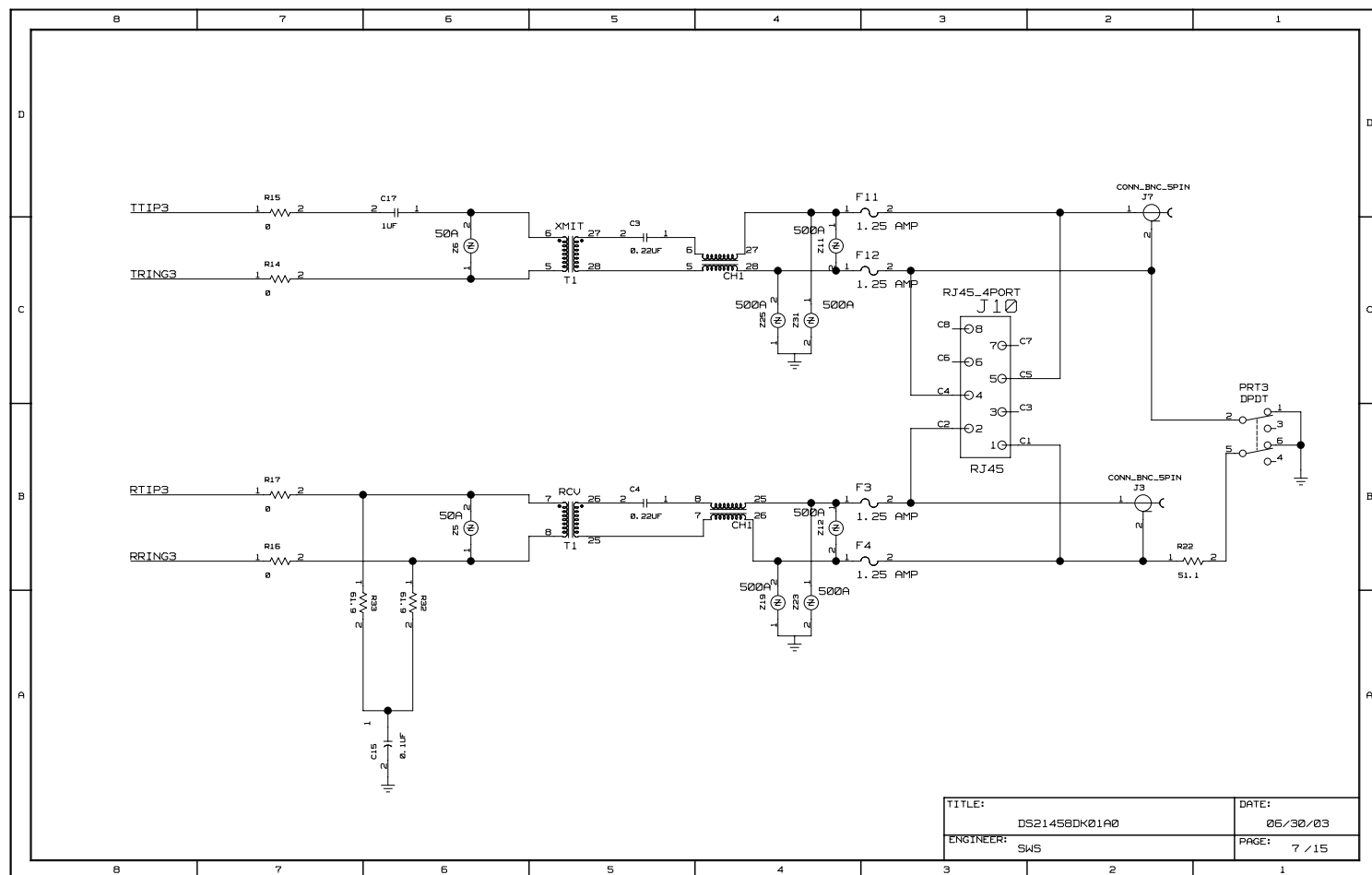


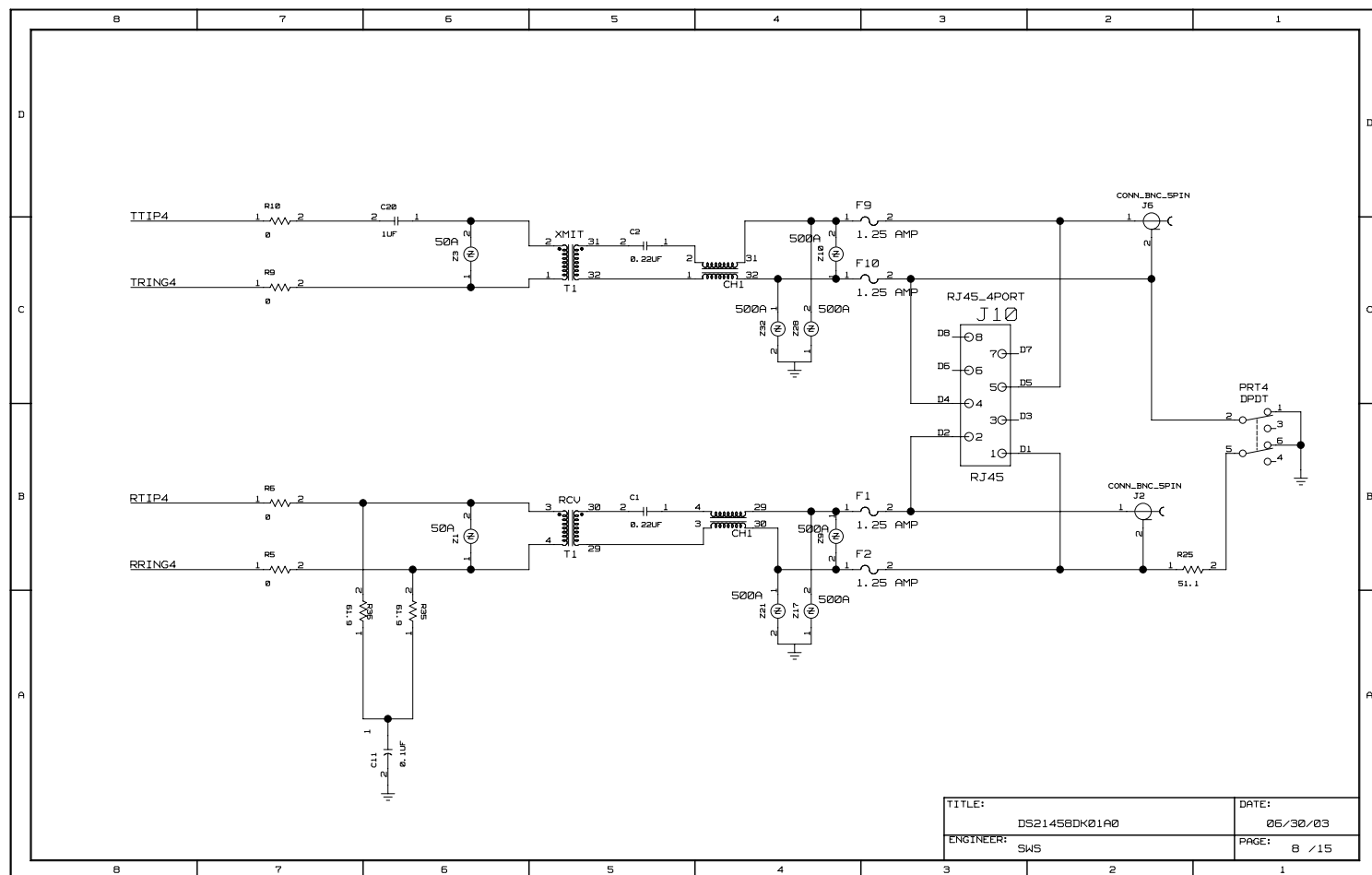
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ENGINEER:	SWS	PAGE:	4 / 15

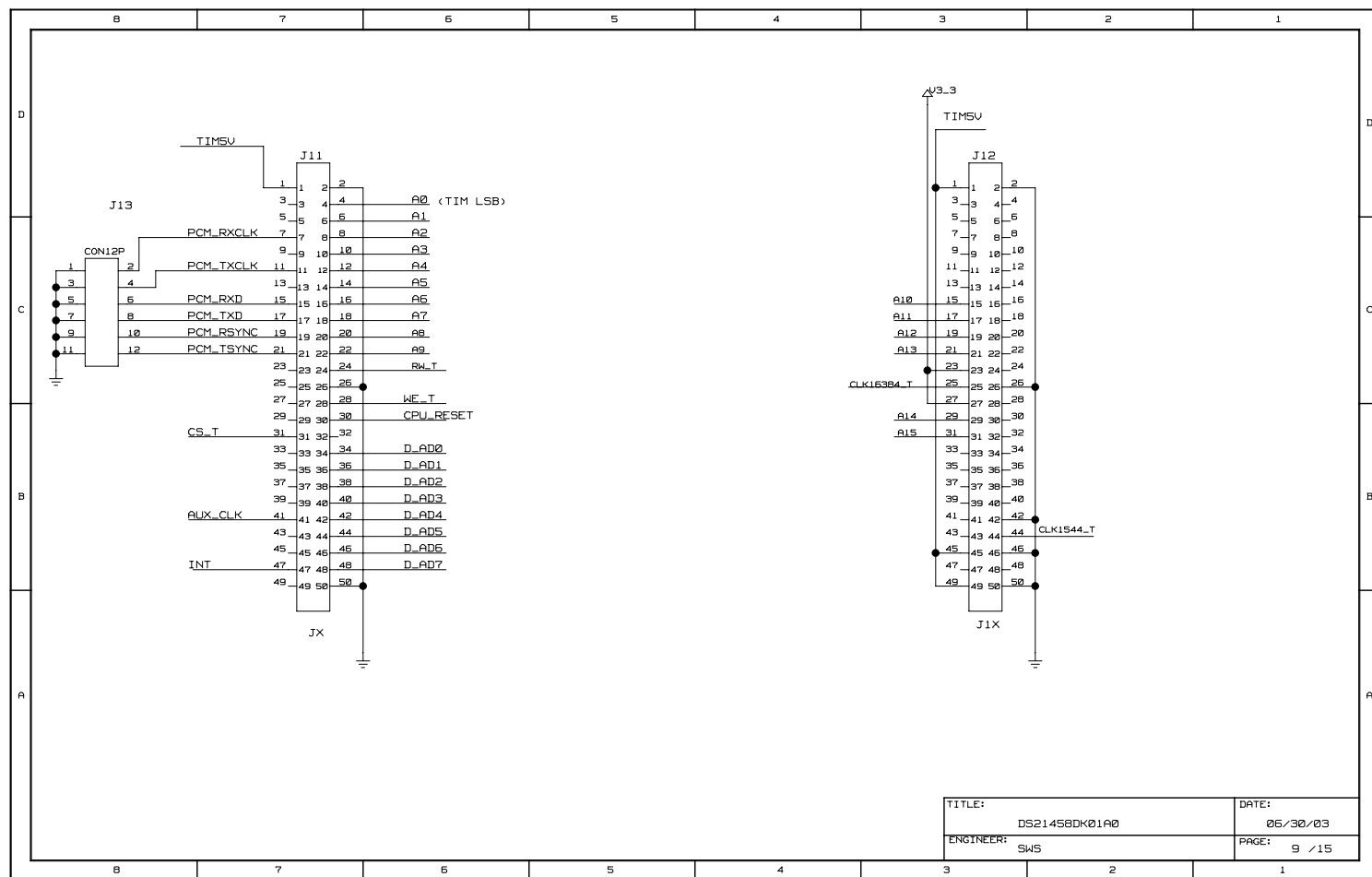


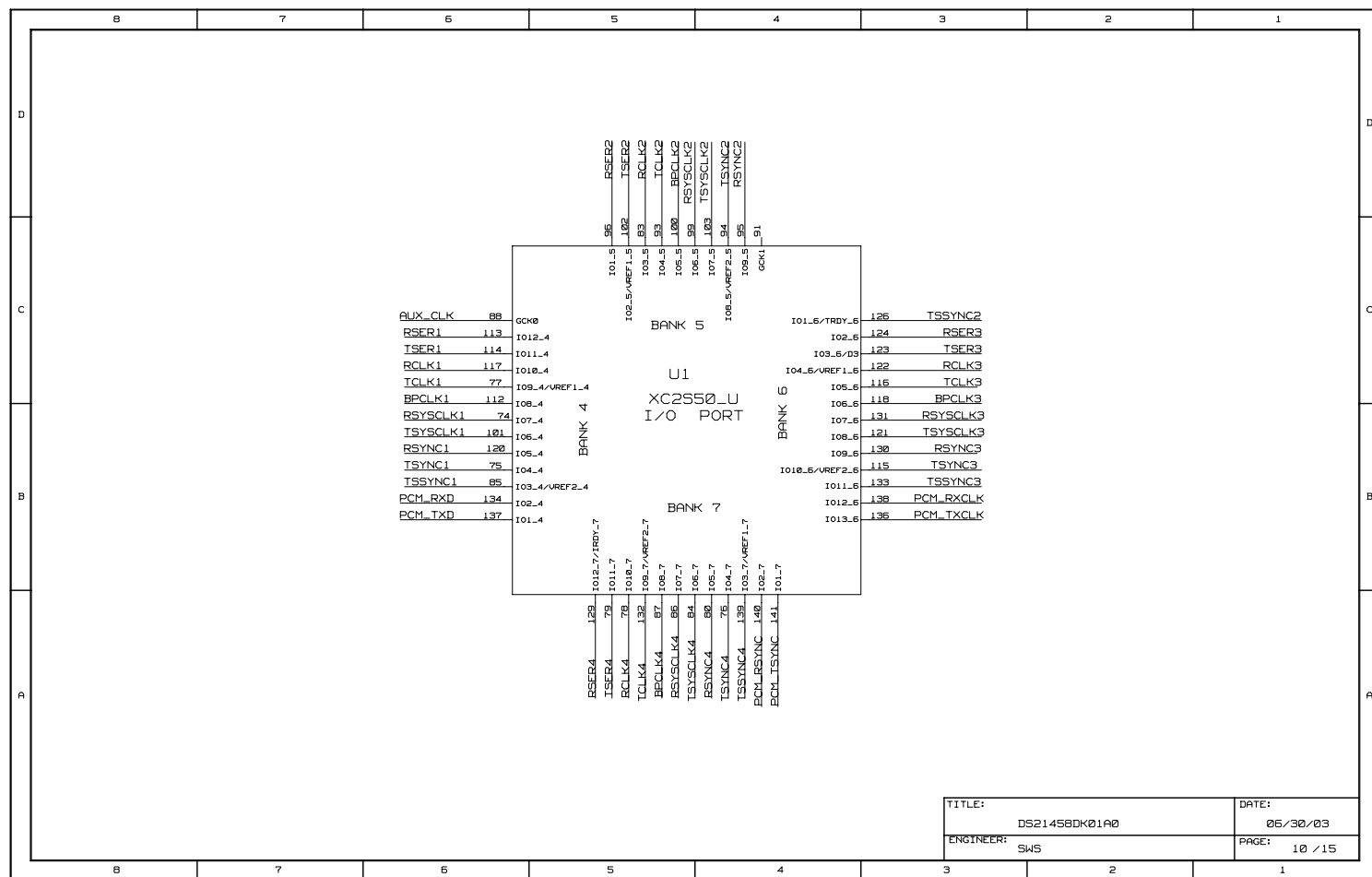


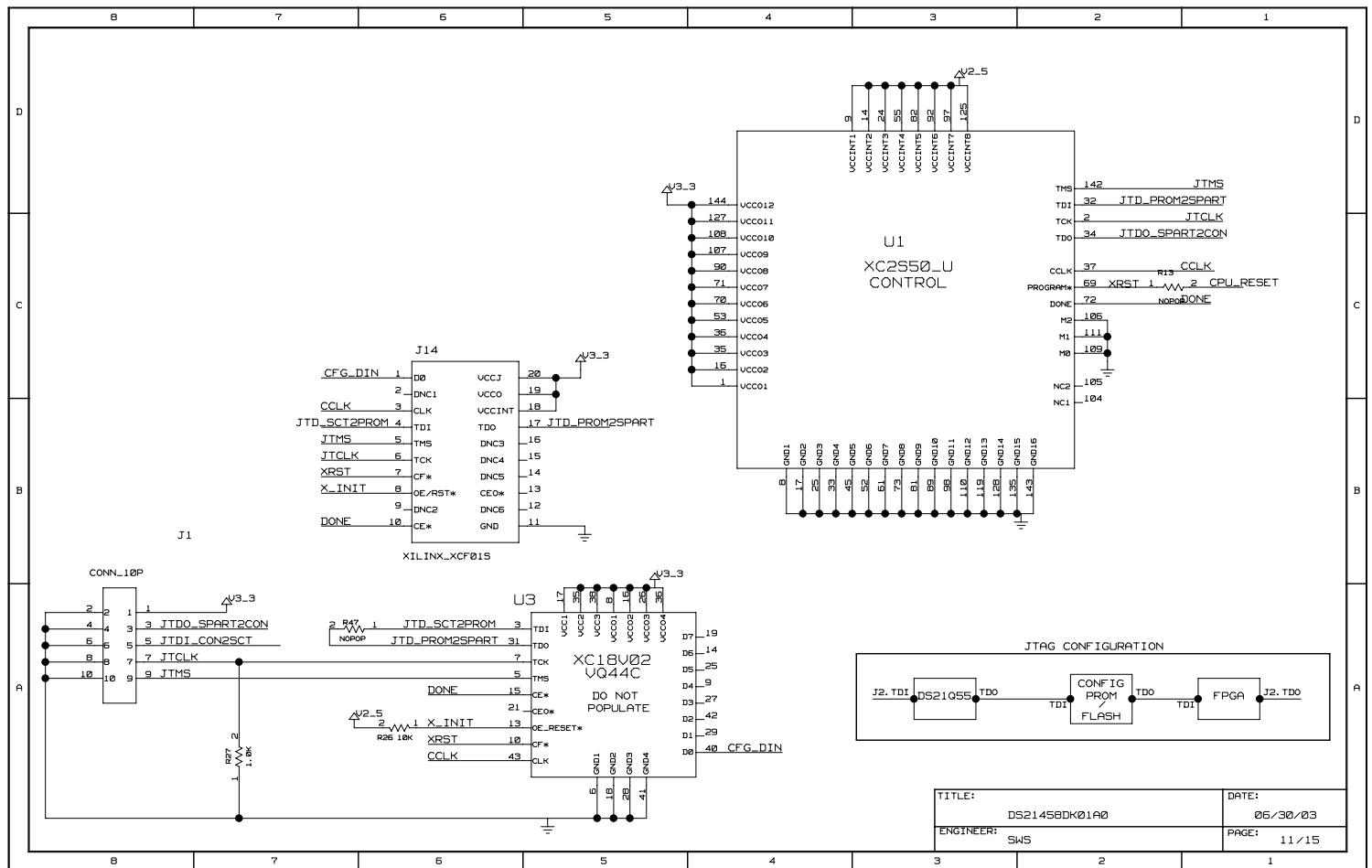
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ENGINEER:	SWS	PAGE:	6 / 15



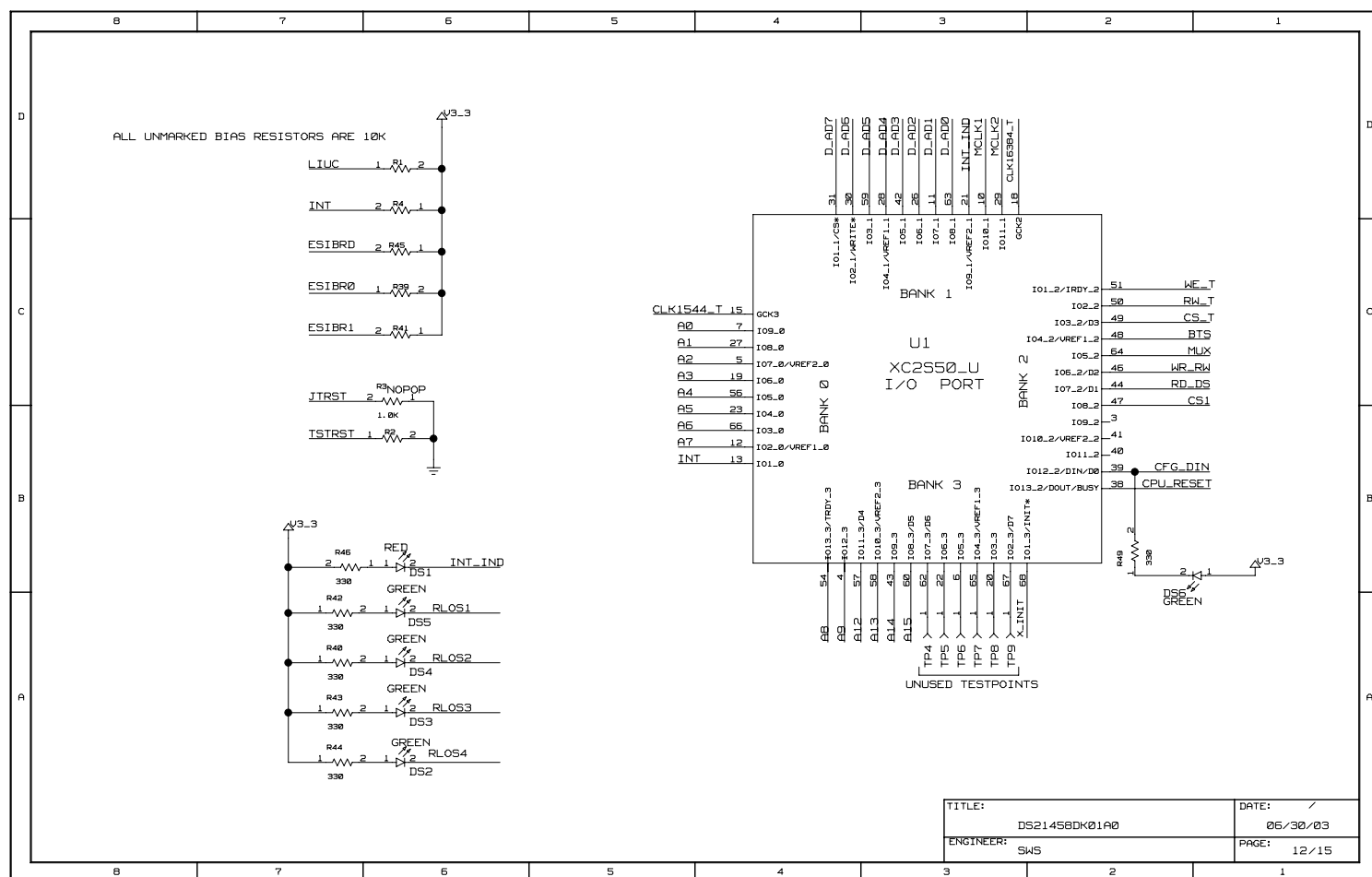


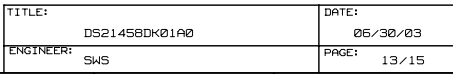






TITLE:	DS21458DK01A0	DATE:	05/30/03
ENGINEER:	SWS	PAGE:	11/15





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D	*** Signal Cross-Reference for the entire design ***							
	A0	906<> 1205<> 203<	ASER3	48B<> 18C3<>				
	A1	906<> 1205<> 203<	ASER4	48A<> 18A5<>				
	A2	906<> 1205<> 203<	RSYNC1	38B<> 18B5<>				
	A3	906<> 1205<> 203<	RSYNC2	38A<> 18A4<>				
	A4	906<> 1205<> 203<	RSYNC3	48B<> 18B3<>				
	A5	906<> 1205<> 203<	RSYNC4	48A<> 18A4<>				
	A6	906<> 1205<> 203<	RSYCLK1	18B5<> 38B<				
	A7	906<> 1205<> 203<	RSYCLK2	18D5<> 38A<				
	A8	906<> 1205<> 203<	RSYCLK3	18B3<> 48B<				
C	A9	906<> 1204<> 203<	RSYCLK4	18A5<> 48A<				
	A10	906<> 1204<> 203<	RTIP1	3C3<> 5B5<				
	A11	906<> 1204<> 203<	RTIP2	3C4<> 6B8<				
	A12	906<> 1204<> 203<	RTIP3	4C8<> 7B8<				
	A13	906<> 1204<> 203<	RTIP4	4C4<> 6B8<				
	A14	906<> 1204<> 203<	RA_L_T	9C8<> 12C1<>				
	A15	906<> 1204<> 203<	TCLK1	18C8<> 3C3<				
	APCLK1	906<> 1205<> 203<	TCLK2	18D5<> 3C1<				
	BPCLK2	3A1<> 18D5<>	TCLK3	18C3<> 4C5<				
	BPCLK3	4A8<> 18B3<>	TCLK4	18B5<> 4C1<				
B	BPCLK4	4A1<> 18B5<>	TRING1	5C3<> 5C3<				
	BT5	12C1<> 2B3<	TRING2	3C1<> 6C8<				
	CLK	11B7<> 11A6< 11C1<	TRING3	4C3<> 7C3<				
	CLK1544_T	906<> 1205<	TRING4	4C1<> 6C8<				
	CLK16384_T	906<> 1203<	TSER1	18C8<> 3B5<				
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	C2	OP	825	J8	CONN_BNC_SPIN 602	Z5	SIDACTOR_2 7B5	
	C3	OP	7C3	J9	CONN_BNC_SPIN 502	Z6	SIDACTOR_2 7C5	
	C4	OP	7B5	J10	R145_9 5C3 6C3 7C3 8C3	Z7	SIDACTOR_2 5B5	
	C5	OP	6B5	J11	CONN_SBP2 507	Z8	SIDACTOR_2 5C5	
	C6	OP	5B5	J12	CONN_SBP2 503	Z9	SIDACTOR_2 8B4	
	C7	OP	5C5	J13	CONN_2P 502	Z10	SIDACTOR_2 8C4	
	C8	OP	6C5	J14	X11NK_XCF815 11C5	Z11	SIDACTOR_2 7C4	
	C9	OP	13B7	PR1	SWITCH_DPOT_SLIDE_5P 5C1	Z12	SIDACTOR_2 7B4	
C	C10	OP	13B5	PR2	SWITCH_DPOT_SLIDE_5P 5C1	Z13	SIDACTOR_2 6C4	
	C11	OP	8A6	PR3	SWITCH_DPOT_SLIDE_5P 7C1	Z14	SIDACTOR_2 6B4	
	C12	OP	13B4	PR4	SWITCH_DPOT_SLIDE_5P 8C1	Z15	SIDACTOR_2 5C4	
	C13	OP	6A6	R1	RES1 1205	Z16	SIDACTOR_2 5B4	
	C14	OP	5A6	R2	RES1 1206	Z17	SIDACTOR_2 5A4	
	C15	OP	7A6	R3	RES 12C5	Z18	SIDACTOR_2 6A4	
	C16	OP	5D6	R4	RES1 1205	Z19	SIDACTOR_2 6A4	
	C17	OP	7D6	R5	RES 8B7	Z20	SIDACTOR_2 5A4	
	C18	OP	13B7	R6	RES 8B7	Z21	SIDACTOR_2 6A4	
	C19	OP	6C6	R7	RES 8B7	Z22	SIDACTOR_2 6A4	
B	C20	OP	8C6	R8	RES 8B7	Z23	SIDACTOR_2 7A4	
	C21	OP	13C4	R9	RES 8C7	Z24	SIDACTOR_2 5A4	
	C22	OP	13B5	R10	RES 8D7	Z25	SIDACTOR_2 7C4	
	C23	OP	13B2	R11	RES 6C7	Z26	SIDACTOR_2 5C4	
	C24	OP	13B2	R12	RES 6D7	Z27	SIDACTOR_2 5C4	
	C25	OP	13B6	R13	RES1 11C2	Z28	SIDACTOR_2 6C4	
	C26	OP	13B1	R14	RES 7C7	Z29	SIDACTOR_2 5C4	
	C27	OP	13B4	R15	RES 7D7	Z30	SIDACTOR_2 6C4	
	C28	OP	13B2	R16	RES 7B7	Z31	SIDACTOR_2 7C4	
	C29	OP	13B3	R17	RES 7B7	Z32	SIDACTOR_2 6C4	
A	C30	OP	13B5	R18	RES 5B7			
	C31	OP	13B7	R19	RES 5B7			
	C32	OP	13B3	R20	RES 5C7			
	C33	OP	13B2	R21	RES 5D7			
	C34	OP	13D3	R22	RES 7B2			
	C35	OP	13B1	R23	RES 5B2			
	C36	OP	13D2	R24	RES 6B2			
	C37	OP	13D3	R25	RES 6B2			
	C38	OP	13B3	R26	RES 11A6			
	C39	OP	13B4	R27	RES1 11A7			
	C40	OP	13B6	R28	RES1 6A6			
	C41	OP	13B2	R29	RES1 5A6			
	C42	OP	13B2	R30	RES1 5A6			
	C43	OP	13B0	R31	RES1 5A6			
	C44	OP	13B0	R32	RES1 7A6			
	C45	OP	13B0	R33	RES1 7A6			
	CH1	CHOKE_QUADPORT_T1	5B4 5C4 6B4 6C4 7B4 7C4 8B4	R34	RES1 6A6			
	D51	LED	12B5	R35	RES1 6A6			
	D52	LED	12A6	R36	RES1 6A6			
	D53	LED	12A6	R37	RES 12C5			
	D54	LED	12A6	R41	RES 12C5			
	D55	LED	12B6	R42	RES1 12A7			
	D56	LED	12B2	R43	RES1 12A7			
	F1	FUSE	8B4	R44	RES1 12A7			
	F2	FUSE	8B4	R45	RES 12C5			
	F3	FUSE	7B4	R46	RES1 12B7			
	F4	FUSE	7B4	R47	RES1 11A7			
	F5	FUSE	6B3	R48	RES 2C7			
	F6	FUSE	6B3	R49	RES1 12B2			
	F7	FUSE	5B4	T1	XFMR_QUADPORT_T1	5B5 5C5 6B5 6C5 7B5 7C5 8B5		
	F8	FUSE	5B4					
	F9	FUSE	8D4	TP1	TSTPNT_SNG 13B3			
	F10	FUSE	8C4	TP4	TESTPOINT 12A3			
	F11	FUSE	7D4	TP5	TESTPOINT 12A3			
	F12	FUSE	7C4	TP6	TESTPOINT 12A3			
	F13	FUSE	6D3	TP7	TESTPOINT 12A3			
	F14	FUSE	6C3	TP8	TESTPOINT 12A3			
	F15	FUSE	5D4	TP9	TESTPOINT 12A3			
	F16	FUSE	5C4	TP24	TSTPNT_SNG 13B4			
	J1	CONN_10P	11B9	TP25	TSTPNT_SNG 13B4			
	J2	CONN_BNC_SPIN	8B2	TP26	TSTPNT_SNG 13B4			
	J3	CONN_BNC_SPIN	7B2	U1	XC25585U 10C5 11C3 12C3			
	J4	CONN_BNC_SPIN	6B2	U2	DS9145E-U 6C5 5C3 3C7 4C3 4C7			
	J5	CONN_BNC_SPIN	5B2	U3	XC18A02V044C-U 11A6			
	J6	CONN_BNC_SPIN	6B2	U4	MAX1752 13D4			
				Z1	SIDACTOR_2 6B6			
				Z2	SIDACTOR_2 6B6			
				Z3	SIDACTOR_2 6C5			
B		7	6	5	4	3	2	1
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