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[DLPD3V3LC-7](#)

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NOT RECOMMENDED FOR NEW DESIGNS

DLPD3V3LC



3.3V LOW CAPACITANCE BIDIRECTIONAL TVS

Features

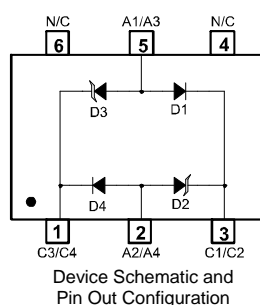
- 330 Watts Peak Pulse Power ($t_p = 8 \times 20 \mu s$)
- Transient Protection for data, signal, and V_{CC} bus to IEC61000-4-2 level 4 (ESD)
- Low Capacitance, typ. $< 3 \text{ pF}$
- Bidirectional Configuration
- Surface Mount Package Ideally Suited for Automated Insertion
- **Lead Free By Design/RoHS Compliant (Note 3)**
- **"Green" Device (Note 4)**

Mechanical Data

- Case: SOT-26
- Case Material: Molded Plastic, "Green" Molding Compound, Note 4. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 2
- Ordering Information: See Page 2
- Weight: 0.017 grams (approximate)



Top View



Maximum Ratings, Total Device @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Peak Pulse Power (Note 2)	P_{pk}	330	W

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	286	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Reverse Standoff Voltage	Breakdown Voltage V_{BR} @ I_T		Test Current I_T (mA)	Max. Reverse Leakage @ V_{RWM} (Note 7) I_R (mA)	Max. Clamping Voltage @ $I_p = 1 \text{ A}$ (Note 2) V_C (V)	Max. Clamping Voltage V_C @ I_{PP} (Note 2) (V)	Max. Peak Pulse Current (Note 2) I_{PP} (A)	Typical Total Capacitance (Note 1) (pF)
	Min (V)	Max (V)						
V_{RWM} (V)	4.0	—	1.0	0.11	8.0	22	15	2.5

- Notes:
1. $V_R = 0\text{V}$, $f = 1\text{MHz}$ as measured between pins 1 and 3.
 2. $t_p = 8 \times 20 \mu s$. See figure 2.
 3. No purposefully added lead.
 4. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
 5. Device mounted on FR-4 PCB with pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.
 6. From pin 3 to pin 1, and/or from pin 1 to pin 3.
 7. Short duration pulse test used to minimize self-heating effect.



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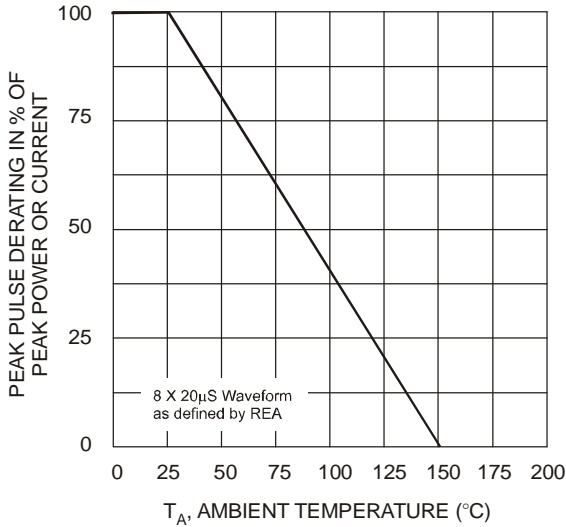


Fig. 1 Pulse Derating Curve

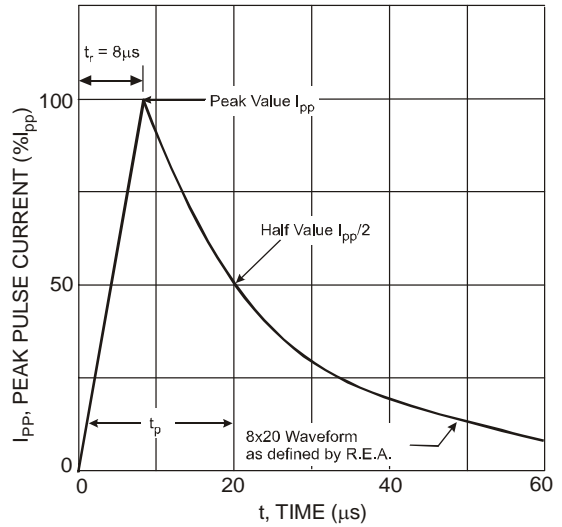


Fig. 2 Pulse Waveform

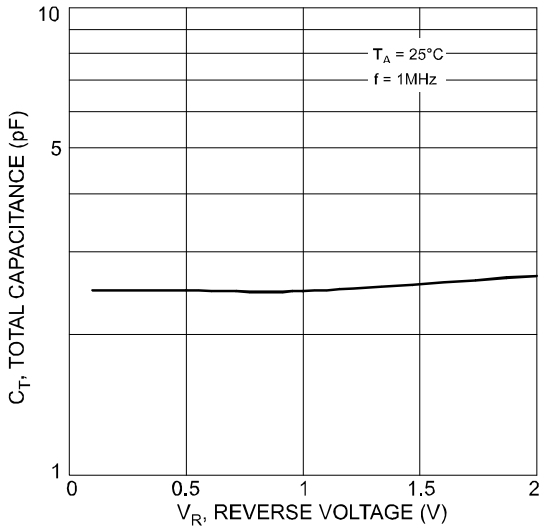


Fig. 3 Typical Total Capacitance vs. Reverse Voltage (Per Element)

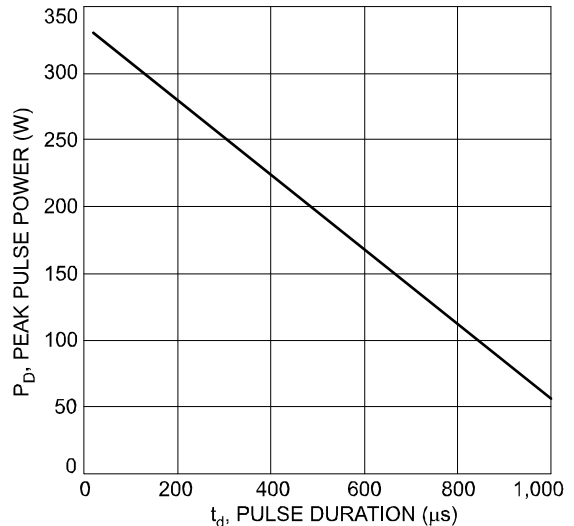


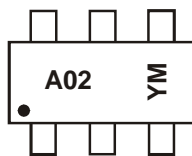
Fig. 4 Max. Peak Pulse Power vs. Pulse Time

Ordering Information (Note 8)

Part Number	Case	Packaging
DLPD3V3LC-7	SOT-26	3000/Tape & Reel

Notes: 8. For packaging details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

Marking Information



A02 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: U = 2007)
 M = Month (ex: 9 = September)

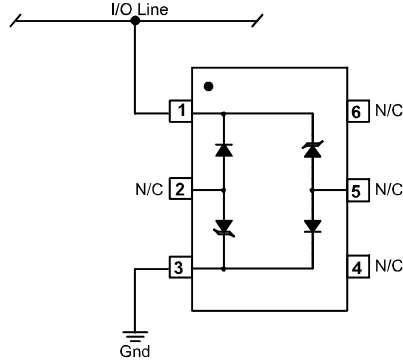
Date Code Key

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015
Code	U	V	W	X	Y	Z	A	B	C

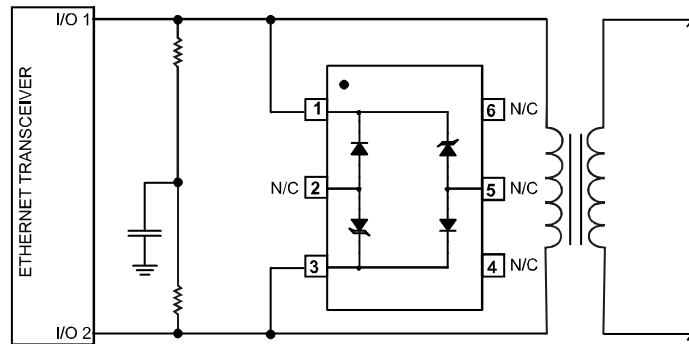
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Typical Applications

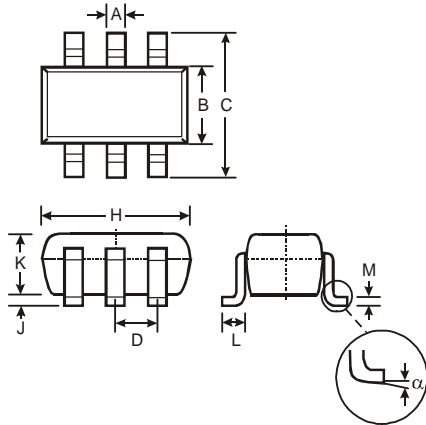
Common-Mode I/O Port Protection



Differential-Mode Ethernet Protection



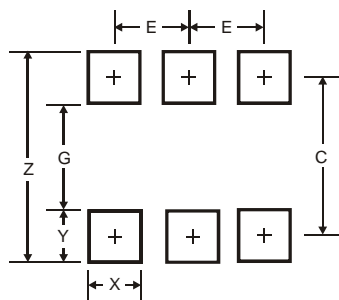
Package Outline Dimensions



SOT-26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
α	0°	8°	—

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C	2.40
E	0.95

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