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[ON Semiconductor](#)
[NSS20600CF8T1G](#)

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NSS20600CF8T1G

20 V, 7.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb-Free Device

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	-20	Vdc
Collector-Base Voltage	V_{CBO}	-20	Vdc
Emitter-Base Voltage	V_{EBO}	-7.0	Vdc
Collector Current - Continuous	I_C	-6.0	Adc
Collector Current - Peak	I_{CM}	-7.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 1)	830 6.7	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	150	$^\circ\text{C}/\text{W}$
Total Device Dissipation, $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 2)	1.4 11.1	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	90	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$ (Note 2)	15	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 sec)	$P_{D\text{single}}$ (Notes 2 & 3)	2.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

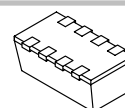
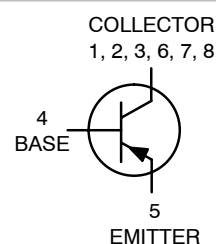
1. FR-4 @ 100 mm², 1 oz copper traces.
2. FR-4 @ 500 mm², 1 oz copper traces.
3. Thermal response.



ON Semiconductor®

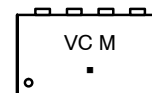
<http://onsemi.com>

-20 VOLTS, 7.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 50 m Ω



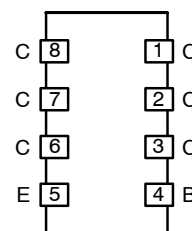
ChipFET™
 CASE 1206A
 STYLE 4

MARKING DIAGRAM



VC = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NSS20600CF8T1G	ChipFET (Pb-Free)	3000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSS20600CF8T1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Collector – Emitter Breakdown Voltage ($I_C = -10\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	-20	-	-	Vdc
Collector – Base Breakdown Voltage ($I_C = -0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	-20	-	-	Vdc
Emitter – Base Breakdown Voltage ($I_E = -0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-7.0	-	-	Vdc
Collector Cutoff Current ($V_{CB} = -20\text{ Vdc}$, $I_E = 0$)	I_{CBO}	-	-	-0.1	μA dc
Emitter Cutoff Current ($V_{EB} = -7.0\text{ Vdc}$)	I_{EBO}	-	-	-0.1	μA dc

ON CHARACTERISTICS

DC Current Gain (Note 4) ($I_C = -10\text{ mA}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -500\text{ mA}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -1.0\text{ A}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -2.0\text{ A}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -3.0\text{ A}$, $V_{CE} = -2.0\text{ V}$)	h_{FE}	250 250 220 200 180	- - 300 - -	- - - - -	
Collector – Emitter Saturation Voltage (Note 4) ($I_C = -0.1\text{ A}$, $I_B = -0.010\text{ A}$) (Note 5) ($I_C = -1.0\text{ A}$, $I_B = -0.100\text{ A}$) ($I_C = -1.0\text{ A}$, $I_B = -0.010\text{ A}$) ($I_C = -2.0\text{ A}$, $I_B = -0.020\text{ A}$) ($I_C = -3.0\text{ A}$, $I_B = -0.030\text{ A}$) ($I_C = -4.0\text{ A}$, $I_B = -0.400\text{ A}$)	$V_{CE(sat)}$	- - - - - -	-0.007 -0.050 -0.065 -0.090 -0.140 -0.160	-0.010 -0.060 -0.080 -0.130 -0.180 -0.200	V
Base – Emitter Saturation Voltage (Note 4) ($I_C = -1.0\text{ A}$, $I_B = -0.01\text{ A}$)	$V_{BE(sat)}$	-	-	-0.90	V
Base – Emitter Turn-on Voltage (Note 4) ($I_C = -2.0\text{ A}$, $V_{CE} = -3.0\text{ V}$)	$V_{BE(on)}$	-	-	-0.90	V
Cutoff Frequency ($I_C = -100\text{ mA}$, $V_{CE} = -5.0\text{ V}$, $f = 100\text{ MHz}$)	f_T	100	-	-	MHz
Input Capacitance ($V_{EB} = -0.5\text{ V}$, $f = 1.0\text{ MHz}$)	C_{ibo}	-	-	700	pF
Output Capacitance ($V_{CB} = -3.0\text{ V}$, $f = 1.0\text{ MHz}$)	C_{obo}	-	-	280	pF

SWITCHING CHARACTERISTICS

Delay ($V_{CC} = -15\text{ V}$, $I_C = 750\text{ mA}$, $I_{B1} = 15\text{ mA}$)	t_d	-	-	120	ns
Rise ($V_{CC} = -15\text{ V}$, $I_C = 750\text{ mA}$, $I_{B1} = 15\text{ mA}$)	t_r	-	-	250	ns
Storage ($V_{CC} = -15\text{ V}$, $I_C = 750\text{ mA}$, $I_{B1} = 15\text{ mA}$)	t_s	-	-	400	ns
Fall ($V_{CC} = -15\text{ V}$, $I_C = 750\text{ mA}$, $I_{B1} = 15\text{ mA}$)	t_f	-	-	250	ns

 4. Pulsed Condition: Pulse Width = 300 μsec , Duty Cycle $\leq 2\%$.

5. Guaranteed by design but not tested.

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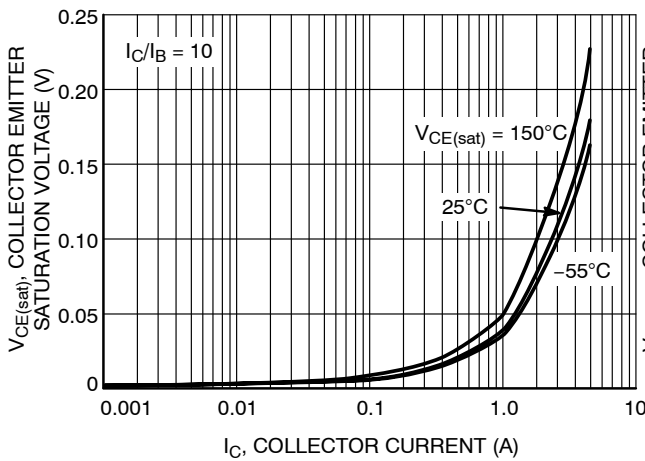


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

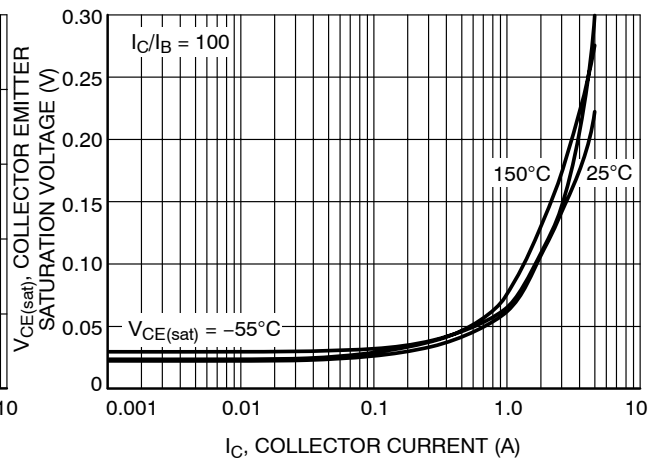


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

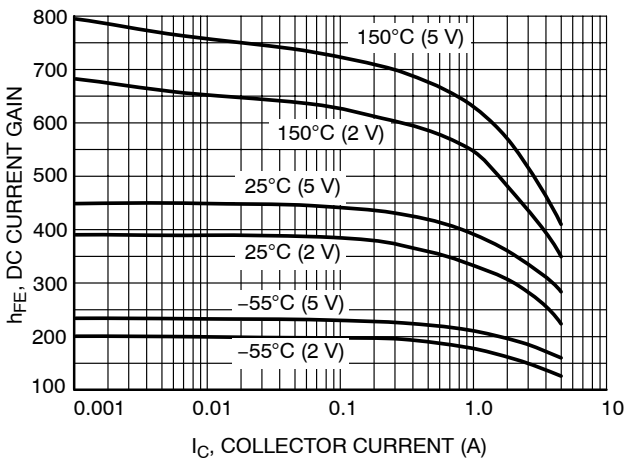


Figure 3. DC Current Gain vs. Collector Current

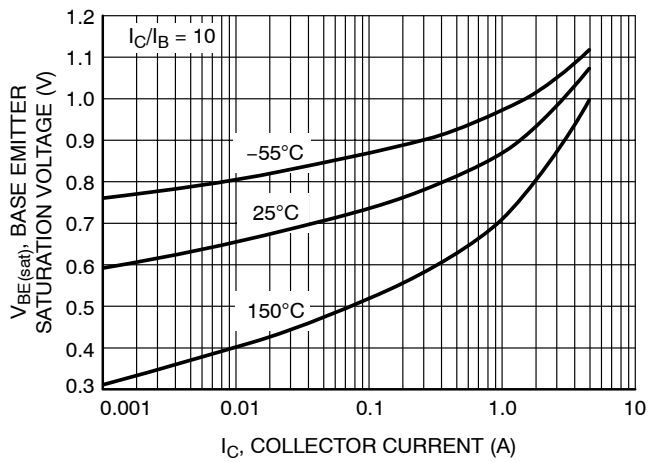


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

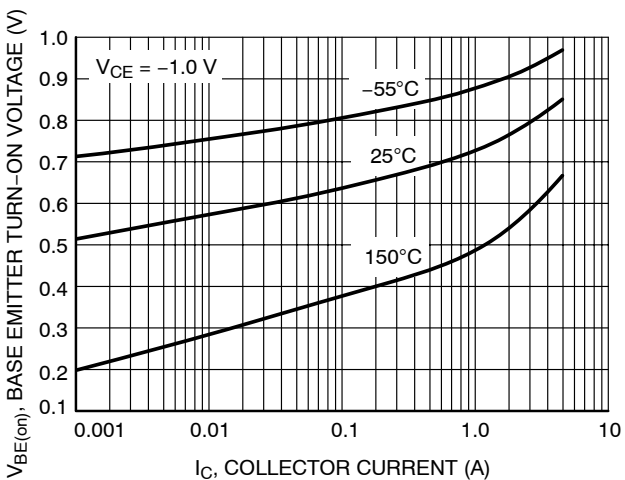


Figure 5. Base Emitter Turn-On Voltage vs. Collector Current

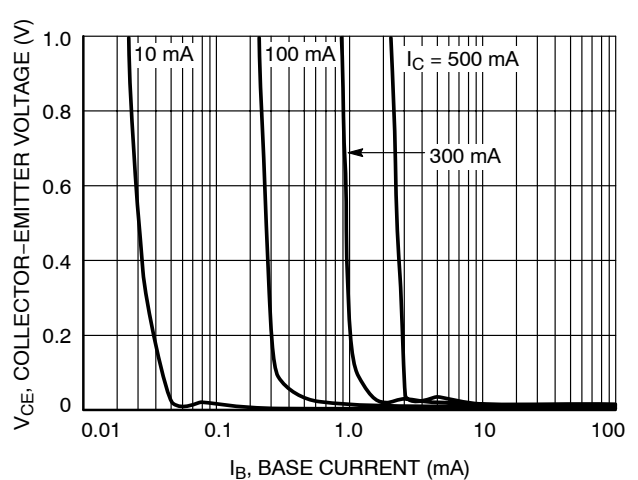


Figure 6. Saturation Region

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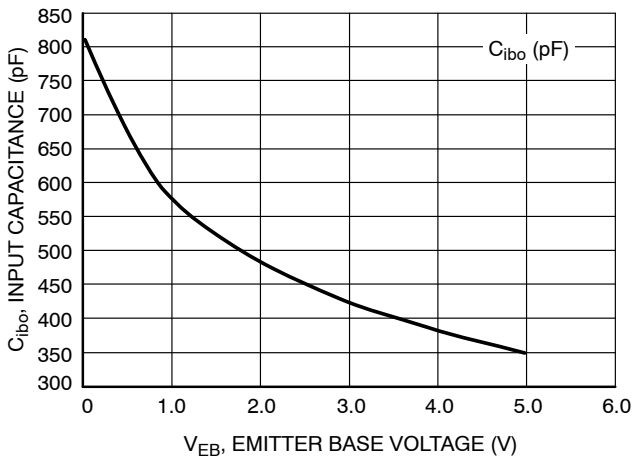


Figure 7. Input Capacitance

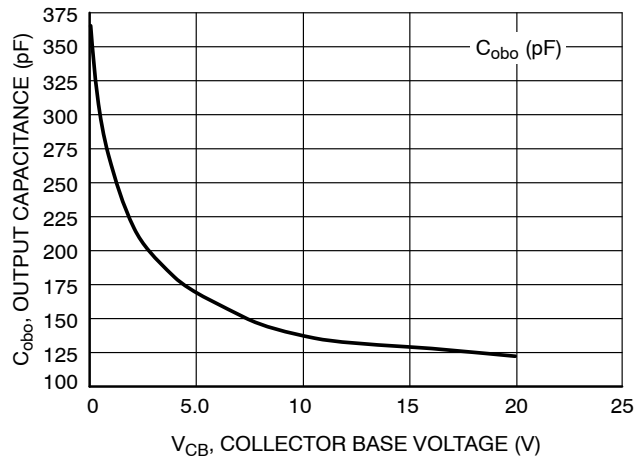


Figure 8. Output Capacitance

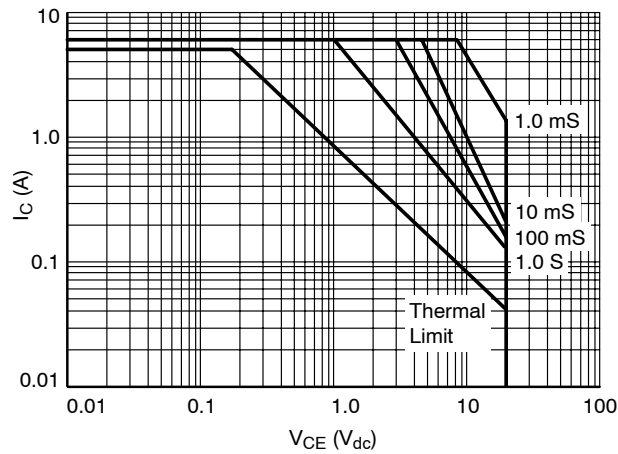
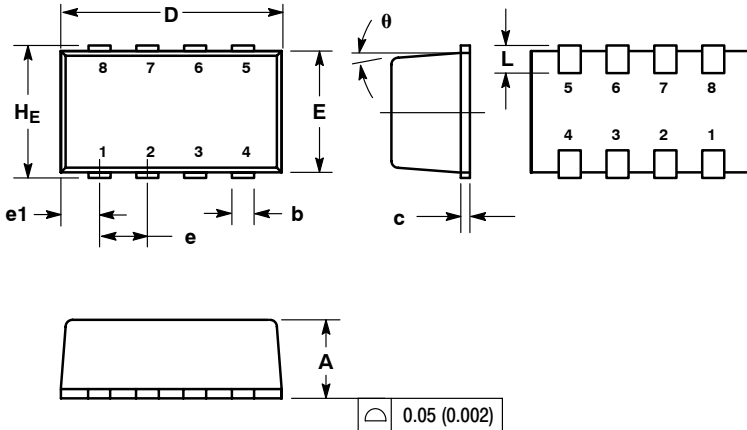


Figure 9. Safe Operating Area

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PACKAGE DIMENSIONS

ChipFET
 CASE 1206A-03
 ISSUE G



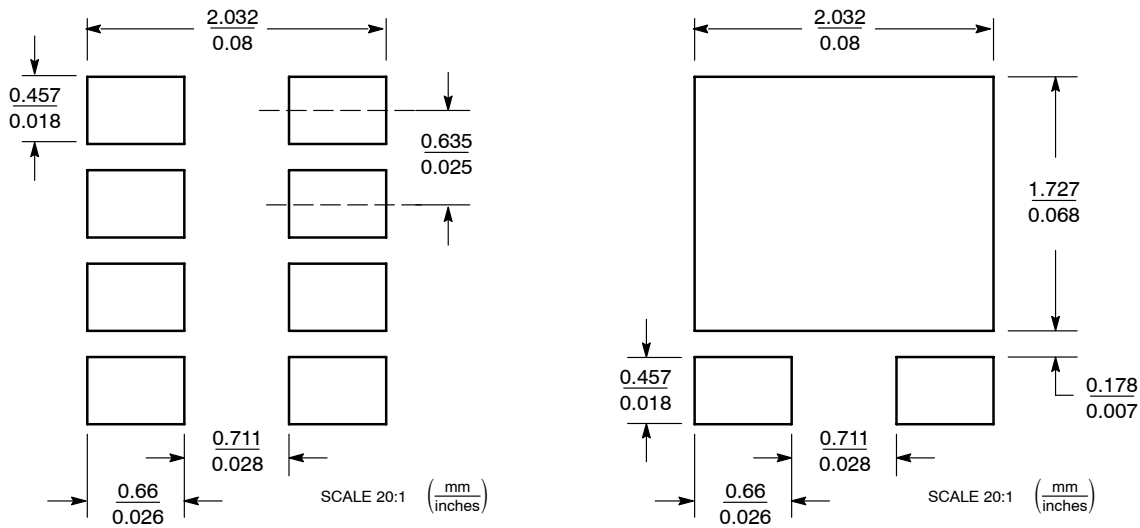
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5°NOM			5°NOM		

0.05 (0.002)

SOLDERING FOOTPRINT*



Basic

Style 4

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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