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[NTMFS4744NT1G](#)

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sales@integrated-circuit.com

NTMFS4744N

Power MOSFET

30 V, 53 A, Single N-Channel, SO-8 FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DS}	30	V		
Gate-to-Source Voltage	V_{GS}	20	V		
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	11	A	
		$T_A = 85^\circ\text{C}$	8.0		
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	2.2	W		
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	7.0	A	
		$T_A = 85^\circ\text{C}$	5.0		
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	0.88	W		
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	53	A	
		$T_C = 85^\circ\text{C}$	38		
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	47.2	W		
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	106	A
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150		$^\circ\text{C}$	
Source Current (Body Diode)	I_S	46		A	
Drain to Source dV/dt	dV/dt	6.0		V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50\text{ V}, V_{GS} = 10\text{ V}, I_L = 24\text{ A}_{pk}, L = 1.0\text{ mH}, R_G = 25\ \Omega$)	EAS	286		mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$	

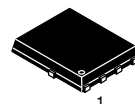
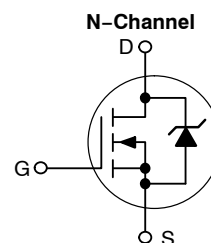
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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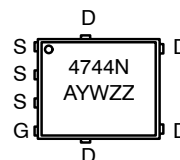
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	10 m Ω @ 10 V	53 A
	14 m Ω @ 4.5 V	



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4744N = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4744NT1G	SO-8 FL (Pb-Free)	1500 Tape & Reel
NTMFS4744NT3G	SO-8 FL (Pb-Free)	5000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.65	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	56.9	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	142.4	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			10		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	μA
					10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$		7.6		m Ω
		$I_D = 30\text{ A}$		7.3		
		$I_D = 15\text{ A}$		7.3	10	
		$I_D = 10\text{ A}$		10.4		
		$V_{GS} = 4.5\text{ V}$		10.1		
		$I_D = 10\text{ A}$		9.9	14	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		25		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		1300		μF
Output Capacitance	C_{OSS}			550		
Reverse Transfer Capacitance	C_{RSS}			132		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		10	17	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.9		
Gate-to-Source Charge	Q_{GS}			1.8		
Gate-to-Drain Charge	Q_{GD}			5.9		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		25	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}, R_G = 3.0\ \Omega$		12		ns
Rise Time	t_r			203		
Turn-Off Delay Time	$t_{d(OFF)}$			14		
Fall Time	t_f			83		

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 4)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 11.5 V, V _{DS} = 15 V, I _D = 30 A, R _G = 3.0 Ω		7.0		ns
Rise Time	t _r			94		
Turn-Off Delay Time	t _{d(OFF)}			23		
Fall Time	t _f			4.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C		0.78	1.2	V
			T _J = 125°C		0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		37	60	ns	
Charge Time	t _a			21			
Discharge Time	t _b			17			
Reverse Recovery Charge	Q _{RR}			37		nC	

PACKAGE PARASITIC VALUES

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Source Inductance	L _S	T _A = 25°C		0.65		nH
Drain Inductance	L _D			0.005		
Gate Inductance	L _G			1.84		
Gate Resistance	R _G			2.0	5.0	

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES

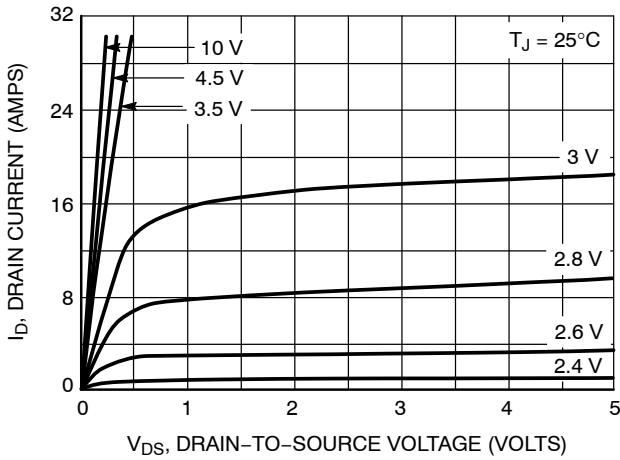


Figure 1. On-Region Characteristics

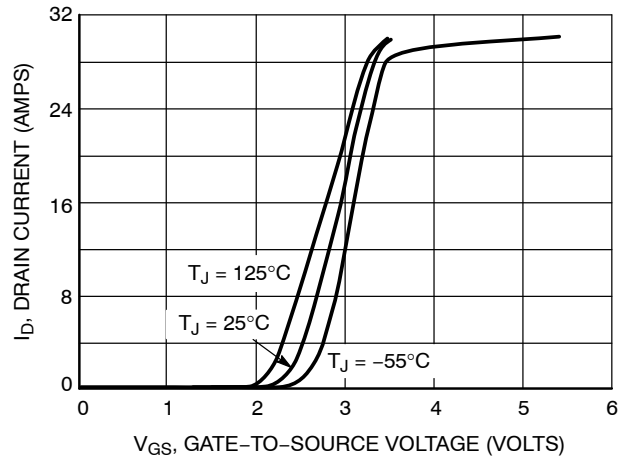


Figure 2. Transfer Characteristics

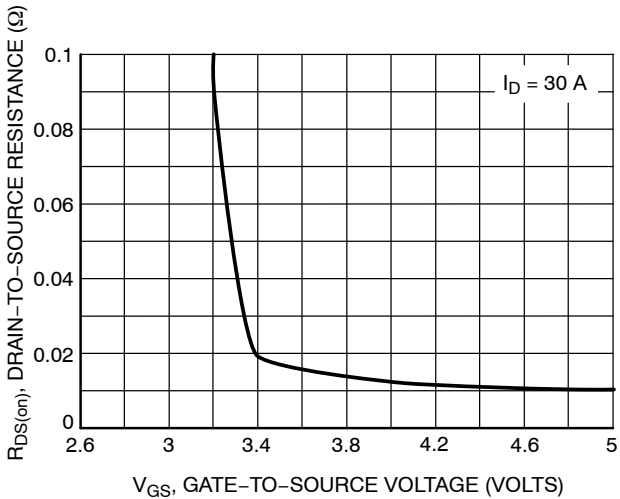


Figure 3. On-Resistance vs. Gate-to-Source Voltage

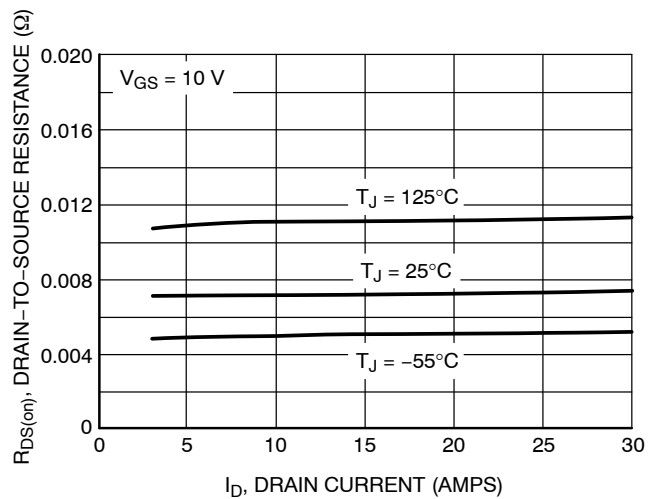


Figure 4. On-Resistance vs. Drain Current and Temperature

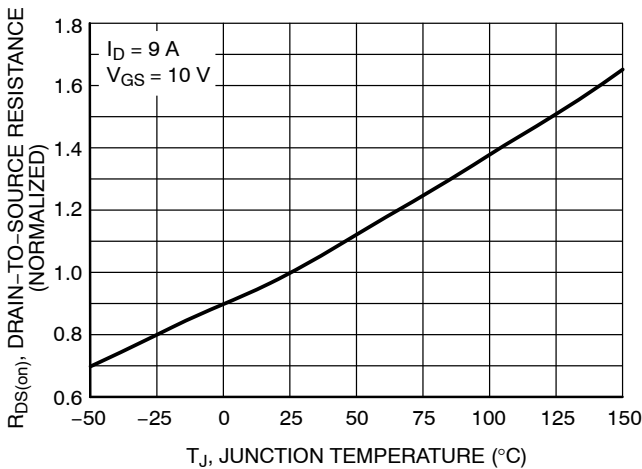


Figure 5. On-Resistance Variation with Temperature

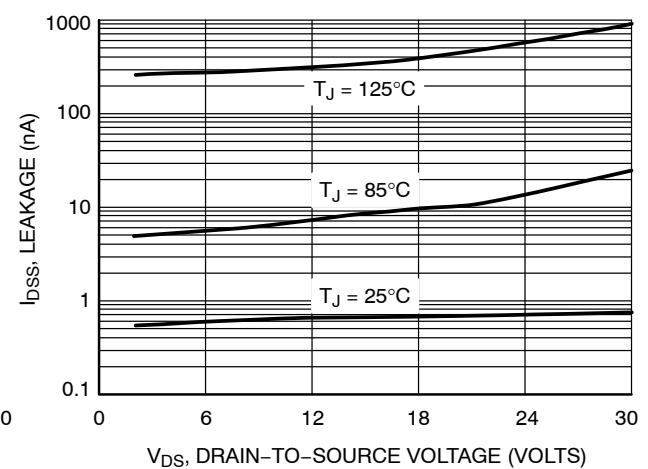


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

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TYPICAL PERFORMANCE CURVES

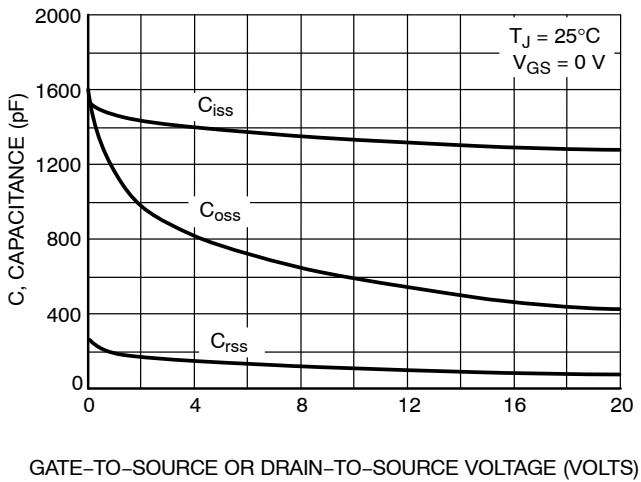


Figure 7. Capacitance Variation

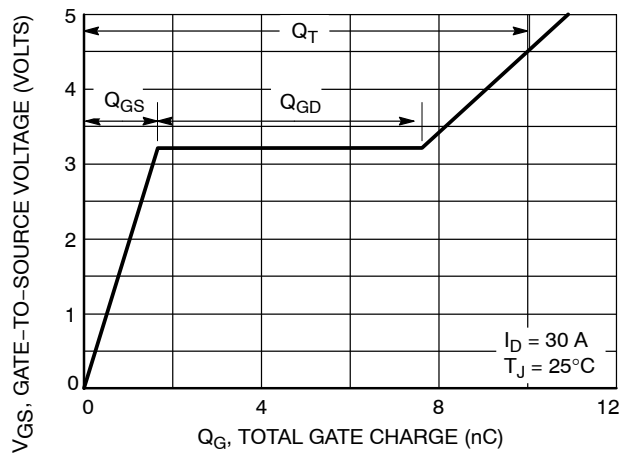


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

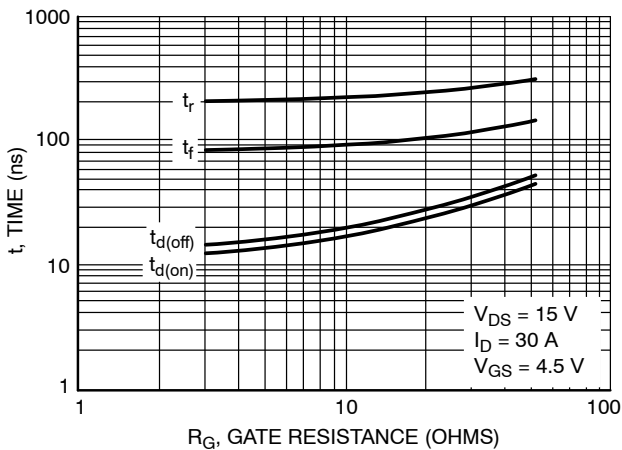


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

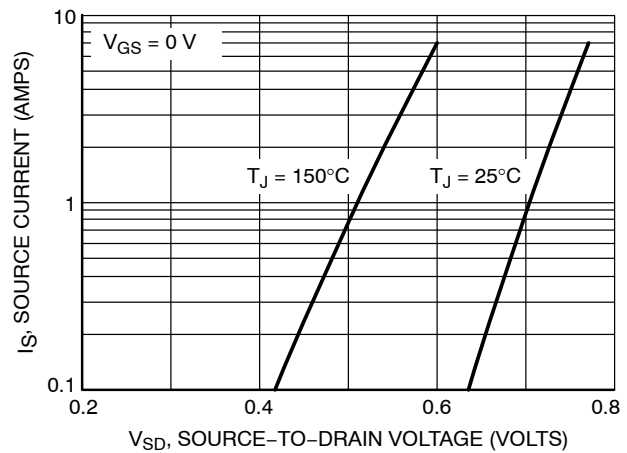


Figure 10. Diode Forward Voltage vs. Current

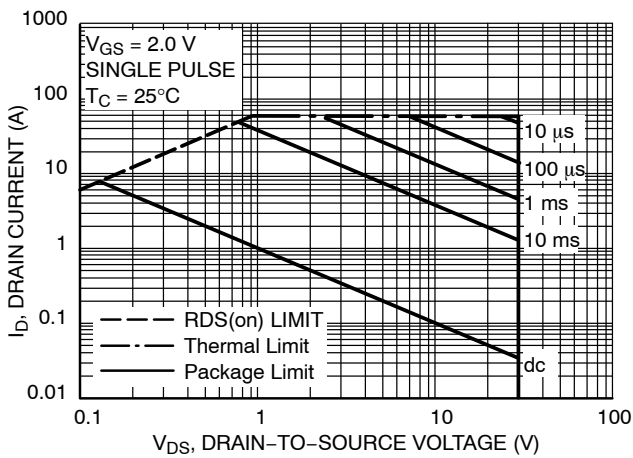


Figure 11. Maximum Rated Forward Biased Safe Operating Area

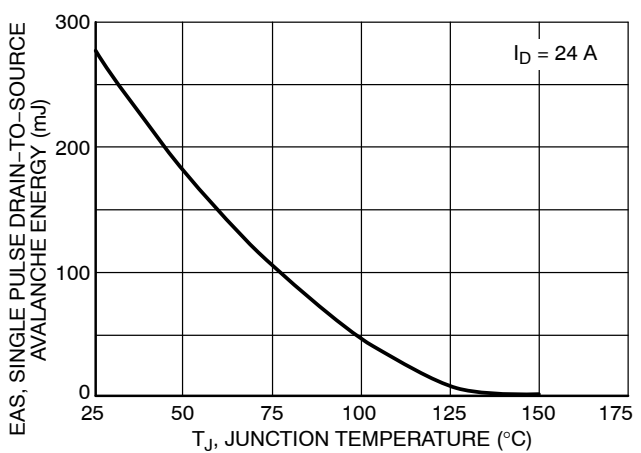


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL PERFORMANCE CURVES

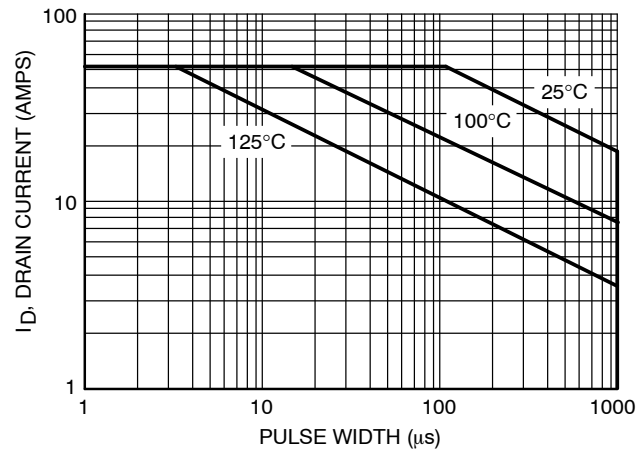
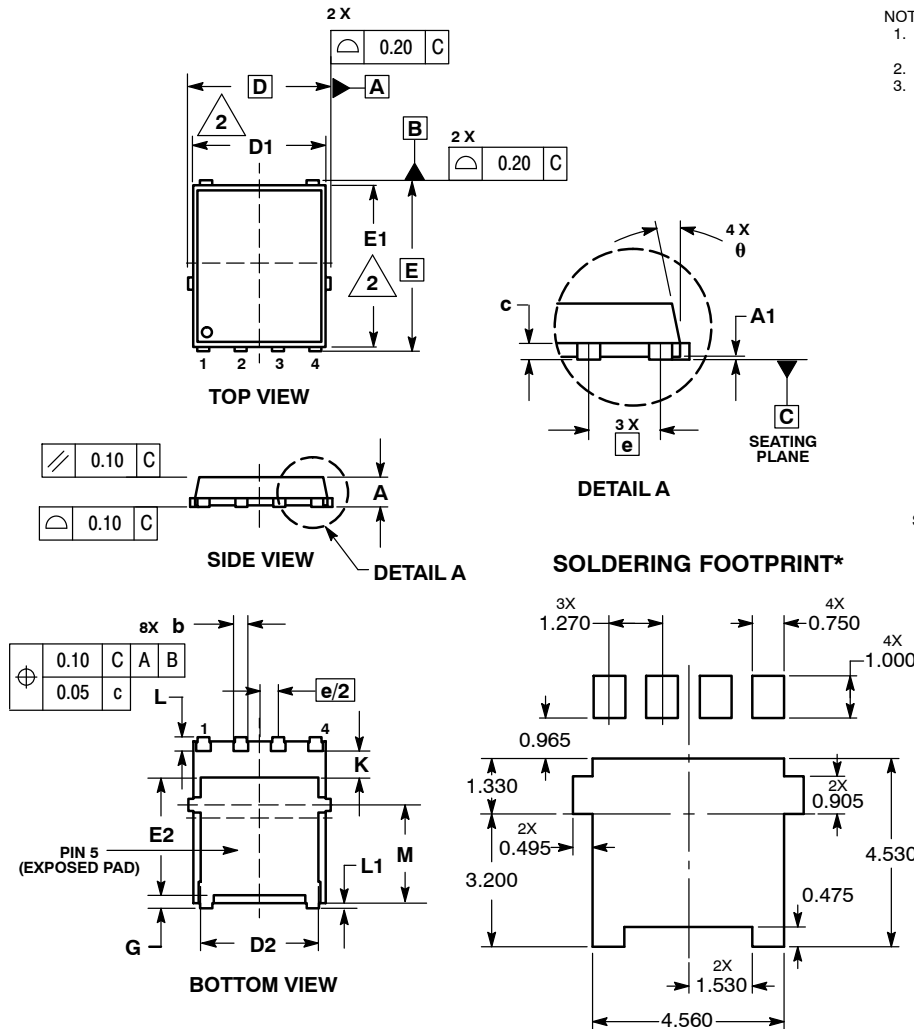


Figure 13. Avalanche Characteristics

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PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE G



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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