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[ON Semiconductor](#)  
[NUP412VP5T5G](#)

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# NUP412VP5

## Low Capacitance Quad Array for ESD Protection

This integrated transient voltage suppressor device (TVS) is designed for applications requiring transient overvoltage protection. It is intended to be used in sensitive equipment such as wireless headsets, PDAs, digital cameras, computers, printers, communication systems, and other applications. The integrated design provides very effective and reliable protection for four separate lines using only one package. This device is ideal for situations where board space is at a premium.

### Features

- ESD Protection: IEC61000-4-2: Level 4
- Four Separate Unidirectional Configurations for Protection
- Low Leakage Current < 1  $\mu$ A @ 9 V
- Small SOT-953 SMT Package
- Low Capacitance
- These are Pb-Free Devices

### Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Protects Four Lines Against Transient Voltage Conditions
- Minimize Power Consumption of the System
- Minimize PCB Board Space

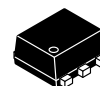
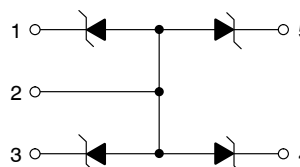
### Typical Applications

- Cellular and Portable Electronics
- Serial and Parallel Ports
- Microprocessor Based Equipment
- Notebooks, Desktops, Servers



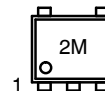
ON Semiconductor®

<http://onsemi.com>



SOT-953  
CASE 526AB

### MARKING DIAGRAM



2 = Specific Device Code  
 M = Date & Assembly Code

### ORDERING INFORMATION

Device	Package	Shipping†
NUP412VP5T5G	SOT-953 (Pb-Free)	8000 / Tape & Reel

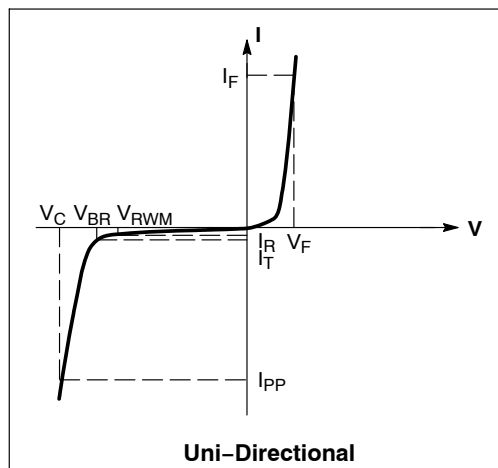
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## NUP412VP5

### ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current
V <sub>C</sub>	Clamping Voltage @ I <sub>PP</sub>
V <sub>RWM</sub>	Working Peak Reverse Voltage
I <sub>R</sub>	Maximum Reverse Leakage Current @ V <sub>RWM</sub>
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>
I <sub>T</sub>	Test Current
θV <sub>BR</sub>	Maximum Temperature Coefficient of V <sub>BR</sub>
I <sub>F</sub>	Forward Current
V <sub>F</sub>	Forward Voltage @ I <sub>F</sub>
Z <sub>ZT</sub>	Maximum Zener Impedance @ I <sub>ZT</sub>
I <sub>ZK</sub>	Reverse Current
Z <sub>ZK</sub>	Maximum Zener Impedance @ I <sub>ZK</sub>



### MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Peak Power Dissipation (8 X 20 μs @ T <sub>A</sub> = 25°C) (Note 1)	P <sub>PK</sub>	18	W
Thermal Resistance Junction-to-Ambient Above 25°C, Derate	R <sub>θJA</sub>	560 4.5	°C/W mW/°C
Maximum Junction Temperature	T <sub>Jmax</sub>	150	°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature (10 seconds duration)	T <sub>L</sub>	260	°C
Human Body Model (HBM) Machine Model (MM)	ESD	8000 400	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Non-repetitive current.

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

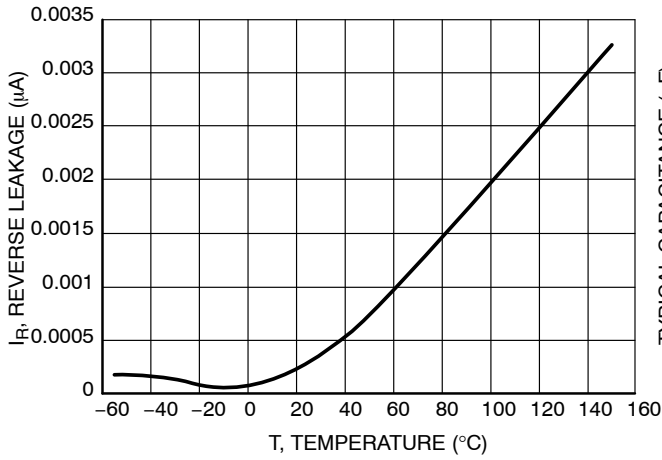
Device	Device Marking	Breakdown Voltage V <sub>BR</sub> @ 5 mA (Volts)			Leakage Current I <sub>RM</sub> @ V <sub>RM</sub>		Typ Capacitance @ 0 V Bias (pF) (Note 2)		Typ Capacitance @ 3 V Bias (pF) (Note 2)	
		Min	Nom	Max	V <sub>RWM</sub>	I <sub>RWM</sub> (μA)	Typ	Max	Typ	Max
NUP412VP5 (Note 3)	2	11.4	12	12.7	9.0	0.5	6.5	10	3.5	5.0

2. Capacitance of one diode at f = 1 MHz, T<sub>A</sub> = 25°C.

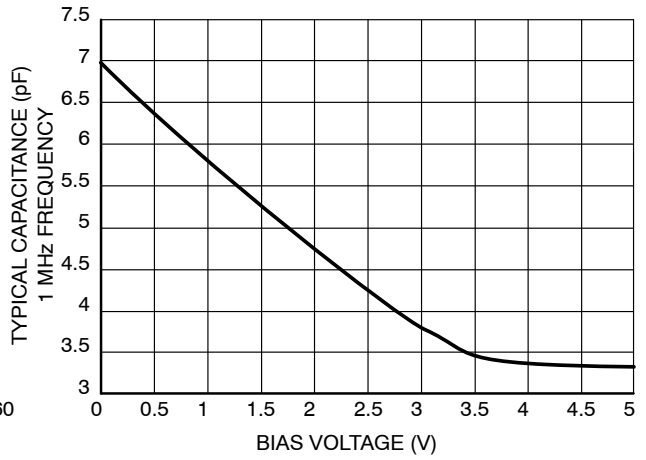
3. V<sub>BR</sub> at 5 mA.

**NUP412VP5**

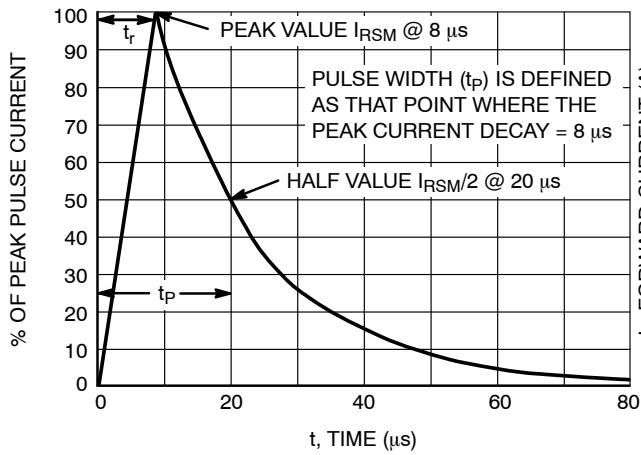
**TYPICAL ELECTRICAL CHARACTERISTICS**



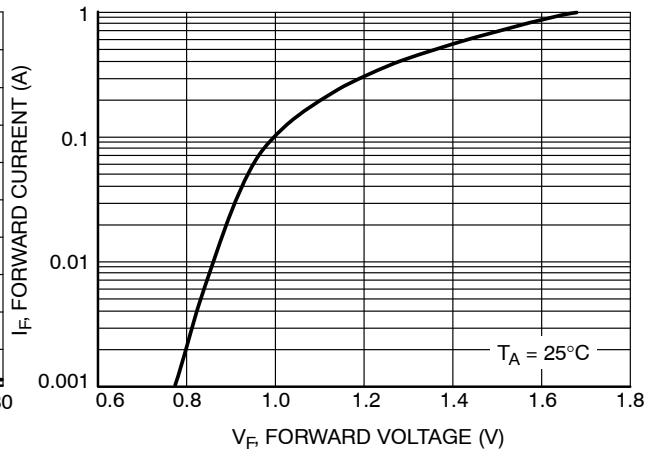
**Figure 1. Reverse Leakage versus Temperature**



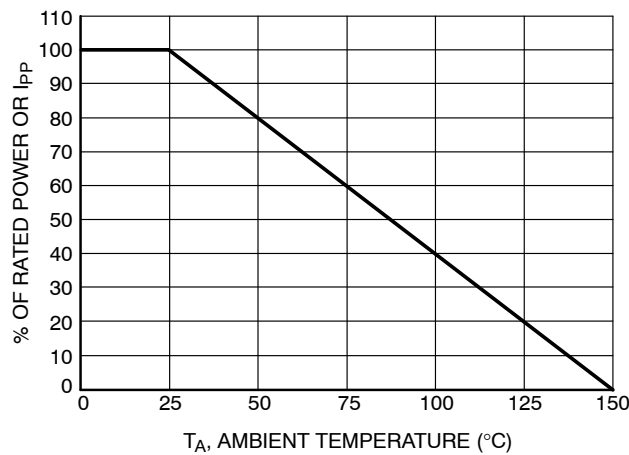
**Figure 2. Capacitance**



**Figure 3. 8 × 20 µs Pulse Waveform**



**Figure 4. Forward Voltage**

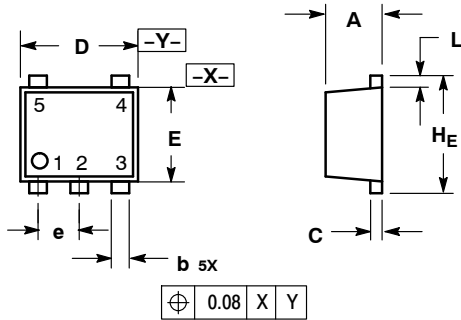


**Figure 5. Power Derating Curve**

## NUP412VP5

### PACKAGE DIMENSIONS

SOT-953  
CASE 527AB-01  
ISSUE B

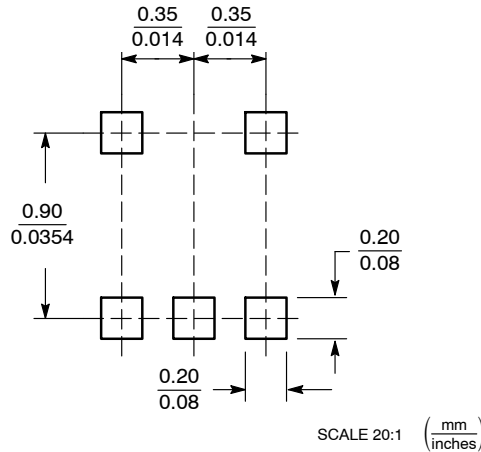


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.42	0.50	0.013	0.017	0.020
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.05	0.10	0.15	0.002	0.004	0.006
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H <sub>E</sub>	0.95	1.00	1.05	0.037	0.039	0.041

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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