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[Texas Instruments](#)  
[MM5452N/NOPB](#)

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## MM5452/MM5453 Liquid Crystal Display Drivers

Check for Samples: [MM5452](#), [MM5453](#)

### FEATURES

- Serial Data Input
- No Load Signal Required
- **DATA ENABLE (MM5452)**
- Wide Power Supply Operation
- TTL Compatibility
- 32 or 33 Outputs
- Alphanumeric and Bar Graph Capability
- Cascaded Operation Capability

### APPLICATIONS

- COPS™ or Microprocessor Displays
- Industrial Control Indicator
- Digital Clock, Thermometer, Counter, Voltmeter
- Instrumentation Readouts
- Remote Displays

### DESCRIPTION

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin PDIP package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

### Block Diagram

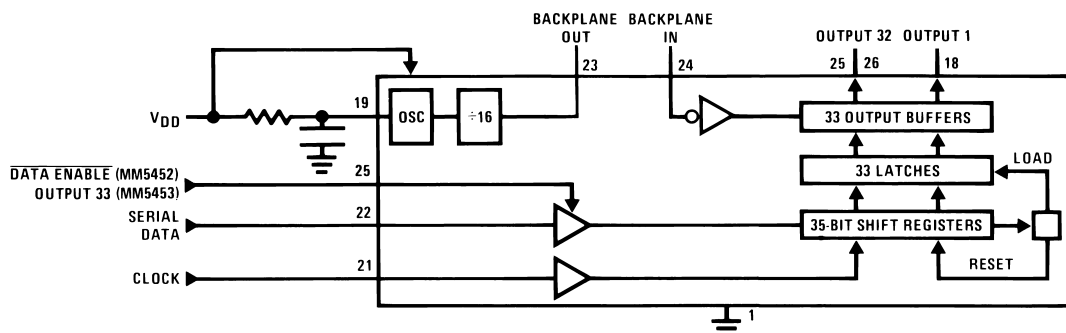


Figure 1.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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## MM5452, MM5453

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### Absolute Maximum Ratings <sup>(1)(2)</sup>

Voltage at Any Pin, Referenced to Gnd	-0.3V to +10V
Storage Temperature	-65°C to +150°C
Power Dissipation at 25°C	350mW
Power Dissipation at 70°C	300mW
Junction Temperature	+150°C
Lead Temperature (Soldering, 10s)	300°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

### Recommended Operating Conditions

V <sub>DD</sub>	3V to 10V
Operating Temperature	-40°C to 85°C

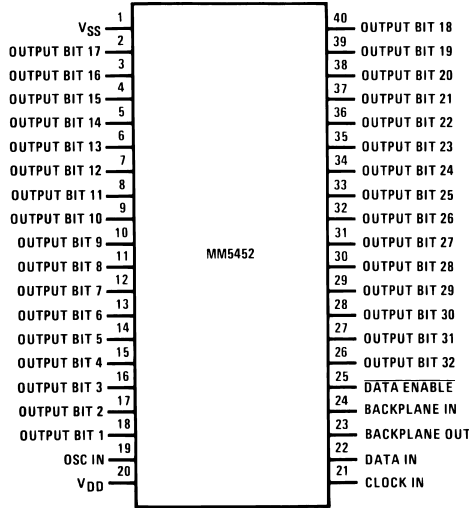
### Electrical Characteristics

 T<sub>A</sub> within operating range, V<sub>DD</sub> = 3.0V to 10V, V<sub>SS</sub> = 0V unless otherwise specified.

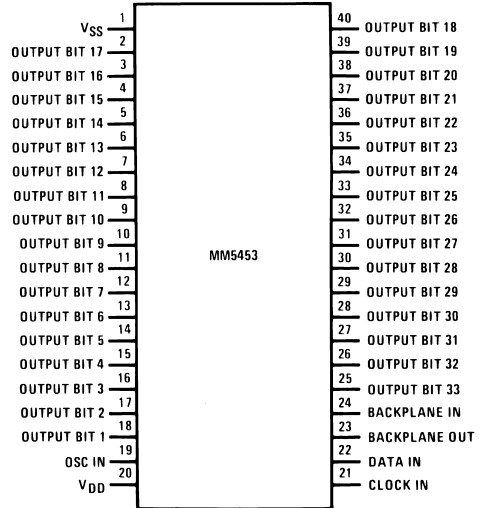
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage, V <sub>DD</sub>		3		10	V
Average Supply Current, I <sub>DD</sub>	All Outputs Open, Clock=Gnd, Data=Gnd, OSC=Gnd, BP_IN @ 32Hz				
	V <sub>DD</sub> = 5V			10	μA
	V <sub>DD</sub> = 10V			40	μA
Input Logical '0' Voltage, V <sub>IL</sub>	V <sub>DD</sub> = 3V			0.4	V
	V <sub>DD</sub> = 5V			0.8	V
	V <sub>DD</sub> = 10V			0.8	V
Input Logical '1' Voltage, V <sub>IH</sub>	V <sub>DD</sub> = 3V	2.0			V
	V <sub>DD</sub> = 5V	2.0			V
	V <sub>DD</sub> = 10V	8.0			V
Segment Sink Current, I <sub>OL</sub>	V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 0.3V	-20	-40		μA
Segment Source Current, I <sub>OH</sub>	V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 2.7V	20	40		μA
Backplane Out Sink Current, I <sub>OL</sub>	V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 0.3V	-320	-500		μA
Backplane Out Source Current, I <sub>OH</sub>	V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 2.7V	320	500		μA
Segment Output Offset Voltage	Segment Load = 250pF <sup>(1)</sup>			+/-50	mV
Backplane Output Offset Voltage	Backplane Load = 8750pF <sup>(1)</sup>			+/-50	mV
Backplane Out Frequency	R <sub>OSC_IN</sub> = 50kΩ, C <sub>OSC_IN</sub> = 0.01μF		75		Hz
Clock Input Frequency, f <sub>CLOCK</sub> <sup>(2)</sup>	V <sub>DD</sub> = 3V <sup>(1) (3)</sup>			500	kHz
	V <sub>DD</sub> = 5V <sup>(1)</sup>			750	kHz
	V <sub>DD</sub> = 10V <sup>(1)</sup>			1.0	MHz
Clock Input Duty Cycle <sup>(2)</sup>		40		60	%
Data Input Set-Up Time, t <sub>DS</sub>		300			ns
Data Input Hold Time, t <sub>DH</sub>		300			ns
DataEnable Set-up Time, t <sub>DES</sub>		100			ns

- (1) This parameter is ensured (but not production tested) over the operating temperature range and the operating supply voltage range. Not to be used in Q.A. testing.
- (2) Clock input rise time (t<sub>r</sub>) and fall time (t<sub>f</sub>) must not exceed 300ns
- (3) AC input waveform for test purposes: t<sub>r</sub> ≤ 20ns, t<sub>f</sub> ≤ 20ns, f<sub>CLOCK</sub> = 500kHz, Duty Cycle = 50% ±10%

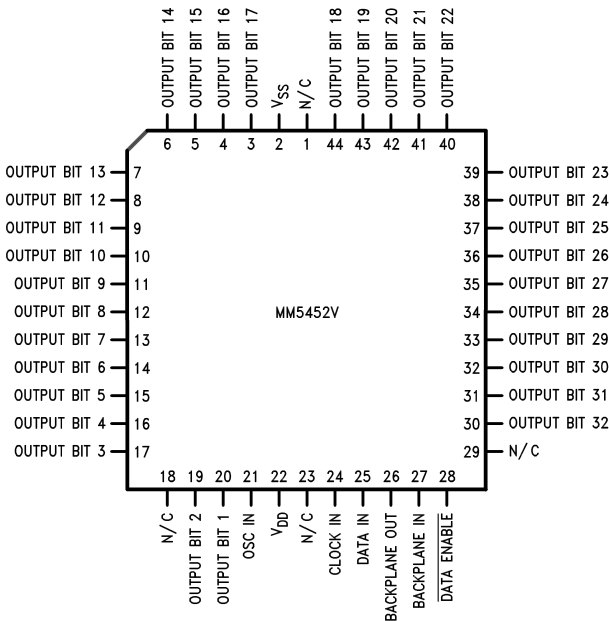
**Connection Diagram**



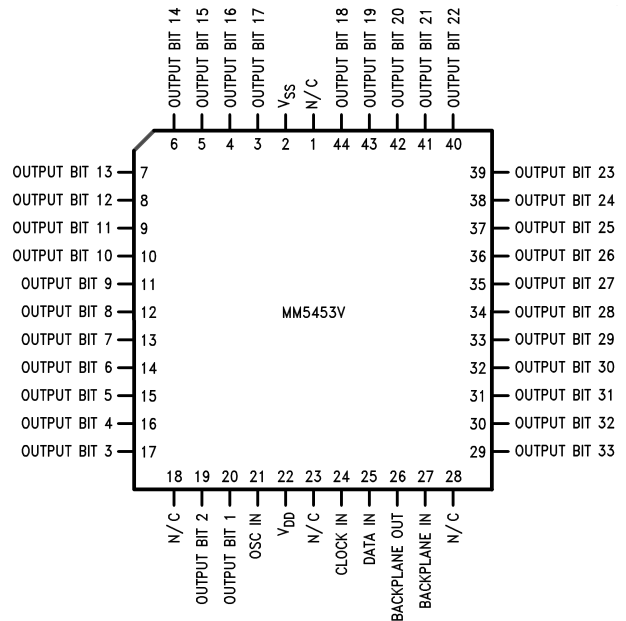
**Figure 2. Top View**  
See Package Number NFJ0040A



**Figure 3. Top View**  
See Package Number NFJ0040A



**Figure 4. Top View**  
See Package Number FN0044A



**Figure 5. Top View**  
See Package Number FN0044A

## MM5452, MM5453

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### FUNCTIONAL DESCRIPTION

The MM5452 is specifically designed to operate 4½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading “1” followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in Figure 1. For the MM5452 a  $\overline{\text{DATA ENABLE}}$  is used instead of the 33rd output. If the  $\overline{\text{DATA ENABLE}}$  signal is not required, the 33rd output can be brought out. This is the MM5453 device.

Figure 7 shows the input data format. A start bit of logical “1” precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be at least a complete set of 36 clocks otherwise the shift registers will not load and clear.

Bit 1 is the first bit following the start bit and it will appear on device pin 18 of the MM5452N and MM5453N, and on device pin 20 of the MM5452V and MM5453V.

Figure 6 shows the timing relationships between data, clock and  $\overline{\text{DATA ENABLE}}$ .

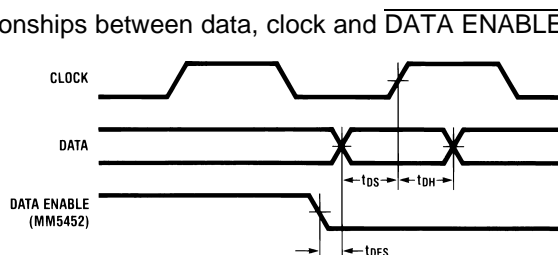


Figure 6. Timing Diagram

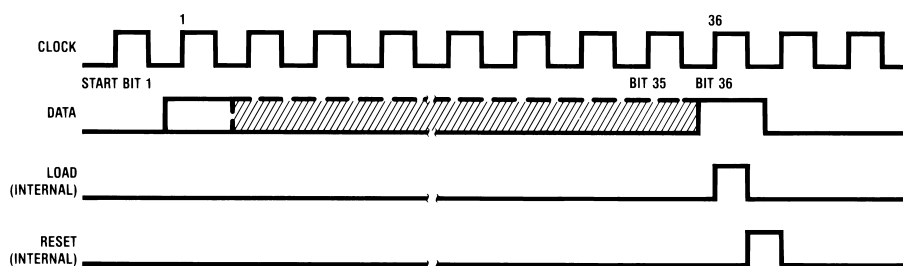
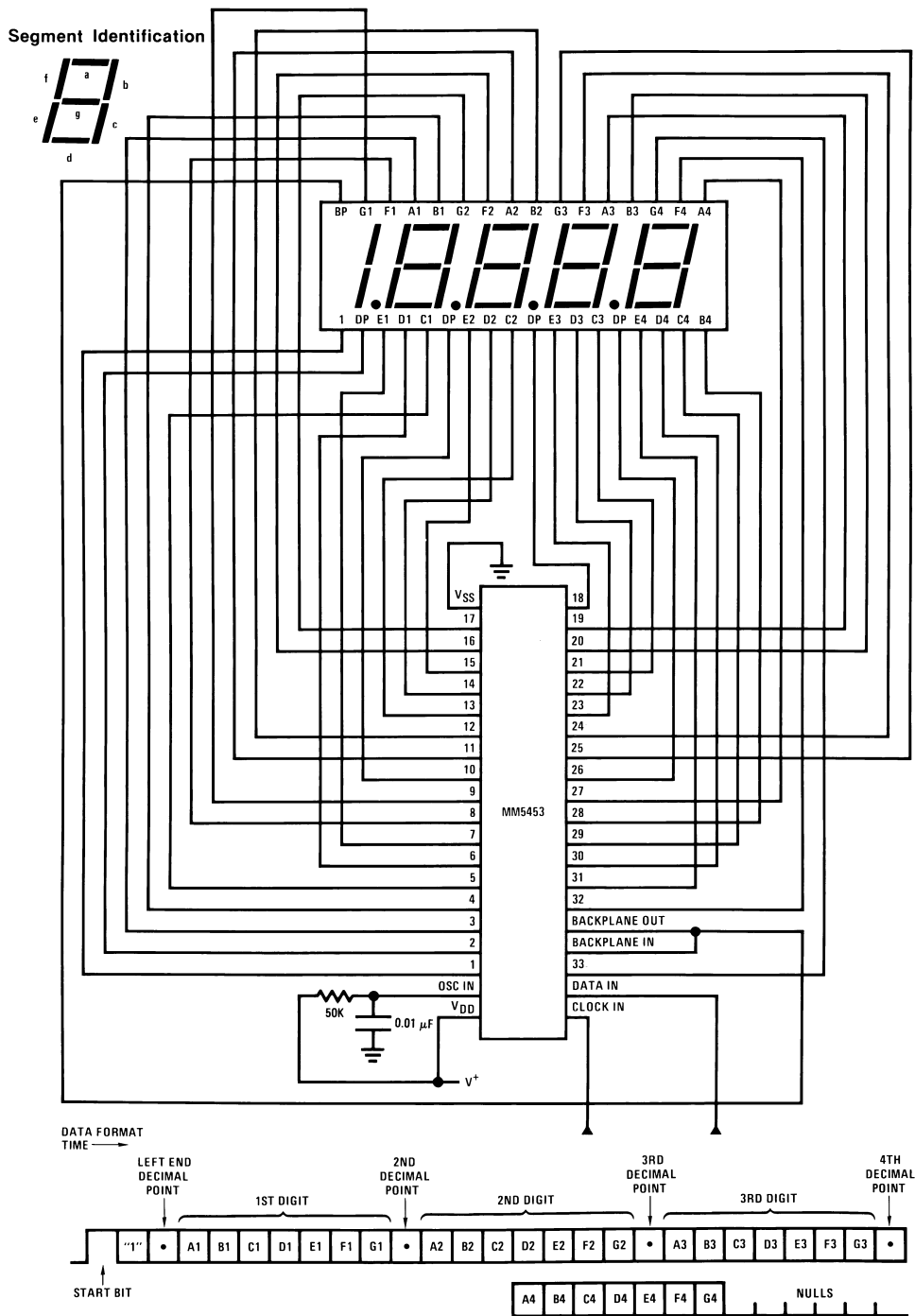


Figure 7. Input Data Format

Figure 8 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. The application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.



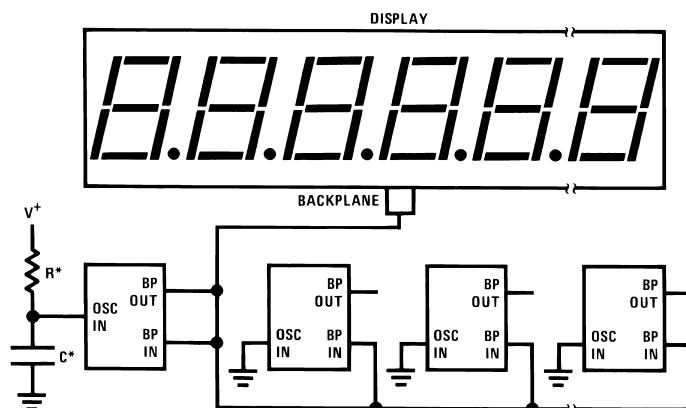
Consult LCD manufacturer's data sheet for specific pinouts.

**Figure 8. Typical 4 1/2-Digit Display Application**

**MM5452, MM5453**

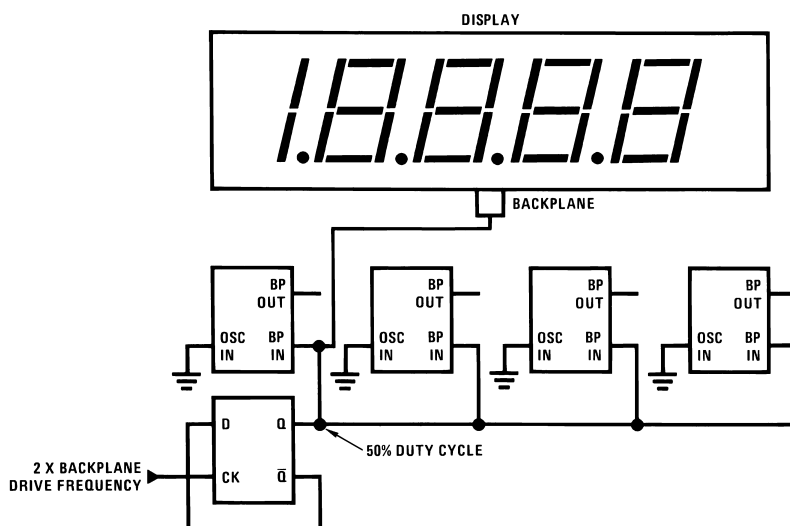
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\*The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately  $4.91 \times 10^{-4}$  should produce a backplane frequency between 30 Hz and 150 Hz.

**Figure 9. Parallel Backplane Outputs**



**Figure 10. External Backplane Clock**

Figure 11 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

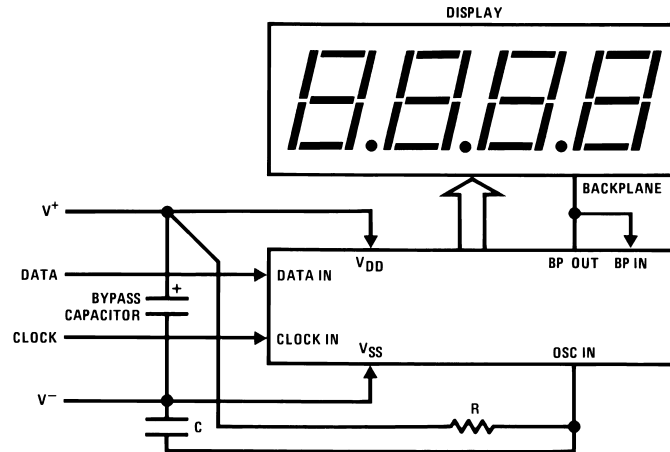
**USING AN EXTERNAL CLOCK**

The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In Figure 10, a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

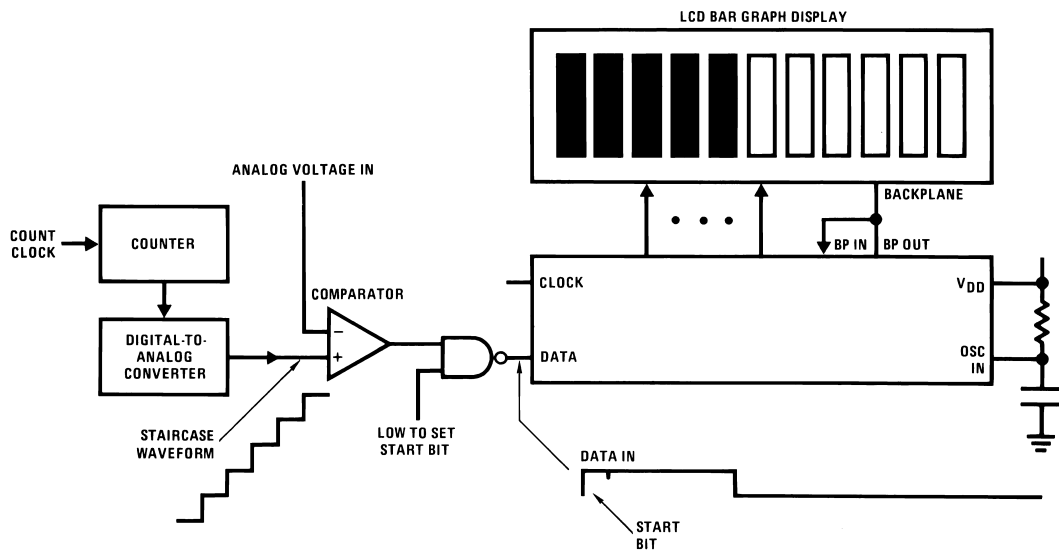
Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 12 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.



**Figure 11. Four Wire Remote Display**



Data is high until staircase > input

**Figure 12. Analog Display**





**MM5452, MM5453**



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**REVISION HISTORY**

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">7</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MM5452N	NRND	PDIP	NFJ	40		TBD	Call TI	Call TI	-40 to 85	MM5452N	
MM5452N/NOPB	ACTIVE	PDIP	NFJ	40	9	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	MM5452N	<a href="#">Samples</a>
MM5452V	NRND	PLCC	FN	44	25	TBD	Call TI	Call TI	-40 to 85	MM5452V	
MM5452V/NOPB	ACTIVE	PLCC	FN	44	25	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	MM5452V	<a href="#">Samples</a>
MM5452VX/NOPB	ACTIVE	PLCC	FN	44	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	MM5452V	<a href="#">Samples</a>
MM5453N	NRND	PDIP	NFJ	40	9	TBD	Call TI	Call TI	-40 to 85	MM5453N	
MM5453N/NOPB	ACTIVE	PDIP	NFJ	40	9	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	MM5453N	<a href="#">Samples</a>
MM5453V/NOPB	ACTIVE	PLCC	FN	44	25	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	MM5453V	<a href="#">Samples</a>
MM5453VX/NOPB	ACTIVE	PLCC	FN	44	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	MM5453V	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

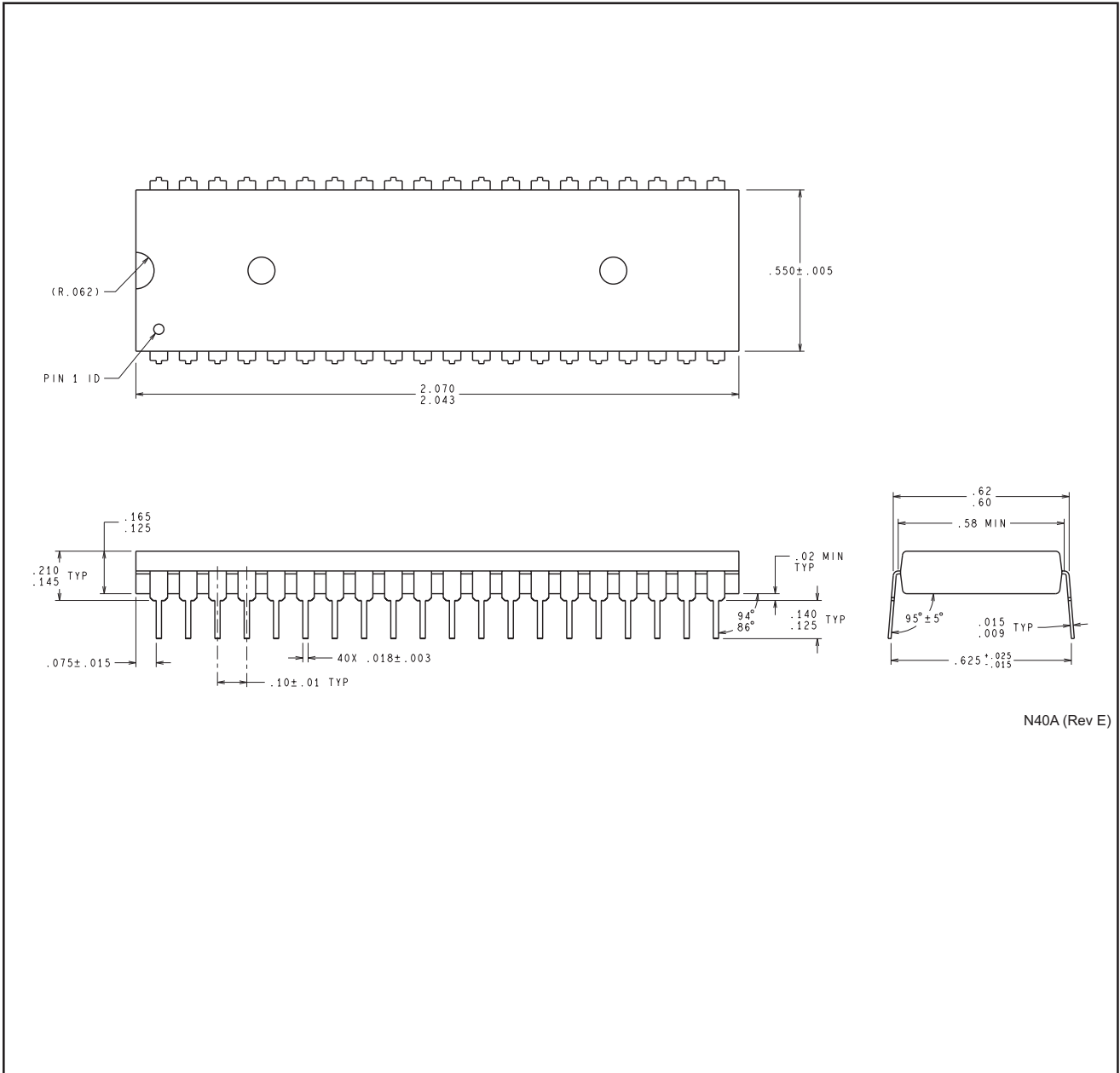
<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**MECHANICAL DATA**

**N0040A**

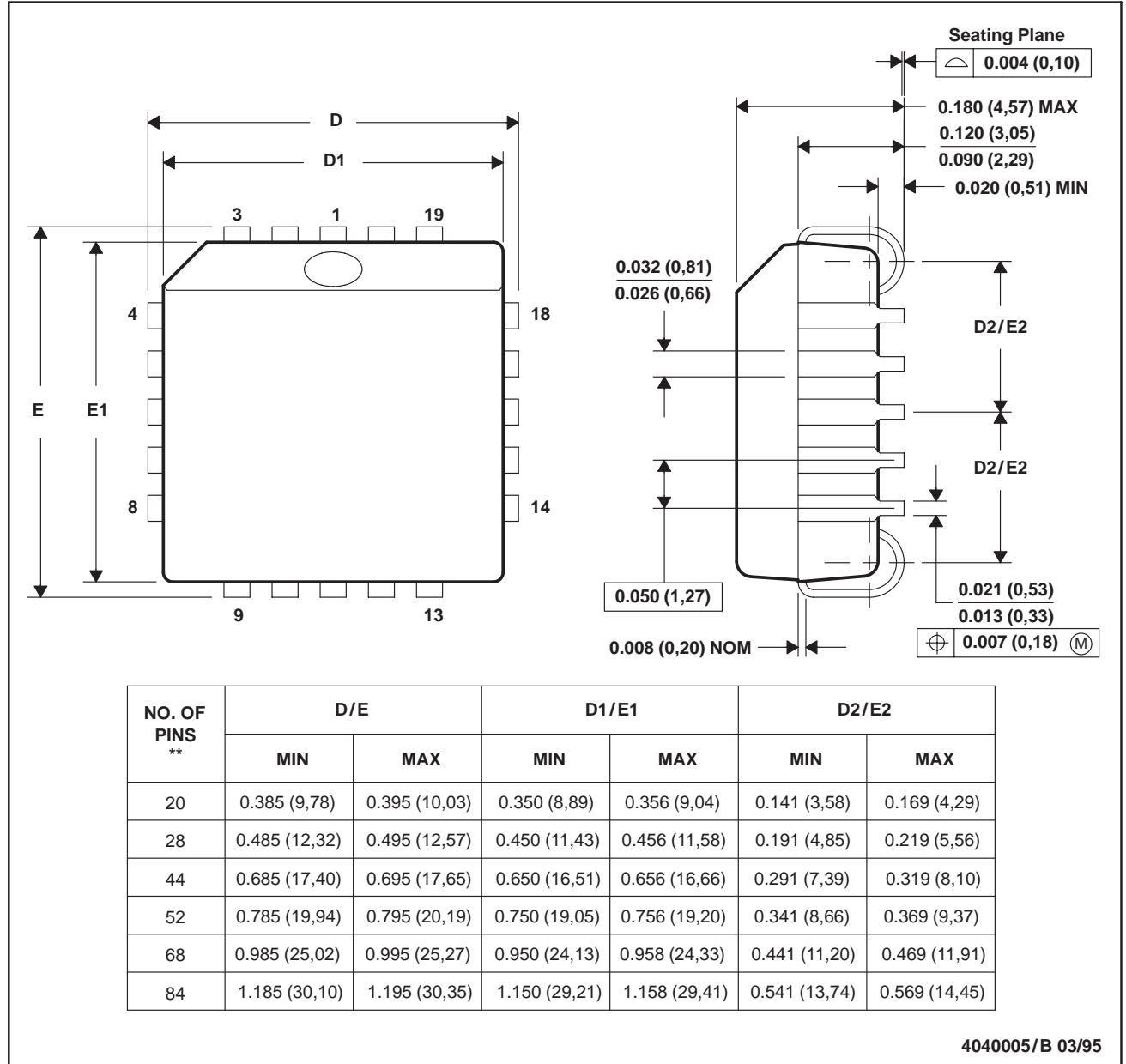


N40A (Rev E)

**FN (S-PQCC-J\*\*)**

**PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

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