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ACS8946 JAM PLL

Jitter Attenuating, Multiplying Phase Locked Loop, with Protection Switch, for OC-12/STM-4 and GbE

ADVANCED COMMUNICATIONS **FINAL** **DATASHEET**

Introduction

The ACS8946 JAM PLL is a Jitter-Attenuating, Multiplying differential Phase-Locked Loop, for generating low jitter output clocks compliant up to SONET OC-12 and STM-4 622.08 MHz specifications. Its primary function is to clean up clock jitter for high performance optical line cards with OC-12 framers and serializers. It also provides reference switching functionality for line card protection, and frequency translation.

Typical output jitter generation is within OC-12/STM-4 specifications, at 2.8 ps rms, making it an ideal dejittering solution for use with Semtech clock and line card parts: ACS8510, ACS8520, ACS8522 and ACS8530. The ACS8946 can also be used as a basic line card protection device in some applications.

The ACS8946 JAM PLL has two differential, frequency programmable, LVPECL reference inputs and one differential sync input. It has four outputs, programmable as LVPECL or CML, and frequency programmable to any common SONET/SDH rate i.e. 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz and 622.08 MHz. Jitter cleaning of Gigabit Ethernet (GbE) 125 MHz and 156.25 MHz is also possible, with output frequency multiplication up to 625.00 MHz available.

The device's operating bandwidth (and consequently the jitter attenuation point relating to this bandwidth) is fully configurable, and is set by external passive components.

Note...For items marked [1],[2], etc. references are given in full in the Reference Section on page 38.

Features

- Meets rms jitter requirements of:
  - Telcordia GR-253[8] for OC-3 and OC-12
  - ITU-T G.813[4]/G.812[3] for STM-1 and STM-4 rates
  - ETSI EN300-462-7[1]/EN302-084[2] up to STM-16 rates
- PLL bandwidth and jitter peaking fully adjustable—supports PLL loop bandwidths from 2 kHz for superior input jitter filtering
- Typical jitter generation down to:
  - 0.3 ps rms for 250 kHz to 5 MHz band for G.813, or EN300 462, at STM-4 (OC-12) rates
  - 2.8 ps rms for 12 kHz to 20 MHz band (against 4.02 ps rms for GR-253-CORE at OC-48 rate)
- ITU, ETSI and Telcordia frequency band results shows exceptional performance in a “Real World” environment (low PLL bandwidth of 2 KHz and a typical input from an ACS8525 partner IC):
  - 0.4 ps rms for 250 kHz to 5 MHz band for G.813, or EN300 462, at STM-4 (OC-12) rates
  - 2.8 ps rms for 12 kHz to 20 MHz band
- Tracking range ±400 ppm about a wide range of input frequencies
- Manual or automatic control of reference selection
- External feedback option
- LOS alarms for each input, and for selected reference
- 3.3 V operation, - 40 to +85 °C temperature range
- Small outline leadless 7 mm x 7 mm QFN48 package
- Lead (Pb)-free version available (ACS8946T), RoHS[11] and WEEE[12] compliant

Block Diagram

Figure 1 Simplified Block Diagram of the ACS8946 JAM PLL

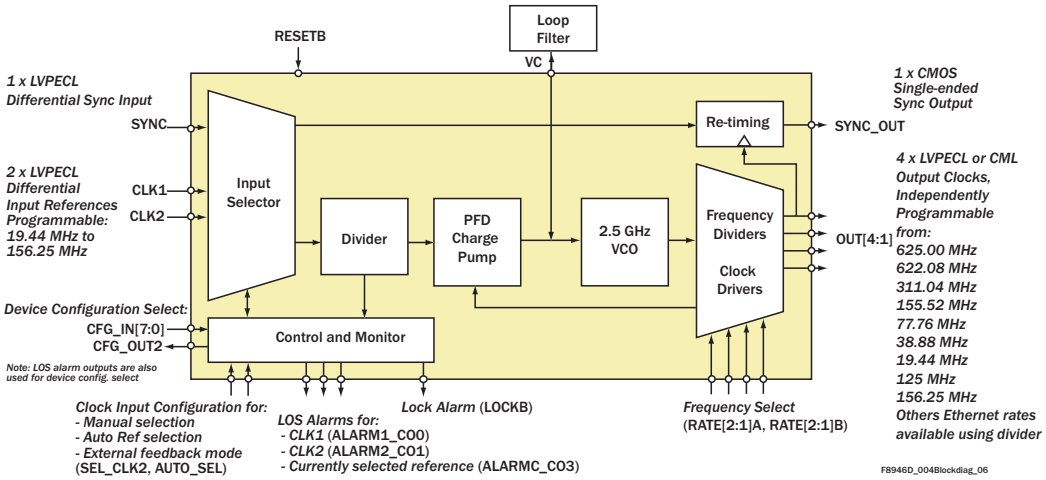

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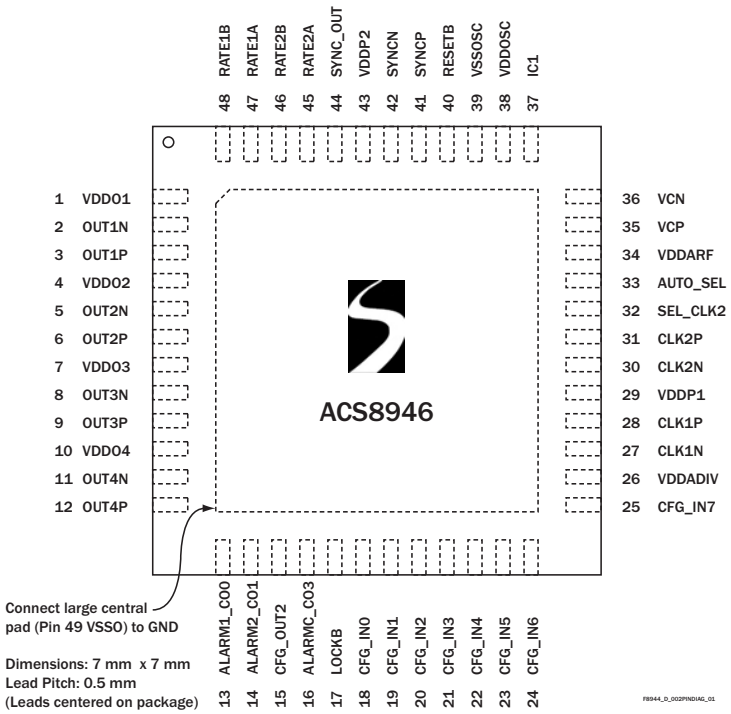
Figure 2 ACS8946 Pin Diagram



Pin Description

Table 1 Power Pins

Pin No.	Symbol	I/O	Type	Description
1, 4, 7, 10	VDDO1, VDDO2, VDDO3, VDDO4	P	-	Supply Voltage: Independent supplies to power each clock output (differential pair of pins) OUT1N/P to OUT4N/P respectively. +3.3 Volts ±5%. To disable an output and save power, tie associated VDD to 0V.
26	VDDADIV	P	-	Supply Voltage: Supply for internal Dividers in VCO loop, kept as an isolated supply to allow for low supply noise for the output divider stages. +3.3 Volts ±5%.
29	VDDP1	P	-	Supply Voltage: Supply to differential inputs, alarm and config. pins. +3.3 Volts ±5%.
43	VDDP2	P	-	Supply Voltage: Supply to Sync input and Sync output pins, rate selection pins, input selection pins and reset pin. +3.3 Volts ±5%.
34	VDDARF	P	-	Supply Voltage: Supply for phase and frequency detector (PFD), kept as an isolated supply to allow for low supply noise. +3.3 Volts ±5%.
38	VDDOSC	P	-	Supply Voltage: Supply input to the internal VCO. +3.3 Volts +5/-10%.
39	VSSOSC	P	-	Supply Ground: 0 V for the internal VCO.
49	VSS0	P	-	Supply Ground: Common 0 V. This is the central leadframe pad on the underneath of the package.

Note...A= Analog, I = Input, O = Output, P = Power, LVTTL/LVCMOS^{U} = LVTTL/LVCMOS input with pull-up resistor, LVTTL/LVCMOS$_{D}$ = LVTTL/LVCMOS input with pull-down resistor.

Table 2 Internally Connected (IC) Pin

Pin No.	Symbol	I/O	Type	Description
37	IC1	-	-	Internally Connected: Connect to ground.

Table 3 Functional Pins

Pin No.	Symbol	I/O	Type	Description
2	OUT1N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 3; programmable at spot frequencies from 19.44 MHz up to 625.00 MHz. For outputs OUT1 and OUT2 only, output frequency can be instantly configured using Rate Selection pins (pins 47 and 48 for OUT1), from a set of four pre-configured “Available Rates”. See“Configuration” on page 13. Output is on when VDD01 is supplied with 3.3 V, or off when VDD01 is tied to zero volts. If VDD01 is connected to 0 V remove external biasing resistors.
3	OUT1P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 2. See pin 2 description for more detail.
5	OUT2N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 6; programmable at spot frequencies from 19.44 MHz up to 625.00 MHz. For outputs OUT1 and OUT2 only, output frequency can be instantly configured using Rate Selection pins (pins 45 and 46 for OUT2), from a set of four pre-configured “Available Rates”. See“Configuration” on page 13. Output is on when VDD02 is supplied with 3.3 V, or off when VDD02 is tied to zero volts. If VDD02 is connected to 0 V remove external biasing resistors.
6	OUT2P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 5. See pin 5 description for more detail.
8	OUT3N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 9; programmable at spot frequencies from 19.44 MHz up to 625.00 MHz. For outputs OUT3 and OUT4 only, the output frequency selection is controlled at power-up or on reset from a set of four pre-configured “Available Rates”. See“Configuration” on page 13. Output is on when VDD03 is supplied with 3.3 V, or off when VDD03 is tied to zero volts. If VDD03 is connected to 0 V remove external biasing resistors.
9	OUT3P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 8. See pin 8 description for more detail.
11	OUT4N	O	CML or LVPECL	One of four CML or LVPECL differential outputs, partnered with pin 12; programmable at spot frequencies from 19.44 MHz up to 625.00 MHz. For outputs OUT3 and OUT4 only, the output frequency selection is controlled at power-up or on reset from a set of four pre-configured “Available Rates”. See“Configuration” on page 13. Output is on when VDD04 is supplied with 3.3 V, or off when VDD04 is tied to zero volts. If VDD04 is connected to 0 V remove external biasing resistors.
12	OUT4P	O	CML or LVPECL	CML or LVPECL differential output partnered with pin 11. See pin 11 description for more detail.
13	ALARM1_CO0	O	LVTTL/ LVCMOS	Activity alarm output for the CLK1P/CLK1N input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up, where it is used as a configuration output pin, that may be connected to CFG_IN[0:7] input pins as required. See “Configuration” on page 13.
14	ALARM2_CO1	O	LVTTL/ LVCMOS	Activity alarm output for the CLK2P/CLK2N input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up time, where it is used as a configuration output pin, that may be connected to CFG_IN[0:7] input pins as required. See “Configuration” on page 13.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
15	CFG_OUT2	O	LVTTL/ LVCMOS	Configuration pin, used in the configuration on power-up of expected input clock frequency and Resync selection, by connecting to appropriate pin from the CFG_IN[0:7] pins as required. See “Configuration” on page 13.
16	ALARMC_CO3	O	LVTTL/ LVCMOS	Activity alarm output for the currently selected input reference clock. Active high; high indicating clock failure. It is also used to configure the device at power-up, where it is used as a configuration output pin that may be connected to CFG_IN[0:7] input pins as required. See “Configuration” on page 13.
17	LOCKB	O	Analog	Lock detect output. This is a pulse-width modulated output current, with each pulse typically +10 µA. The output produces a pulse with a width in proportion to the phase error seen at the internal phase detector. This pin should be connected via an external parallel capacitor and resistor to ground. The pin voltage will then give an indication of phase lock: When low, the device is phase locked; when high the device has frequent large phase errors and so is not phase locked. The value of the RC components used determines the time and level of consistency required for lock indication. If LOCKB is disabled by configuration the LOCKB output is held low.
18	CFG_IN0	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power, or one of the configuration outputs at pins 13 to 16. This pin is used with pin 19 to set the available output rates as shown in Table 11.
19	CFG_IN1	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power, or one of the configuration outputs at pins 13 to 16. This pin is used with pin 18 to set the available output rates as shown in Table 11.
20	CFG_IN2	I	LVTTL/ $LVCMOS_D$ Schmitt Trigger	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power, or one of the configuration outputs at pins 13 to 16. This pin is used with pin 21 to set the input divider and output pad mode (CML or LVPECL) configuration for OUT1 and OUT2 as in Table 10.
21	CFG_IN3	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power, or one of the configuration outputs at pins 13 to 16. This pin is used with pin 20 to set the input divider and output pad mode (CML or LVPECL) configuration for OUT1 and OUT2 as in Table 10.
22	CFG_IN4	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power or one of the configuration outputs at pins 13 to 16. This pin is used with pin 23 to set the clock edge used for SYNC sampling, and the output clock frequency of OUT3 (pins 8 and 9) and OUT4 (pins 11 and 12), as shown in Table 12.
23	CFG_IN5	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power or one of the configuration outputs at pins 13 to 16. This pin is used with pin 22 to set the clock edge used for SYNC sampling, and the output clock frequency of OUT3 (pins 8 and 9) and OUT4 (pins 11 and 12), as shown in Table 12.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
24	CFG_IN6	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power or one of the configuration outputs at pins 13 to 16. This pin is used with pin 25 to to set the value of the odd divider, which applies a division of 1/3/5/7/9/11/13 or 15 to the otherwise selected spot frequency, on each of the four outputs OUTN/P[4:1]. It is also used to enable or disable the lock detector (pin 17 LOCKB), and to set the output pad mode (CML or PECL) for OUT3 and OUT4 as shown in Table 13.
25	CFG_IN7	I	LVTTL/ $LVCMOS_D$	Configuration pin for setting up the device just after power-up or after a system reset (via pin 40, RESETB). This configuration pin is analyzed during the configuration phase, just after power-up, so that the device works out whether this pin is connected to ground, power or one of the configuration outputs at pins 13 to 16. This pin is used with pin 24 to to set the value of the odd divider, which applies a division of 1/3/5/7/9/11/13 or 15 to the otherwise selected spot frequency on each of the four outputs OUTN/P[4:1]. It is also used to enable or disable the lock detector (pin 17 LOCKB) and to set the output pad mode (CML or PECL) for OUT3 and OUT4 as shown in Table 13.
27	CLK1N	I	LVPECL	Input reference clock that the PLL will phase and frequency lock to. Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz or 156.25 MHz, and frequencies near to these so long as the chosen frequency remains stable to within the tracking range of ±400 ppm. (See “Inputs” on page 8 and Table 10). Can accept LVPECL or LVDS or CML inputs given suitable external interface components. Partnered with pin 28. This clock or CLK2 can be automatically or manually selected as the reference clock, see Table 4.
28	CLK1P	I	LVPECL	Input reference clock that the PLL will phase and frequency lock to. Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz or 156.25 MHz and frequencies near to these so long as the chosen frequency remains stable to within the tracking range of ±400 ppm. (See “Inputs” on page 8 and Table 10). Can accept LVPECL or LVDS or CML inputs given suitable external interface components. Partnered with pin 27. This clock or CLK2 can be automatically or manually selected as the reference clock, see Table 4.
30	CLK2N	I	LVPECL	Second Input reference clock that the PLL will phase and frequency lock to. Input reference clock that the PLL will phase and frequency lock to. Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz or 156.25 MHz, and frequencies near to these so long as the chosen frequency remains stable to within the tracking range of ±400 ppm. (See “Inputs” on page 8 and Table 10). Can accept LVPECL or LVDS or CML inputs given suitable external interface components. Partnered with pin 31. This clock or CLK1 can be automatically or manually selected as the reference clock, see Table 4.
31	CLK2P	I	LVPECL	Second Input reference clock that the PLL will phase and frequency lock to. Input reference clock that the PLL will phase and frequency lock to. Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz or 156.25 MHz, and frequencies near to these so long as the chosen frequency remains stable to within the tracking range of ±400 ppm. (See “Inputs” on page 8 and Table 10). Can accept LVPECL or LVDS or CML inputs given suitable external interface components. Partnered with pin 30. This clock or CLK2 can be automatically or manually selected as the reference clock, see Table 4.
32	SEL_CLK2	I	LVTTL/ $LVCMOS_D$	Used in combination with pin 33, AUTO_SEL, either to select the CLK2 clock (high) or CLK1 clock (low) in manual control mode, or to select automatic switching mode, as described in Table 4.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
33	AUTO_SEL	I	LVTTL/ $LVCMOS_D$	Used in combination with pin 32, SEL_CLK2, to select automatic switching mode, as described in Table 4.
35	VCP	A	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output up to a level of 210 µA.
36	VCN	A	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output up to a level of 210 µA.
40	RESETB	I	LVTTL/ $LVCMOS^U$ Schmitt Trigger	Active low reset signal with pull up and Schmitt type input. Used to apply an active-low Power-on Reset (POR) signal during system initialization. Should be connected via a capacitor to ground.
41	SYNCP	I	LVPECL	Additional differential input (2 kHz or 8 kHz) where the Sync signal on this input is sampled and resynchronized by clock output OUT1. The resynchronization can be configured via CFG_IN4 and CFG_IN5 to be with the rising or falling edge of output OUT1; see Table 12. Will also accept CML or LVDS signal types when used in conjunction with external biasing components as described in Figures 14 to 19.
42	SYNCN	I	LVPECL	Additional differential input (2 kHz or 8 kHz) where the Sync signal on this input is sampled and resynchronized by clock output OUT1. The resynchronization can be configured via CFG_IN4 and CFG_IN5 to be with the rising or falling edge of output OUT1; see Table 12. Will also accept CML or LVDS signal types when used in conjunction with external biasing components as described in Figures 14 to 19.
44	SYNC_OUT	O	LVTTL/ LVCMOS	A sampled and therefore lower jitter and resynchronized version of the SYNC signal selected from the SYNC1 input. The clock selected on OUT1 (see pins 2 and 3) is used to perform the resynchronization. The resynchronization can be configured to be with the rising or falling edge of output OUT1; see Table 12. The maximum output frequency on OUT1 = 77.76 MHz when the Sync function is used.
45	RATE2A	I	LVTTL/ $LVCMOS_D$	Inputs to control the frequency of the signal produced on pins 5 (OUT2P) and 6 (OUT2N). See Table 11.
46	RATE2B	I	LVTTL/ $LVCMOS_D$	Inputs to control the frequency of signal that is produced on pins 5 (OUT2P) and 6 (OUT2N). See Table 11.
47	RATE1A	I	LVTTL/ $LVCMOS_D$	Inputs to control the frequency of signal that is produced on pins 2 (OUT1P) and 3 (OUT1N). See Table 11.
48	RATE1B	I	LVTTL/ $LVCMOS_D$	Inputs to control the frequency of signal that is produced on pins 2 (OUT1P) and 3 (OUT1N). See Table 11.

Note...A= Analog, I = Input, O = Output, P = Power, LVTTL/$LVCMOS^U$ = LVTTL/LVCMOS input with pull-up resistor, LVTTL/$LVCMOS_D$ = LVTTL/LVCMOS input with pull-down resistor.

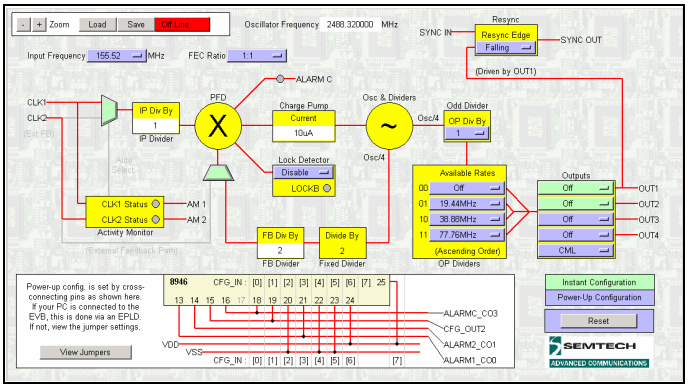
Description

The ACS8946 is a low-jitter integrated PLL for dejittering and clock rate translation, meeting the jitter requirements for SONET up to and including OC-12 (622.08 MHz) systems. It is compliant to the relevant ITU, Telcordia/Bellcore and ETSI standards for at least OC-3 (155.52 MHz) and OC-12 (622.08 MHz) - equivalent to the corresponding STM1 and 4 rates. It may also be used as an initial clock clean-up device in, for example, in OC-48 systems, where the CMU PLL in the Serializer/Framer has a suitable bandwidth.

The ACS8946 can be configured for a range of applications using a minimal number of external components and is available in a small form factor QFN48 package at 7 mm x 7 mm x 0.9 mm outer dimensions.

An evaluation board and GUI software is available on request for hands-on device assessment.

Figure 3 Example EVB GUI Software



Inputs

The ACS8946 has two LVPECL differential inputs (CLK1N/P, pins 27 and 28, and CLK2N/P, pins 30 and 31). These are programmable to accept input frequencies of 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz or 156.25 MHz. Frequencies near to these spot frequencies can also be accepted (see Table 5) so long as the chosen frequency supplied to each input remains stable to within the ±400 ppm tracking range.

LVDS and CML inputs can be accepted given suitable passive resistive and capacitive interface components.

Phase comparisons are performed directly at the selected spot frequency rates in the internal Phase and Frequency Detector (PFD), unless GbE (Gigabit Ethernet) rates are selected for output rates, in which case the input frequencies are divided as required prior to the PFD.

Either clock input may be manually or automatically selected as the reference based on the detection of clock activity at the inputs. The signals AUTO_SEL and SEL_CLK2, shown in Table 4, are used to control the input clock selection. In automatic mode the clock selection between CLK1 and CLK2 is non-revertive, i.e. if the PLL is locked onto CLK1 and CLK1 fails so that the PLL switches over to CLK2, then when CLK1 becomes operational again the PLL will not switch back to CLK1.

Table 4 Input Selection Decoding

AUTO_SEL	SEL_CLK2	Selected Reference	Feedback Clock
0	0	CLK1	Internal Path
0	1	CLK2	Internal Path
1	0	CLK1	CLK2
1	1	AUTOMATIC SELECTION (Activity Monitor determines)	Internal Path

Configuration of expected input clock frequency, which has to be the same for both clock inputs, is set by the wiring of configuration pins described in Table 10.

Unused differential inputs from CLK[2:1]N/P and SYNCN/P should be wired P to GND and N to VDD.

In addition to the main clock inputs CLK1, and CLK2, a single differential SYNC input is provided.

The permitted input frequency range either side of the selected spot frequency depends on the input clock rate. Table 5 presents the list of configurable input spot frequencies, and shows the maximum and minimum range about each input spot frequency that can be allowed as input to the device as a percentage of the configured input spot frequency.

An External Feedback mode is available and may be used for greater control of phase discrepancies for example when using external buffers. In External Feedback mode the external feedback signal is received at the CLK2 input, hence CLK1 can be the only input in this mode.

Outputs

The ACS8946 has four, LVPECL or CML, differential outputs: OUT[4:1]N/P, pins 11/12, 8/9, 5/6, and 2/3. Outputs are produced in a CML or LVPECL output format on up to four outputs concurrently. Interfacing to LVDS is

Table 5 Permitted Input Frequency Range

Selected Input Spot Frequency/ MHz	Selected FEC Ratio (*or Divider Ratio using Odd Divider)	Max and Min Permitted Input Frequency Expressed as a Percentage Above (+%) or Below (-%) the Selected Input Spot Frequency	
		+%	-%
19.44, 38.88 77.76, 155.52	1:1	12.0	3.0
125.00	5:4*	10.0	3.0
156.25	1:1	12.0	3.0

also possible using suitable passive components (see “Input and Output Interface Terminations” on page 27).

Output clock rates at 19.44 MHz, 38.88 MHz, 77.76 MHz, 125.00 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 622.08 MHz or 625.00 MHz are selectable. Additionally, odd number division of these frequencies up to divide-by-15 can also be configured. Note that if odd number division is used, the frequency adjustment factor will apply to all outputs, adjusting all selected output frequencies proportionally.

The output frequency of each output is determined by a combination of the wiring of the configuration pins CFG_IN[7:0] read at power-up, and state of the asynchronously set RATE[2:1]A and RATE[2:1]B pins. The user configures a set of “Available Rates” (four frequencies that are available for selection at every Clock Output) and then configures each output individually to output one of these four rates. OUT1 and OUT2 are asynchronously controllable allowing the output frequency to be switched among the “Available Rates” under control from the rate selection pins (RATE[2:1]A and RATE[2:1]B).

To determine the correct wiring of configuration pins to configure the device involves the use of several look-up tables, and for completeness the datasheet includes all of these, with worked examples (See “Configuration” on page 13). However, to make configuring the device much more simple than this description and look-up tables suggest, Semtech provides a user-friendly Graphical User Interface (GUI) software package to accompany the ACS8946 in which the User enters the required I/O frequencies, dividers settings etc. as required for a particular application, and the GUI responds by displaying the interconnections required to achieve that configuration. Refer to the ACS8946 EVB Document and associated software.

Unused outputs should be left floating with their associated VDD connected to GND. For example, if OUT4 is not required, connect VDD04 to GND and leave OUT4N and OUT4P unconnected.

Clock Multiplication

The ACS8946 provides options to multiply a 19.44 MHz input by 2, 4, 8, 16, or 32 for standard SONET SDH spot frequency configurations. 125.00 MHz dejittered output for Gigabit Ethernet (GbE/10 GbE) is also supported if 125.00 MHz is provided as the input reference, and 156.25 MHz input (for 12.5 GbE) is also supported. These rates are configured by the wiring of CFG_IN[3:2], see Table 10.

If the input frequency used is a percentage away from the configured spot frequency, then the resulting output frequency will change by the same percentage. Refer back to Table 5 for permitted input frequencies.

Note...GbE rates are not directly available as conversions from SONET/SDH rates.

Voltage Controlled Oscillator

The internal VCO operates at 2.48832 GHz when the device is configured for standard SONET/SDH spot frequencies. The VCO frequency is divided down to the selected rate giving a precise 50/50 balanced mark/space ratio for the output. For 125.00 MHz operation the VCO operates at 2.500 GHz.

Jitter Filtering

Input jitter is attenuated by the PLL with the frequency cut-off point (Fc), at which jitter is either tracked or attenuated, defined by the -3 dB point i.e. the position of the first pole of the PLL loop filter. The bandwidth (frequency at which the first pole occurs) is defined by the component value selected for the filter in Tables 6 and 7.

For 19.44 MHz input, using a loop filter bandwidth of 2 kHz and damping factor of 1.2 gives:

- High input jitter attenuation and roll off:
  - - 20 dB/decade from first loop filter pole, (Fc)
  - - 40 dB/decade from 2nd pole (typically 10 x Fc)
- Jitter peaking is less than 1 dB (dependent on the loop filter components)

- Typical final output jitter. e.g. 2.8 ps rms measured over the integration range of 12 kHz -20 MHz offset from carrier.

Jitter Filtering: Partnering with Semtech Line Card Protection Parts

One possible line card solution is to use the ACS8946 on the line card to provide line card protection and direct jitter filtering of references received from a Semtech SETS device (ACS8520/30) on the sync card. If a Semtech LC/P part (ACS8525) is used on the line card, another possible solution uses the ACS8946 after the Semtech LC/P part to dejitter the LC/P device's output.

In the first solution, Master/Slave phase alignment on reference switchover is taken care of by a redundant pair arrangement of SETS devices, which use their output phase alignment features to ensure the ACS8946 is supplied with input clocks that are very closely tied in phase. Then, on a line card reference switch, the ACS8946 acts as a simple MUX adding negligible phase offset between the references, giving very low output disturbance for the combined system, as well as performing its dejittering function.

In the second, more sophisticated solution, the reference switching capability of ACS8946 is not used, as this is carried out by the SETS or LC/P part.

In both cases, the ACS8946 can be used as both an output jitter cleaner, and as a rate converter (19.44 MHz and above).

One "Real World" application for the ACS8946 is to use it to dejitter the 19.44 MHz output from a Semtech ACS8525 LC/P device. In this case it is recommended to set the ACS8946 PLL bandwidth to around 2 kHz to provide a low jitter total solution. The test results detailed in the Electrical Specifications section show the "Real World" performance of this combination of parts which is a superior solution to those traditionally using simple discrete PLLs, and has the following advantages:

- Low overall bandwidth, 18 Hz for example—dictated by the ACS8525.
- High input jitter attenuation and roll-off:
- First, second and third order roll-off points:
  - - 20 dB/decade 18 Hz to 2 kHz,
  - - 40 dB/decade 2 kHz to 200 kHz and
  - - 60 dB/decade for >200 kHz.
- Typical final output jitter, e.g. 2.9 ps rms (measured over the integration range 12 kHz - 20 MHz) dictated by the ACS8946.
- High frequency stability when all input clocks fail; holdover frequency control to Stratum 3—dictated by the ACS8525.

Input Jitter Tolerance

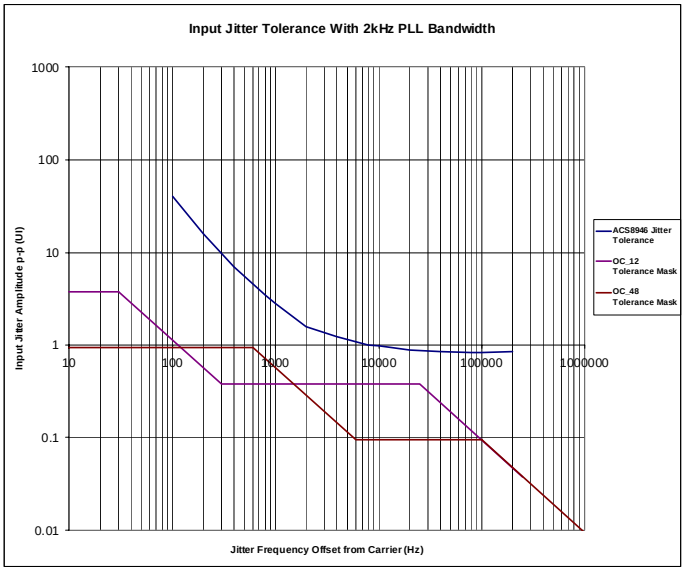
Jitter tolerance is defined as the maximum amplitude of sinusoidal jitter that can exist on the input reference clock above which the device fails to acquire/maintain lock.

For the stand-alone device, the jitter tolerance is shown in Figure 4. for an undivided reference i.e. full rate PFD. For frequencies below the PLL bandwidth, jitter tolerance is seen to decrease at a rate of -20 dB per decade. For jitter frequencies above the PLL bandwidth, jitter tolerance is limited to 0.9 UI p-p.

Note...If the reference clock is divided, then the jitter tolerance will be improved.

When the ACS8946 follows an ACS8525, the input jitter tolerance is wholly defined by the ACS8525. The system jitter tolerance is dramatically increased due to the extended phase capture range of the digital PLL within the ACS8525.

Figure 4 Jitter Tolerance ACS8946

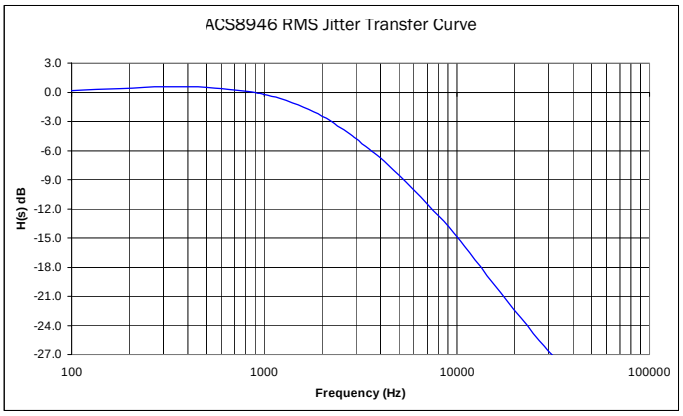


Jitter Transfer

Jitter transfer is a ratio of input jitter present on the reference clock to the filtered jitter present on the output clock. Standalone, the ACS8946 Jitter Transfer

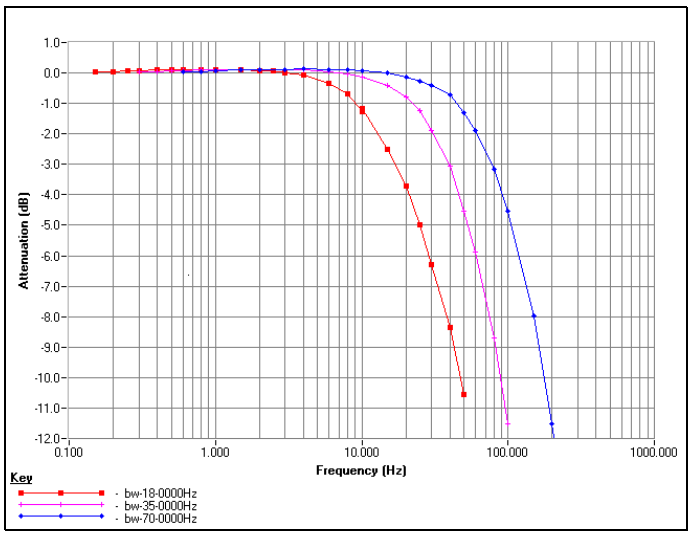
Characteristic is defined solely by the loop filter bandwidth and is shown in Figure 5, which shows the transfer characteristic using the recommended loop filter bandwidth of 2 kHz with a damping factor of 1.2.

Figure 5 Jitter Transfer Characteristic, ACS8946 Stand-alone



In the combined solution, the ACS8525 device provides additional low frequency jitter filtering. The Jitter Transfer Characteristic of the combined ACS8946 and ACS8525 is shown in Figure 6.

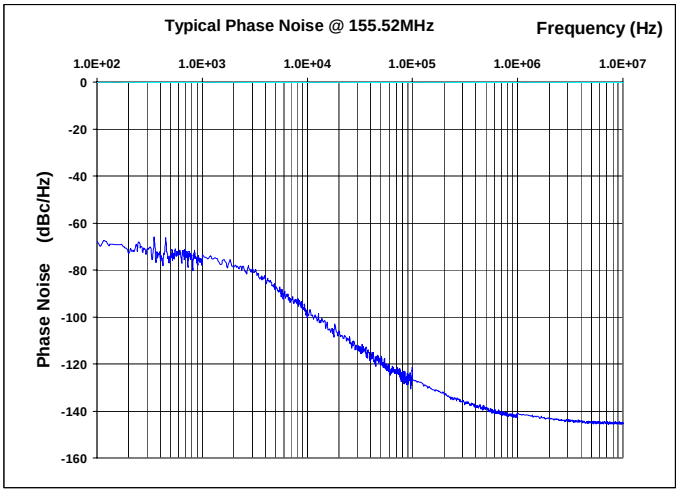
Figure 6 Jitter Transfer Characteristic, ACS8525 and ACS8946 combined



Phase Noise Performance

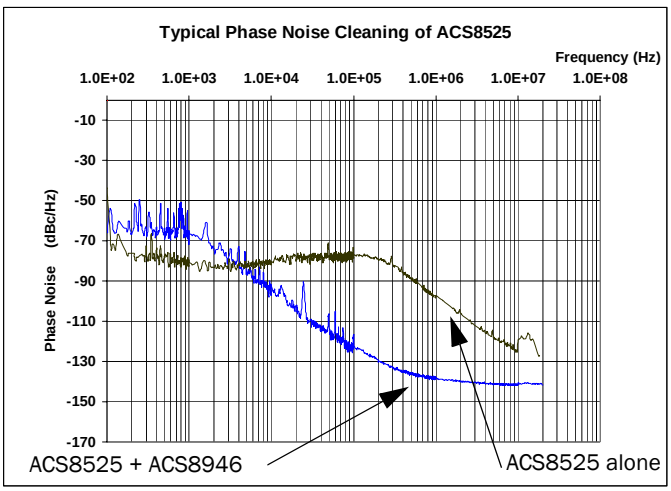
The inherent jitter generation by the ACS8946 is shown in the phase noise plot in Figure 7 measured on a 155.52 MHz output clock using an input reference of 19.44 MHz.

Figure 7 Phase Noise Offset from Carrier of ACS8946 622.08 MHz output clock



In the combined line card solution, the inherent jitter generated by the ACS8525 is attenuated by the ACS8946 as shown in the phase noise plot in Figure 8.

Figure 8 Phase Noise Offset from Carrier, ACS8525 155.52 MHz output clock, with and without ACS8946 Clock Cleaner



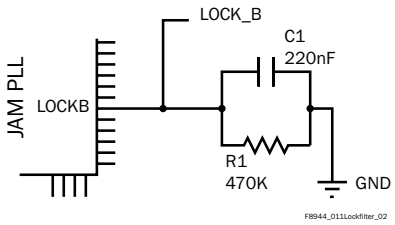
Lock Detector

A simple lock detector is incorporated which combines the plus and minus phase errors from the phase detector,

such that if any phase error signal is present, the LOCKB output drives out a +10 µA current, otherwise it is off.

Consequently this output (LOCKB) is a pulse width modulated (PWM) pulse stream whose mark/space ratio indicates the current input phase error. Filtering this signal with a simple external RC parallel filter as shown in Figure 9 will give a signal whose output level indicates PLL phase and frequency lock.

Figure 9 Lock Filter Components

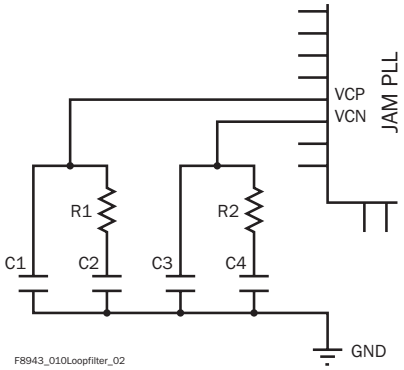


The filtering components are external so that the time to indicate lock or not locked can be optimized for the application. The output indicates both phase and frequency lock. During off-frequency conditions the LOCKB output will be predominately high in its PWM generation with the filtered version giving a constant high state.

PLL Bandwidth Setting

The bandwidth is set by two identical sets of passive RC components that connect to the differential charge pump outputs and internal VCO control inputs. Pins VCN and VCP are the combined differential charge pump outputs and VCO control voltage inputs. Figure 10 shows the arrangement.

Figure 10 Loop Filter Components



All capacitors should be low leakage and low ESR (Equivalent Series Resistance). Tantalum, or ceramic where possible, are suitable. Tables 6 to 9 are based on a damping factor of 1.2 (phase margin 80.2°). Higher damping factors may be used if lower transfer peaking is required. Contact Semtech Sales Support for further details.

RC Components Required to Achieve Bandwidth at Given Input Frequencies (Tables 6 to 9).

Table 6 77.76 MHz or 19.44 MHz Input Frequency

Bandwidth Closed Loop	R1 & R2/ Ω	C2 & C4/ µF	C1 & C3 nF
1500	56	33	200
2000	75	15	100
4000	150	4.7	33
8000	270	0.68	7.5

Table 7 155.52 MHz or 38.88 MHz Input Frequency

Bandwidth Closed Loop	R1 & R2/ Ω	C2 & C4/ µF	C1 & C3 nF
1500*	110	15	91
2000	150	6.8	47
4000	300	2.2	15
8000	560	0.47	3.9

Note... not available at 155.52 MHz input*

Table 8 125 MHz Input Frequency

Bandwidth Closed Loop	R1 & R2/ Ω	C2 & C4/ µF	C1 & C3 nF
1500	68	22	150
2000	91	15	91
4000	180	3.3	20
8000	360	0.68	6.2

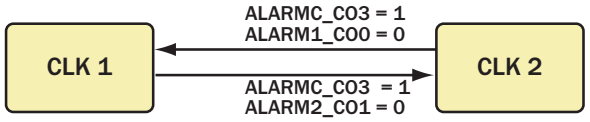
Note...All bandwidths are subject to ± 20% variation due to component tolerancing.

Table 9 156.25 MHz Input Frequency

Bandwidth Closed Loop	R1 & R2/ Ω	C2 & C4/ µF	C1 & C3 µF
2000	75	15	100
4000	150	4.7	33
8000	270	0.68	7.5

Source Switching - State Diagram

Figure 11 Simplified State Diagram of Source Switching



ALARM SIGNALS:
ALARMC_CO3 – Activity alarm for the currently selected clock (from PFD)
ALARM1_CO0 – Activity alarm for CLK1
ALARM2_CO1 – Activity alarm for CLK2

F8946D_012SimpStateDiag_01

The state diagram in Figure 11 shows a simplified view of the automatic switching behavior in the presence of activity alarms. The *ALARMC_CO3* signal from the PFD is used to disqualify a clock, and the signals *ALARM1_CO0* and *ALARM2_CO1* representing no activity on input clocks CLK1 and CLK2 respectively, are used to determine whether or not to select the remaining clock.

Switching between CLK1 and CLK2 is non-revertive.

With *ALARMC_CO3* providing a view of the currently selected clock that is independent to *ALARM1_CO0 and ALARM2_CO1* signals, source selection behavior can be more complex when these alarm signals disagree, and so the state machine is necessarily more complex than the one shown here in order to accommodate such behavior e.g. when a clock signal is disconnected for a very short period of time, or when an input clock is running at the wrong frequency. If further details are required contact Semtech Sales Support.

Configuration

A higher degree of flexibility and programmability is possible via the use of configuration pins on the device. Permanent connections made externally from CFG_IN[7:0] pins to the configuration output pins ALARM1_CO0, ALARM2_CO1, CFG_OUT2, ALARMC_CO3 or to ground or VDD set up the device.

The ACS8946 GUI software presents the configuration information in the most user-friendly manner, though the following tables can be used instead to work out the connectivity required for a particular configuration. For example, the last five columns in Table 10 give the results of the wired connections shown in the second and third columns. E.g., taking the row 7, connecting pin CFG_IN2 to VDD and CFG_IN3 to ALARM2_C01, gives an input frequency of 19.44 MHz, a highest output frequency of 622.08 MHz and configures the outputs as LVPECL.

Output Configuration

The output spot frequency selection for OUT1 is asynchronously controlled by the RATE1A/B select pins (pins 47 and 48), which select one from a set of four “Available Rates” that have been pre-selected at power-up by the wiring configuration of pins 18 and 19 (CFG_IN[1:0]). The wiring configuration of these two pins preselects a set of any four out of seven rates: 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz and disabled, which means that each of the four outputs can run independently at any one of the four pre-selected rates - chosen by the AB value in Table 11 and odd divisions thereof as defined by the start-up configuration of CFG_IN2/CFG_IN3 and/or CFG_IN6/CFG-IN7 respectively).

OUT2 is asynchronously controlled by the RATE2A/B select pins (pins 45 and 46) in the same way as OUT1. Outputs OUT3 and OUT4 cannot be controlled asynchronously; the output frequency selection is controlled at power-up or on reset by a combination of the connections of CFG_IN[1:0] and CFG_IN[5:4] to either VSS, VDD, ALARM1_CO0 (pin 13) or ALARM2_CO1 (pin 14). Given the four Available Rates have been configured as described previously, which one of these four rates is available on OUT3 is then dependent on the connections of the CFG_IN4 and CFG_IN5 pins to either VSS, VDD, ALARM1_CO0 (pin 13) or ALARM2_CO1 (pin 14)—see Table 12.

The method to configure the device is summarized as follows:

- Select the required “Available Rates” that will be made available for selection at all four outputs using CFG_IN[1:0] (See Table 11).
- Define the frequencies of the fixed outputs OUT3/OUT4 using CFG_IN[5:4] (See Table 12) and the required RESYNC Edge result.

- Define/change the frequencies of the dynamically controllable outputs OUT1/OUT2 by driving the RATE[2:1]A/B pins high or low in accordance with the AB pattern for the required frequency as given in Table 11.
- Using CFG_IN[3:2], select the output interface type (CML/LVPECL) for outputs OUT1 and OUT2. (See Table 10).
- Using CFG_IN[7:6], enable/disable LOCKB, select the required output interface type for OUT3/OUT4 and set any odd division. If odd division is not required, set to 1. (See Table 13).

Example Configuration

Decide which set of four output rates is most appropriate for the application and look for the configuration that provides these “Available Rates” in Table 11. E.g. If 77.76 MHz, 38.88 MHz, 19.44 MHz and 0ff are required, then configuration No. 34 in Table 11 will suffice, i.e. connect CFG_IN0 to ALARMC_CO3 and connect CFG_IN1 to CFG_OUT2.

To set OUT3 or OUT4 requires the additional configuration of CFG_IN4 and CFG_IN5 as given by Table 12 (which also configures RESYNC Edge). If OUT4 is required to be set to “Off”, since “Off” has already been defined by previous selection as AB=00 in Table 11, then look up the 00 pattern in Table 12, under “resulting RATE 4[AB]” (giving rows 0 to3 and 16 to 19). Now refine the selection such that OUT 3 provides 19.44 MHz output (AB=01) and a rising RESYNC edge is required - this points to row 17 only, i.e. connect CFG_IN4 to ALARM1_CO0 and connect CFG_IN5 to ALARMC-CO3.

Set each of OUT[2:1] to one of these four Available Rates, as required using the rate selection pins, e.g. to set Output OUT2 to output 38.88 MHz, set RATE2A =1 and RATE2B=0.

To configure an input to the required frequency of 77.76 MHz (and Output technology for OUT 1 and OUT2 only to CML), configure CFG_IN2 to GND and CFG_IN3 to CFG_OUT2 as per row 2 in Table 10.

Table 13 provides the configuration information for using pins CFG_IN[7:6] to configure whether LOCKB is enabled or disabled, the value of the odd divider, and the port interface type for OUT3 and OUT4. For example, assuming LVPECL interface type is required, LOCKB is to be enabled and the output rates (set previously according to Tables 11 and 12) are to be divided by 5 to give “Available Rates” of Off, 3.888 MHz,7.776 MHz, 15.552 MHz, then use the configuration in row 9 of Table 13, i.e. wire CFG_IN6 to VDD and CFG_IN7 to ALARM2_CO1. The corresponding frequency selections made for OUT[4:1] will be divided by 5. The configuration of row 15 would be used if the odd divider is not required (i.e. set to divide-by-1).

Table 10 Input Divider, and OUT 1 and OUT2 Output Interface Type Configurations

Row no.	Wiring of Configuration Pins		Output Application	Required Input Frequency/ MHz	Resulting Highest Available Output Frequency/MHz (when no further division is selected)	Output Interface Type for OUT1 and OUT2
	CFG_IN2	CFG_IN3				
0	GND	ALARM1_CO0	SONET/SDH	155.52	622.08	CML
1	GND	ALARM2_CO1	SONET/SDH	155.52	622.08	LVPECL
2	GND	CFG_OUT2	SONET/SDH	77.76	622.08	CML
3	GND	ALARMC_CO3	SONET/SDH	77.76	622.08	LVPECL
4	VDD	GND	SONET/SDH	38.88	622.08	CML
5	VDD	VDD	SONET/SDH	38.88	622.08	LVPECL
6	VDD	ALARM1_CO0	SONET/SDH	19.44	622.08	CML
7	VDD	ALARM2_CO1	SONET/SDH	19.44	622.08	LVPECL
8(i)	CFG_OUT2	ALARM1_CO0	Ethernet	125.00	625.00	CML

Table 10 Input Divider, and OUT 1 and OUT2 Output Interface Type Configurations (cont...)

Row no.	Wiring of Configuration Pins		Output Application	Required Input Frequency/ MHz	Resulting Highest Available Output Frequency/MHz (when no further division is selected)	Output Interface Type for OUT1 and OUT2
	CFG_IN2	CFG_IN3				
9(i)	CFG_OUT2	ALARM2_CO1	Ethernet	125.00	625.00	LVPECL
10(i)	GND	ALARM1_CO0	Ethernet	156.25	625.00	CML
11(i)	GND	ALARM2_CO1	Ethernet	156.25	625.00	LVPECL

Note: (i) Use odd divider to divide output by 5 to get 125.00 MHz output.
(ii) It is not possible to have 125.00 MHz and 625.00 MHz concurrently on separate outputs.

Table 11 Output Configuration and Selection

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (see note[i])			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
0	GND	GND	622.08	311.04	155.52	77.76
1	GND	VDD	622.08	311.04	155.52	38.88
2	GND	ALARM1_CO0	622.08	311.04	155.52	19.44
3	GND	ALARM2_CO1	622.08	311.04	155.52	Off
4	GND	CFG_OUT2	622.08	311.04	77.76	38.88
5	GND	ALARMC_CO3	622.08	311.04	77.76	19.44
6	VDD	GND	622.08	311.04	77.76	Off
7	VDD	VDD	622.08	311.04	38.88	19.44
8	VDD	ALARM1_CO0	622.08	311.04	38.88	Off
9	VDD	ALARM2_CO1	622.08	311.04	19.44	Off
10	VDD	CFG_OUT2	622.08	155.52	77.76	38.88
11	VDD	ALARMC_CO3	622.08	155.52	77.76	19.44
12	ALARM1_CO0	GND	622.08	155.52	77.76	Off
13	ALARM1_CO0	VDD	622.08	155.52	38.88	19.44
14	ALARM1_CO0	ALARM1_CO0	622.08	155.52	38.88	Off
15	ALARM1_CO0	ALARM2_CO1	622.08	155.52	19.44	Off
16	ALARM1_CO0	CFG_OUT2	622.08	77.76	38.88	19.44
17	ALARM1_CO0	ALARMC_CO3	622.08	77.76	38.88	Off
18	ALARM2_CO1	GND	622.08	77.76	19.44	Off
19	ALARM2_CO1	VDD	622.08	38.88	19.44	Off

Table 11 Output Configuration and Selection (cont...)

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (see note[i])			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
20	ALARM2_CO1	ALARM1_CO0	311.04	155.52	77.76	38.88
21	ALARM2_CO1	ALARM2_CO1	311.04	155.52	77.76	19.44
22	ALARM2_CO1	CFG_OUT2	311.04	155.52	77.76	Off
23	ALARM2_CO1	ALARMC_CO3	311.04	155.52	38.88	19.44
24	CFG_OUT2	GND	311.04	155.52	38.88	Off
25	CFG_OUT2	VDD	311.04	155.52	19.44	Off
26	CFG_OUT2	ALARM1_CO0	311.04	77.76	38.88	19.44
27	CFG_OUT2	ALARM2_CO1	311.04	77.76	38.88	Off
28	CFG_OUT2	CFG_OUT2	311.04	77.76	19.44	Off
29	CFG_OUT2	ALARMC_CO3	311.04	38.88	19.44	Off
30	ALARMC_CO3	GND	155.52	77.76	38.88	19.44
31	ALARMC_CO3	VDD	155.52	77.76	38.88	Off
32	ALARMC_CO3	ALARM1_CO0	155.52	77.76	19.44	Off
33	ALARMC_CO3	ALARM2_CO1	155.52	38.88	19.44	Off
34	ALARMC_CO3	CFG_OUT2	77.76	38.88	19.44	Off

Notes: (i) Use the "Available Rates" columns as follows: Select a row of 4 "Available Rates", then, to assign any one of these four frequencies to a particular output, read off the AB value associated with that frequency and apply this value to the rate selection pins or internal signals for that output, e.g. set as High(1) or Low (0) the signals on pin pairs RATE1A and RATE1B for OUT1, RATE 2A and RATE2B for OUT2, and internal signal pairs RATE3A and RATE3B for OUT3, and RATE4A and RATE4B for OUT4.

(ii) Available Rates shown assume standard SONET rates and no odd dividers.

Table 12 SYNC Edge and Clock Output Configurations

Row No.	Wiring of Configuration Pins		RESYNC Edge Result	Resulting RATE4[AB]		Resulting RATE3[AB]	
	CFG_IN4	CFG_IN5		4A	4B	3A	3B
0	GND	GND	Falling	0	0	0	0
1	GND	VDD	Falling	0	0	0	1
2	GND	ALARM1_CO0	Falling	0	0	1	0
3	GND	ALARM2_CO1	Falling	0	0	1	1
4	GND	CFG_OUT2	Falling	0	1	0	0
5	GND	ALARMC_CO3	Falling	0	1	0	1
6	VDD	GND	Falling	0	1	1	0
7	VDD	VDD	Falling	0	1	1	1

Table 12 SYNC Edge and Clock Output Configurations (cont...)

Row No.	Wiring of Configuration Pins		RESYNC Edge Result	Resulting RATE4[AB]		Resulting RATE3[AB]	
	CFG_IN4	CFG_IN5		4A	4B	3A	3B
8	VDD	ALARM1_CO0	Falling	1	0	0	0
9	VDD	ALARM2_CO1	Falling	1	0	0	1
10	VDD	CFG_OUT2	Falling	1	0	1	0
11	VDD	ALARMC_CO3	Falling	1	0	1	1
12	ALARM1_CO0	GND	Falling	1	1	0	0
13	ALARM1_CO0	VDD	Falling	1	1	0	1
14	ALARM1_CO0	ALARM1_CO0	Falling	1	1	1	0
15	ALARM1_CO0	ALARM2_CO1	Falling	1	1	1	1
16	ALARM1_CO0	CFG_OUT2	Rising	0	0	0	0
17	ALARM1_CO0	ALARMC_CO3	Rising	0	0	0	1
18	ALARM2_CO1	GND	Rising	0	0	1	0
19	ALARM2_CO1	VDD	Rising	0	0	1	1
20	ALARM2_CO1	ALARM1_CO0	Rising	0	1	0	0
21	ALARM2_CO1	ALARM2_CO1	Rising	0	1	0	1
22	ALARM2_CO1	CFG_OUT2	Rising	0	1	1	0
23	ALARM2_CO1	ALARMC_CO3	Rising	0	1	1	1
24	CFG_OUT2	GND	Rising	1	0	0	0
25	CFG_OUT2	VDD	Rising	1	0	0	1
26	CFG_OUT2	ALARM1_CO0	Rising	1	0	1	0
27	CFG_OUT2	ALARM2_CO1	Rising	1	0	1	1
28	CFG_OUT2	CFG_OUT2	Rising	1	1	0	0
29	CFG_OUT2	ALARMC_CO3	Rising	1	1	0	1
30	ALARMC_CO3	GND	Rising	1	1	1	0
31	ALARMC_CO3	VDD	Rising	1	1	1	1

Table 13 LOCKB, Output Technology for OUT3 and OUT4, and Odd Divider Configurations

Row No.	Wiring of Configuration Pins		Output Interface Type for OUT3 and OUT4	LOCKB	Odd Divider
	CFG_IN6	CFG_IN7			
0	GND	GND	LVPECL	Disable	3
1	GND	VDD	LVPECL	Disable	5

Table 13 LOCKB, Output Technology for OUT3 and OUT4, and Odd Divider Configurations (cont...)

Row No.	Wiring of Configuration Pins		Output Interface Type for OUT3 and OUT4	LOCKB	Odd Divider
	CFG_IN6	CFG_IN7			
2	GND	ALARM1_CO0	LVPECL	Disable	7
3	GND	ALARM2_CO1	LVPECL	Disable	9
4	GND	CFG_OUT2	LVPECL	Disable	11
5	GND	ALARMC_CO3	LVPECL	Disable	13
6	VDD	GND	LVPECL	Disable	15
7	VDD	VDD	LVPECL	Disable	1
8	VDD	ALARM1_CO0	LVPECL	Enable	3
9	VDD	ALARM2_CO1	LVPECL	Enable	5
10	VDD	CFG_OUT2	LVPECL	Enable	7
11	VDD	ALARMC_CO3	LVPECL	Enable	9
12	ALARM1_CO0	GND	LVPECL	Enable	11
13	ALARM1_CO0	VDD	LVPECL	Enable	13
14	ALARM1_CO0	ALARM1_CO0	LVPECL	Enable	15
15	ALARM1_CO0	ALARM2_CO1	LVPECL	Enable	1
16	ALARM1_CO0	CFG_OUT2	CML	Disable	3
17	ALARM1_CO0	ALARMC_CO3	CML	Disable	5
18	ALARM2_CO1	GND	CML	Disable	7
19	ALARM2_CO1	VDD	CML	Disable	9
20	ALARM2_CO1	ALARM1_CO0	CML	Disable	11
21	ALARM2_CO1	ALARM2_CO1	CML	Disable	13
22	ALARM2_CO1	CFG_OUT2	CML	Disable	15
23	ALARM2_CO1	ALARMC_CO3	CML	Disable	1
24	CFG_OUT2	GND	CML	Enable	3
25	CFG_OUT2	VDD	CML	Enable	5
26	CFG_OUT2	ALARM1_CO0	CML	Enable	7
27	CFG_OUT2	ALARM2_CO1	CML	Enable	9
28	CFG_OUT2	CFG_OUT2	CML	Enable	11
29	CFG_OUT2	ALARMC_CO3	CML	Enable	13
30	ALARMC_CO3	GND	CML	Enable	15
31	ALARMC_CO3	VDD	CML	Enable	1

Table 14 Output Configuration and Selection for Ethernet Rates (156.25 MHz or 125 MHz input)

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (See Note (l))			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
0	GND	GND	625.00	312.50	156.25	78.13
1	GND	VDD	625.00	312.50	156.25	39.06
2	GND	ALARM1_CO0	625.00	312.50	156.25	19.53
3	GND	ALARM2_CO1	625.00	312.50	156.25	Off
4	GND	CFG_OUT2	625.00	312.50	78.13	39.06
5	GND	ALARMC_CO3	625.00	312.50	78.13	19.53
6	VDD	GND	625.00	312.50	78.13	Off
7	VDD	VDD	625.00	312.50	39.06	19.53
8	VDD	ALARM1_CO0	625.00	312.50	39.06	Off
9	VDD	ALARM2_CO1	625.00	312.50	19.53	Off
10	VDD	CFG_OUT2	625.00	156.25	78.13	39.06
11	VDD	ALARMC_CO3	625.00	156.25	78.13	19.53
12	ALARM1_CO0	GND	625.00	156.25	78.13	Off
13	ALARM1_CO0	VDD	625.00	156.25	39.06	19.53
14	ALARM1_CO0	ALARM1_CO0	625.00	156.25	39.06	Off
15	ALARM1_CO0	ALARM2_CO1	625.00	156.25	19.53	Off
16	ALARM1_CO0	CFG_OUT2	625.00	78.13	39.06	19.53
17	ALARM1_CO0	ALARMC_CO3	625.00	78.13	39.06	Off
18	ALARM2_CO1	GND	625.00	78.13	19.53	Off
19	ALARM2_CO1	VDD	625.00	39.06	19.53	Off
20	ALARM2_CO1	ALARM1_CO0	312.50	156.25	78.13	39.06
21	ALARM2_CO1	ALARM2_CO1	312.50	156.25	78.13	19.53
22	ALARM2_CO1	CFG_OUT2	312.50	156.25	78.13	Off
23	ALARM2_CO1	ALARMC_CO3	312.50	156.25	39.06	19.53
24	CFG_OUT2	GND	312.50	156.25	39.06	Off
25	CFG_OUT2	VDD	312.50	156.25	19.53	Off
26	CFG_OUT2	ALARM1_CO0	312.50	78.13	39.06	19.53
27	CFG_OUT2	ALARM2_CO1	312.50	78.13	39.06	Off
28	CFG_OUT2	CFG_OUT2	312.50	78.13	19.53	Off
29	CFG_OUT2	ALARMC_CO3	312.50	39.06	19.53	Off
30	ALARMC_CO3	GND	156.25	78.13	39.06	19.53

Table 14 Output Configuration and Selection for Ethernet Rates (156.25 MHz or 125 MHz input) (cont...)

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (See Note (i))			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
31	ALARMC_C03	VDD	156.25	78.13	39.06	Off
32	ALARMC_C03	ALARM1_C00	156.25	78.13	19.53	Off
33	ALARMC_C03	ALARM2_C01	156.25	39.06	19.53	Off
34	ALARMC_C03	CFG_OUT2	78.13	39.06	19.53	Off

Note: (i) Odd divider = 1 (see Table 13)

Table 15 Output Configuration and Selection for Ethernet Rates (156.25 MHz or 125 MHz input)

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (See Note (i))			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
0	GND	GND	125.00	62.50	31.25	15.63
1	GND	VDD	125.00	62.50	31.25	7.81
2	GND	ALARM1_C00	125.00	62.50	31.25	3.91
3	GND	ALARM2_C01	125.00	62.50	31.25	Off
4	GND	CFG_OUT2	125.00	62.50	15.63	7.81
5	GND	ALARMC_C03	125.00	62.50	15.63	3.91
6	VDD	GND	125.00	62.50	15.63	Off
7	VDD	VDD	125.00	62.50	7.81	3.91
8	VDD	ALARM1_C00	125.00	62.50	7.81	Off
9	VDD	ALARM2_C01	125.00	62.50	3.91	Off
10	VDD	CFG_OUT2	125.00	31.25	15.63	7.81
11	VDD	ALARMC_C03	125.00	31.25	15.63	3.91
12	ALARM1_C00	GND	125.00	31.25	15.63	Off
13	ALARM1_C00	VDD	125.00	31.25	7.81	3.91
14	ALARM1_C00	ALARM1_C00	125.00	31.25	7.81	Off
15	ALARM1_C00	ALARM2_C01	125.00	31.25	3.91	Off
16	ALARM1_C00	CFG_OUT2	125.00	15.63	7.81	3.91
17	ALARM1_C00	ALARMC_C03	125.00	15.63	7.81	Off
18	ALARM2_C01	GND	125.00	15.63	3.91	Off
19	ALARM2_C01	VDD	125.00	7.81	3.91	Off
20	ALARM2_C01	ALARM1_C00	62.50	31.25	15.63	7.81
21	ALARM2_C01	ALARM2_C01	62.50	31.25	15.63	3.91
22	ALARM2_C01	CFG_OUT2	62.50	31.25	15.63	Off

Table 15 Output Configuration and Selection for Ethernet Rates (156.25 MHz or 125 MHz input) (cont...)

Row no.	Wiring of Configuration Pins		"Available Rates" and Associated "AB" Values (See Note (i))			
	CFG_IN0	CFG_IN1	AB = 11	AB = 10	AB = 01	AB = 00
23	ALARM2_CO1	ALARMC_CO3	62.50	31.25	7.81	3.91
24	CFG_OUT2	GND	62.50	31.25	7.81	Off
25	CFG_OUT2	VDD	62.50	31.25	3.91	Off
26	CFG_OUT2	ALARM1_CO0	62.50	15.63	7.81	3.91
27	CFG_OUT2	ALARM2_CO1	62.50	15.63	7.81	Off
28	CFG_OUT2	CFG_OUT2	62.50	15.63	3.91	Off
29	CFG_OUT2	ALARMC_CO3	62.50	7.81	3.91	Off
30	ALARMC_CO3	GND	31.25	15.63	7.81	3.91
31	ALARMC_CO3	VDD	31.25	15.63	7.81	Off
32	ALARMC_CO3	ALARM1_CO0	31.25	15.63	3.91	Off
33	ALARMC_CO3	ALARM2_CO1	31.25	7.81	3.91	Off
34	ALARMC_CO3	CFG_OUT2	15.63	7.81	3.91	Off

Note: (i) Odd divider = 5 (see Table 13)

Output Jitter

The output jitter meets all requirements of ITU, Telcordia and ETSI standards for SONET rates up to 622.08 MHz (OC-12/STM-4). See the "Electrical Specifications" sections for details on the jitter figures across the different output jitter frequency bands relevant to each specification.

The recommended bandwidth of around 2 kHz is suitable for both meeting the specification on output jitter generation requirements and for filtering out the input jitter from the input clock.

System Reset

After power-up or a system reset via the RESETB (pin 40), the internal control logic waits for the presence of an input signal of approximately the correct frequency (at least 40% of the nominal) and then allows a further settling time of 60 ms before allowing internal frequency tuning, frequency-locking and phase-locking on to the input clock. Consequently reset should be removed only when the input frequency is within 400 ppm of the nominal frequency.

Layout Recommendations

It is highly recommended to use a stable and filtered 3.3 V power supply to the device. A separate filtered power and ground plane is recommended with supply decoupling capacitors of 10 nF and 100 pF utilizing good high frequency chip capacitors (0402 or 0603 format surface-mount package) on each VDD. Good differential signal layout on the input and output lines should be used to ensure matched track impedance and phase. Contact Semtech directly for further layout recommendations.

Applications

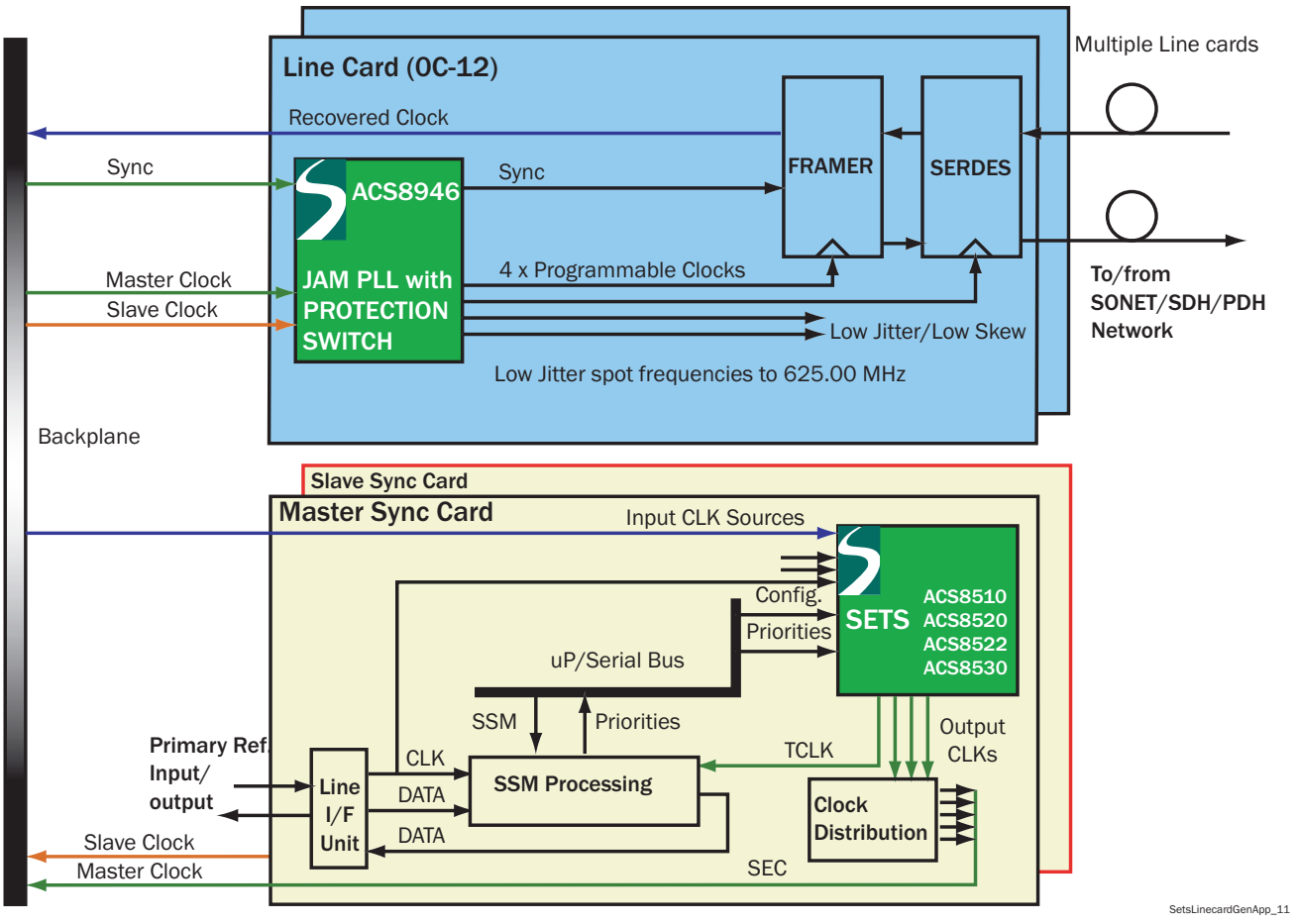
The ACS8946 is targeted at applications requiring clock cleaning, where input jitter is filtered out or attenuated at frequencies above the ACS8946 PLL bandwidth, and at those requiring protection switching. It also performs the function of a clock multiplying unit (CMU) translating from one common spot frequency to one of six spot frequencies (and/or odd divisions thereof) independently on each of its four outputs.

The ACS8946 can save space when compared with discrete analog + VCXO solutions or module-based solutions. In the example in Figure 12 the ACS8946 is shown symbolically as a line card dejittering and clock multiplying device, providing additional jitter cleaning and frequency translation of the output clocks from a Semtech Line Card Protection device.

Figure 13 shows a non-specific example schematic which represents a generic line card design, and demonstrates the I/O connections, configuration controls on the device and the appropriate terminations in different CML/LVPECL technologies, with only the parts relevant to the handling of clocks being shown. This example could be used as a solution for less stringent applications where the ACS8946 could carry out the basic clock protection function in place of a Semtech Line Card Protection device, although it could not, for example, perform group (Clock and Sync) switching, frequency monitoring, or other functions available with members of the Semtech LC/P family of parts.

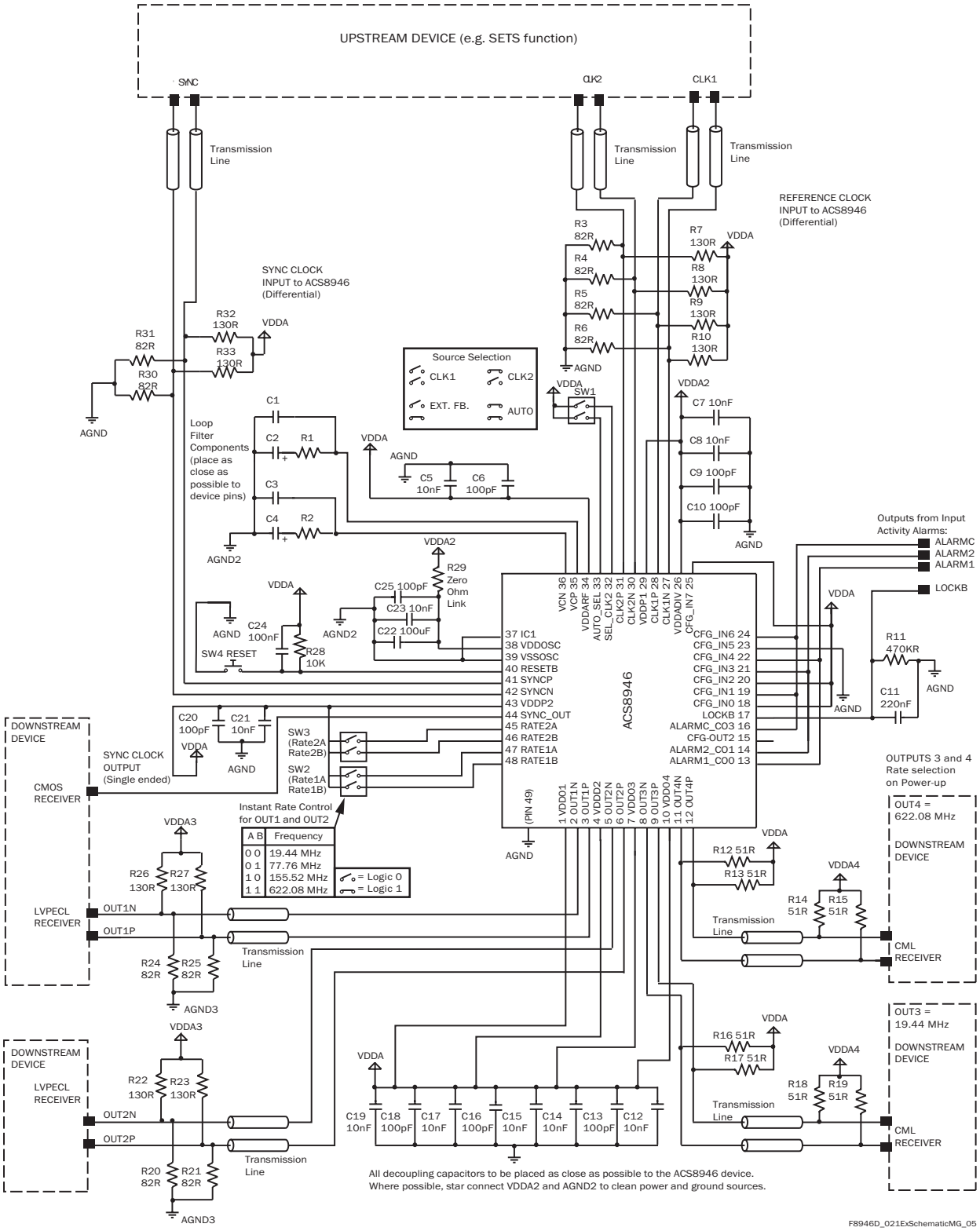
Application Diagram

Figure 12 Typical Application for Semtech JAM PLLs



Example Schematic

Figure 13 Generic Line Card Clock Source with Protection - Example Schematic



Note...For optimal performance use a Low Voltage Dropout (LDO) Regulator to supply VDDA2

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 16, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 16 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage (D.C.): VDD01, VDD02, VDD03, VDD04, VDDP1, VDDP2, VDDADIV, VDDARF, VDDOSC	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins): Digital Inputs: CFG_IN0, CFG_IN1, CFG_IN2, CFG_IN3, CFG_IN4, CFG_IN5, CFG_IN6, CFG_IN7, SELCLK2, AUTO_SEL, RESETB, RATE1A, RATE1B, RATE2A, RATE2B	V_{IN}	-0.5	5.5	V
Input Voltage (non-supply pins) LVPECL Inputs: CLK1N, CLK1P, CLK2N, CLK2P, SYNCN, SYNCP ANALOG I/O: VCN, VCP, LOCKB	V_{IN}	-0.5	V_{DD} + 0.5	V
Output Voltage (non-supply pins): Digital Output: ALARM1_CO1, ALARM2_CO1, CFG_OUT2, ALARMC_CO3, SYNC_OUT LVPECL Outputs: OUT1N, OUT1P, to OUT 4N/P	V_{OUT}	-0.5	V_{DD} + 0.5	V
Ambient Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature	T_{STOR}	-50	+150	°C
Reflow Temperature (Pb)	T_{REPB}	-	+245	°C
Reflow Temperature (Pb Free)	$T_{REPBFREE}$	-	+260	°C
ESD HBM (Human Body Model)[(i), (ii)]	ESD_{HBM}	2	-	kV
Latchup[(iii)]	I_{LU}	±100	-	mA

Notes: (i) All pins pass 2kV HBM except VCN/VCP which are rated at 500 V HBM.

(ii) Tested to JEDEC standard JESD22-A114.

(iii) Tested to JEDEC standard JESD78.

Operating Conditions

Table 17 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage (D.C.): VDDP1, VDDP2, VDDADIV, VDDARF,	V_{DD}	3.135	3.3	3.465	V
Supply Voltage (D.C.): VDDOSC	V_{DDOSC}	3.0	3.3	3.465	V
Supply Voltage (D.C.): VDD01, VDD02, VDD03, VDD04. ** 3.135. V min required to enable output. Supply may be connected to 0 V to disable the associated output.*	V_{DD}	3.135 or 0 V*	3.3	3.465	V
Ambient Temperature Range	T_A	-40	-	+85	°C
Supply Current	I_{DD}	-	330	400	mA
VDDOSC Supply Current	I_{DDOSC}	-	20	25	mA
Device Total Power Dissipation. (All outputs on @625.00 MHz. Excluding power dissipation in external biasing components).	P_{TOT}	-	1145	1390	mW

Thermal Characteristics

Table 18 Thermal Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Thermal Resistance Junction to Ambient	θ_{JA}	-	-	25	°C/W
Operating Junction Temperature	T_{JCT}	-	-	125	°C

AC Characteristics

Table 19 AC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output to Output Skew[(i)]	t_{OSK}	-	-	100	ps
Input to Output Delay	t_{PDIO}	0.5	-	3.0	ns
SYNC_OUT to OUT1 Delay	t_{PDSO}	-2.9	-	-0.4	ns
CLKx to SYNC Set-up	t_{SS}	3.2	-	-	ns
CLKx to SYNC Hold	t_{SH}	2.8	-	-	ns
Input Clock Rise/Fall Time[(ii)] (CLK1, CLK2, SYNC)	t_{CRF}	-	-	10	ns
LVPECL Output Rise/Fall Time[(ii), (iii)]	t_{PECLRF}	-	0.8	1.2	ns
CML Output Rise/Fall Time[(ii), (iv)]	t_{CMLRF}	-	0.7	1.2	ns
SYNC_OUT Rise/Fall Time[(ii), (v)]	t_{SRF}	-	3.0	5.0	ns
Input Clock Duty Cycle (CLK1, CLK2, SYNC)	t_{CDF}	40	50	60	%

Table 19 AC Characteristics (cont...)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Clock Duty Cycle	t_{ODC}	48	50	52	%
RESETB Pulse Width after Power-up	t_{RPW}	100	-	-	ms
Settling Time before Start of Frequency Tuning after RESETB High	t_{FT}	10	-	60	ms

Notes: (i) Outputs running at same frequency.
(ii) Rise/fall time measured 10-90%.
(iii) Using output load specified in Figure 17.
(iv) Using output load specified in Figure 14.
(v) Using 50 Ohm load.

DC Characteristics

Across all operating conditions, unless otherwise stated.

Table 20 DC Characteristics: LVCMOS Input Ports with Internal Pull-down/LVCMOS Schmitt Input Port with Internal Pull-up

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor	R_{PD}	43	-	108	kΩ
Pull-up Resistor (Schmitt Input)	R_{PU}	53	-	113	kΩ
Input Current	I_{IN}	-10	-	+10	µA

Table 21 DC Characteristics: LVPECL Input Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVPECL Input Offset Voltage Differential Inputs (Note (ii))	V_{IO_LVPECL}	V_{DD}-2.0	-	V_{DD}-0.5	V
Input Differential Voltage	V_{ID_LVPECL}	0.1	-	1.4	V
LVPECL Input Low Voltage Single-ended Input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{SS}	-	V_{DD}-1.5	V
LVPECL Input High Voltage Single-ended Input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{DD}-1.3	-	V_{DD}	V
Input High Current Input Differential Voltage V_{ID} = 1.4 V	I_{IH_LVPECL}	-10	-	+10	µA
Input Low Current Input Differential Voltage V_{ID} = 1.4 V	I_{IL_LVPECL}	-10	-	+10	µA

Notes: (i) Unused differential input terminated to VDD-1.4 V.
(ii) Both pins must remain within the supply voltage, i.e. >V_{SS} and <V_{DD}.

Table 22 DC Characteristics: CML Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
I_{OUT} current source	I_{OUT}	13.3	16	19.2	mA
Single-ended output voltage amplitude with 50Ω load to V_{DD} and 50Ω input impedance into next stage.	V_{OS}	-	400	-	mV
Differential output voltage amplitude with 50Ω load to VDD and 50Ω input impedance into next stage on both pins.	V_{OD}	-	800	-	mV

Table 23 DC Characteristics: LVPECL Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVPECL Output Low Voltage (Note (i))	V_{OL_LVPECL}	V_{DD}-2.1	-	V_{DD}-1.62	V
LVPECL Output High Voltage (Note (i))	V_{OH_LVPECL}	V_{DD}-1.45	-	V_{DD}-0.88	V
LVPECL Output Differential Voltage (Note (i))	V_{OD_LVPECL}	0.37	-	1.22	V

Note: (i) With a 50 ohms load on each pin to V_{DD} -2V

Table 24 DC Characteristics: LVTTL/CMOS Output Port

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Low Voltage @ I_{OL} (MAX)	V_{OL}	-	-	0.4	V
Output High Voltage @ I_{OH} (MIN)	V_{OH}	2.4	-	-	V
Low Level Output Current @ V_{OL} = 0.4 V	I_{OL}	2	-	-	mA
High Level Output Current @ V_{OH} = 2.4 V	I_{OH}	2	-	-	mA

Input and Output Interface Terminations

Interfacing to either the same type or electrically different interface types is illustrated by the following circuit diagrams in Figures 14 to 19.

In applications where the output clocks are always running, they may be A.C. coupled, allowing the receive end to be at any common mode voltage, however, the lines must always be terminated at their characteristic impedance.

The preferred termination for the CML type output is 50 Ω to VDD, as shown in Figure 14. A.C. coupling may be used subsequently to translate the levels to other interface types, e.g. to LVPECL/LVDS as shown in Figure 15.

The example of Figure 17 shows LVPECL to LVPECL terminations with D.C. coupling, so that the ACS8946 sees an equivalent load of around 50 Ω from the resistor arrangement at the receiver end. Note that signal levels given in the accompanying graph are nominal levels at 622.08 MHz, and will change with load.

The preferred termination circuitry for the LVDS signals between the ACS8525/26/27 and the ACS8946 LVPECL is shown in Figure 19. The bias for the LVPECL input is set for A.C. inputs at a mid point of approximately 2 V (with a 3.3 V VDD), as opposed to a normal D.C. coupled bias of VDD - 2 V. This is due to the push-pull nature of an A.C. coupled signal.

Note: Where inputs to the ACS8946 are AC coupled, problems may be experienced with activity detection. This is due to noise/cross-talk on the inputs being interpreted as activity. To avoid this, DC couple wherever possible and if AC coupling must be used, consider offsetting the DC bias of the N and P signals, see Figure 16.

Figure 14 CML Output - DC Coupled to CML Receiver

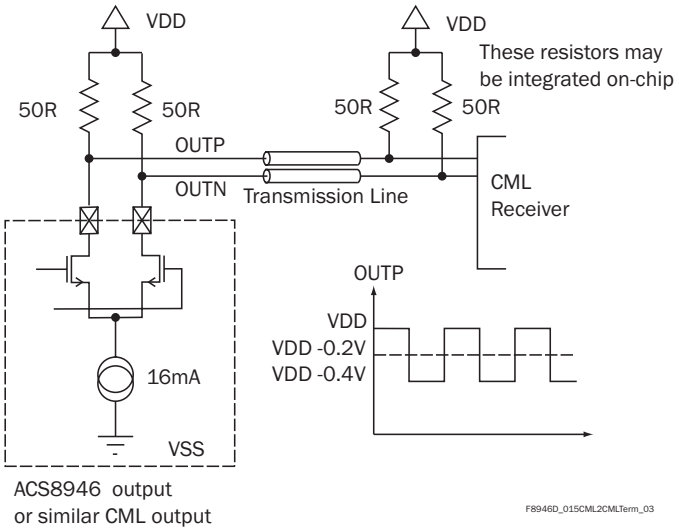


Figure 15 JAM PLL CML Output DC coupled to LVPECL or LVDS Receiver

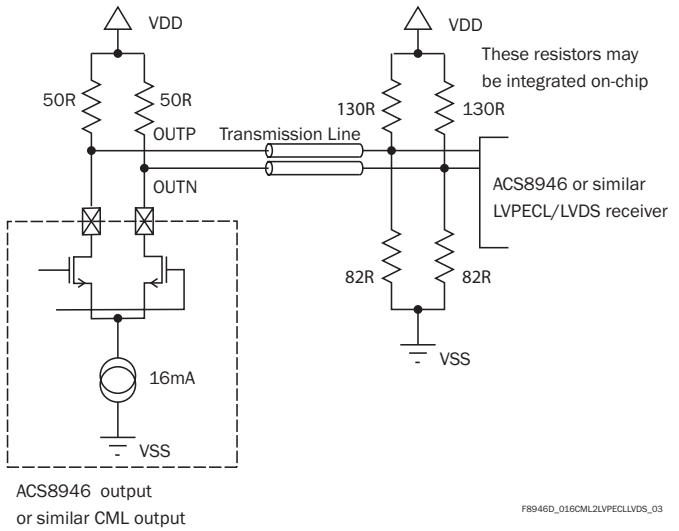
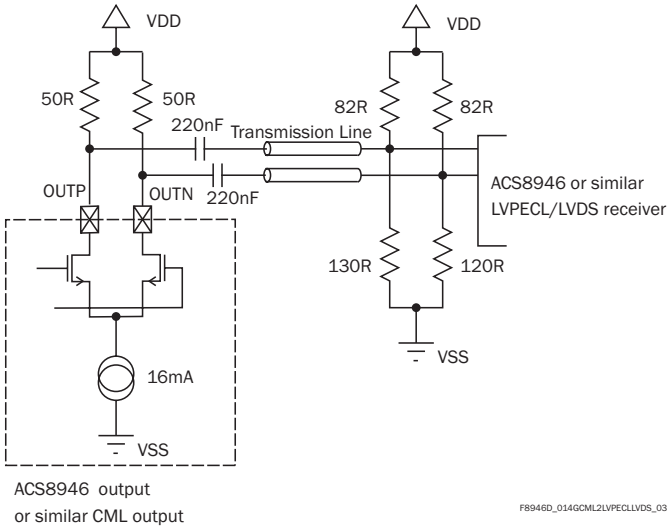


Figure 16 Generic CML Output AC Coupled to LVPECL Receiver



130/120R mismatch is used in the input bias network in Figure 16 to emulate a simplified differential Schmitt trigger, reducing the susceptibility to input noise when no input is connected.

Figure 17 LVPECL Output - DC Coupled to LVPECL or LVDS Receiver

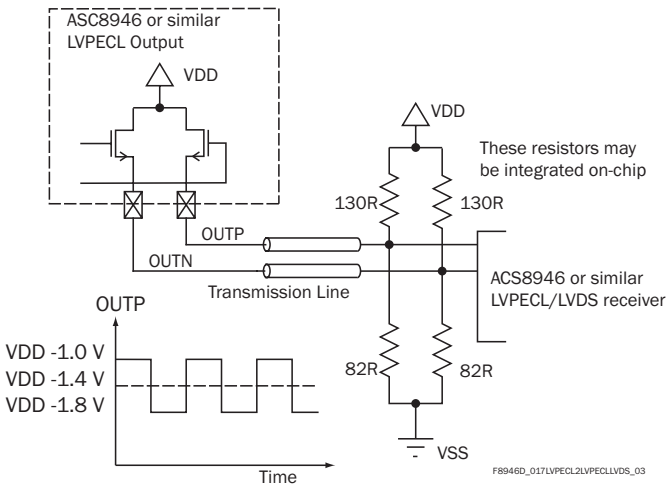


Figure 18 SETS LVDS Output - DC Coupled to LVPECL Receiver

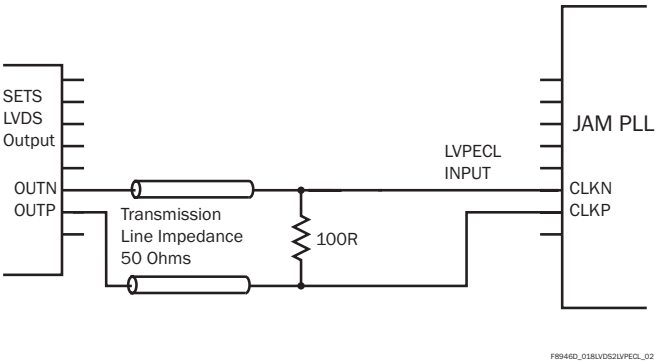
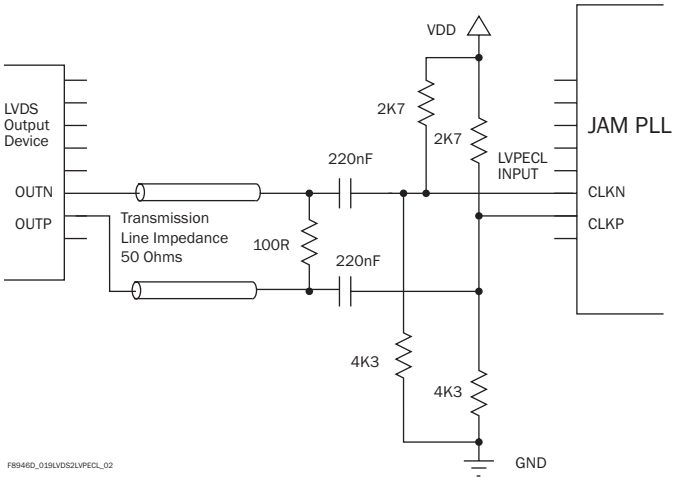


Figure 19 Generic LVDS - AC Coupled to LVPECL Receiver



Note...Activity monitors will not function with this scheme as noise may cause activity detection by mistake. Consider replacing one 4K3 resistor with a 4k7 resistor.

Jitter Performance

Table 25 Output Jitter Generation: ACS8946 Stand-alone @155.52 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.1	12.5	ps p-p
			-	0.5	1.2	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 110.4	302.8	ps p-p
			-	11.0	30.3	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.2	5.3	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 82.4	213.0	ps p-p
			-	8.2	21.3	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.3	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 33.7	90.3	ps p-p
			-	3.4	9.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.1	12.5	ps p-p
			-	0.5	1.2	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 18.1	52.4	ps p-p
			-	1.8	5.2	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 18.2	47.9	ps p-p
			-	1.8	4.8	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 18.4	48.4	ps p-p
				1.8	4.8	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 18.1	52.4	ps p-p
			0.01 UI rms = 64.3 ps	1.8	5.2	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 18.2	47.9	ps p-p
			0.01 UI p-p = 16.1 ps	1.8	4.8	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 33.7	90.3	ps p-p
			-	3.4	9.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.3	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8946 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications

Table 26 Output Jitter Generation: ACS8946 Stand-alone @77.76 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.1	12.3	ps p-p
			-	0.5	1.2	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 102.6	281.3	ps p-p
			-	10.3	28.1	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.2	5.4	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 76.6	197.8	ps p-p
			-	7.7	19.8	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 32.7	87.5	ps p-p
			-	3.3	8.7	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.1	12.3	ps p-p
			-	0.5	1.2	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 17.5	50.8	ps p-p
			-	1.7	5.1	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 17.6	46.4	ps p-p
			-	1.8	4.6	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 17.8	46.9	ps p-p
				1.8	4.7	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 17.5	50.8	ps p-p
			0.01 UI rms = 64.3 ps	1.7	5.1	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 17.6	46.4	ps p-p
			0.01 UI p-p = 16.1 ps	1.8	4.6	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 32.7	87.5	ps p-p
			-	3.3	8.7	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8946 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

Table 27 Output Jitter Generation: ACS8946 Stand-alone @38.88 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.3	12.9	ps p-p
			-	0.5	1.3	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 111.1	304.7	ps p-p
			-	11.1	30.5	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.3	5.4	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 86.9	224.5	ps p-p
			-	8.7	22.4	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 33.7	100.0	ps p-p
			-	3.7	10.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.3	12.9	ps p-p
			-	0.5	1.3	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 19.3	56.1	ps p-p
			-	1.9	5.6	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 19.5	51.2	ps p-p
			-	1.9	5.1	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 19.6	51.7	ps p-p
				2.0	5.2	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 19.3	56.1	ps p-p
			0.01 UI rms = 64.3 ps	1.9	5.6	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 19.5	51.2	ps p-p
			0.01 UI p-p = 16.1 ps	1.9	5.1	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 37.3	100.0	ps p-p
			-	3.7	10.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8946 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

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Table 28 Output Jitter Generation: ACS8946 Stand-alone @19.44 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 6.6	16.0	ps p-p
			-	0.7	1.6	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 137.1	376.0	ps p-p
			-	13.7	37.6	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.4	5.6	ps p-p
			-	0.3	0.6	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 117.5	303.5	ps p-p
			-	11.7	30.3	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 55.9	149.6	ps p-p
			-	5.6	15.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 6.6	16.0	ps p-p
			-	0.7	1.6	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 27.8	80.6	ps p-p
			-	2.8	8.1	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 27.9	73.3	ps p-p
			-	2.8	7.3	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 28.0	73.6	ps p-p
				2.8	7.4	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 27.8	80.6	ps p-p
			0.01 UI rms = 64.3 ps	2.8	8.1	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 27.9	73.3	ps p-p
			0.01 UI p-p = 16.1 ps	2.8	7.3	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 55.9	149.6	ps p-p
			-	5.6	15.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8946 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

Table 29 Output Jitter Generation: ACS8946 Stand-alone @125 MHz Input/156.25 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 4.9	11.8	ps p-p
			-	0.5	1.2	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 81.5	223.6	ps p-p
			-	8.2	22.4	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.2	5.3	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 62.2	160.7	ps p-p
			-	6.2	16.1	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 28.9	77.4	ps p-p
			-	2.9	7.7	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 4.9	11.8	ps p-p
			-	0.5	1.2	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 16.0	46.3	ps p-p
			-	1.6	4.6	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 16.1	42.4	ps p-p
			-	1.6	4.2	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 16.3	42.9	ps p-p
				1.6	4.3	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 16.0	46.3	ps p-p
			0.01 UI rms = 64.3 ps	1.6	4.6	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 16.1	42.4	ps p-p
			0.01 UI p-p = 16.1 ps	1.6	4.2	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 28.9	77.4	ps p-p
			-	2.9	7.7	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8946 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

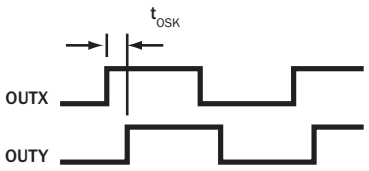
(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

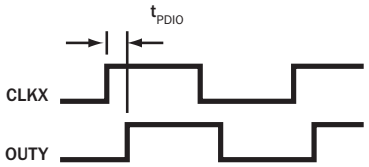
Input/Output Timing

Figure 20 Timing Diagrams

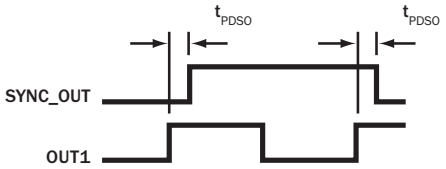
1) Output to Output Clock Skew



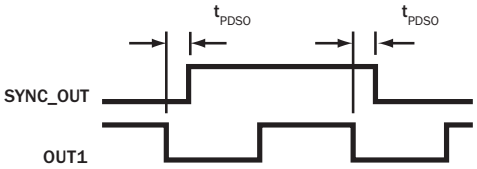
2) Input to Output Delay



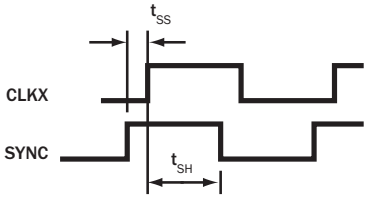
3a) SYNC_OUT to OUT1 Delay (OUT1 Rising Edge Aligned)



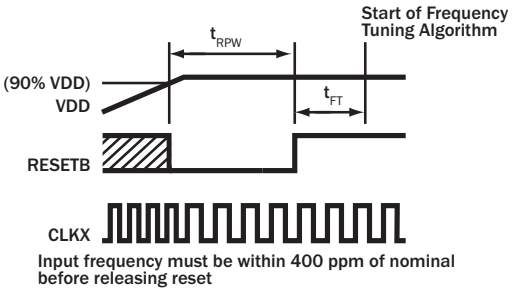
3b) SYNC_OUT to OUT1 Delay (OUT1 Falling Edge Aligned)



4) CLK to SYNC SET UP and HOLD

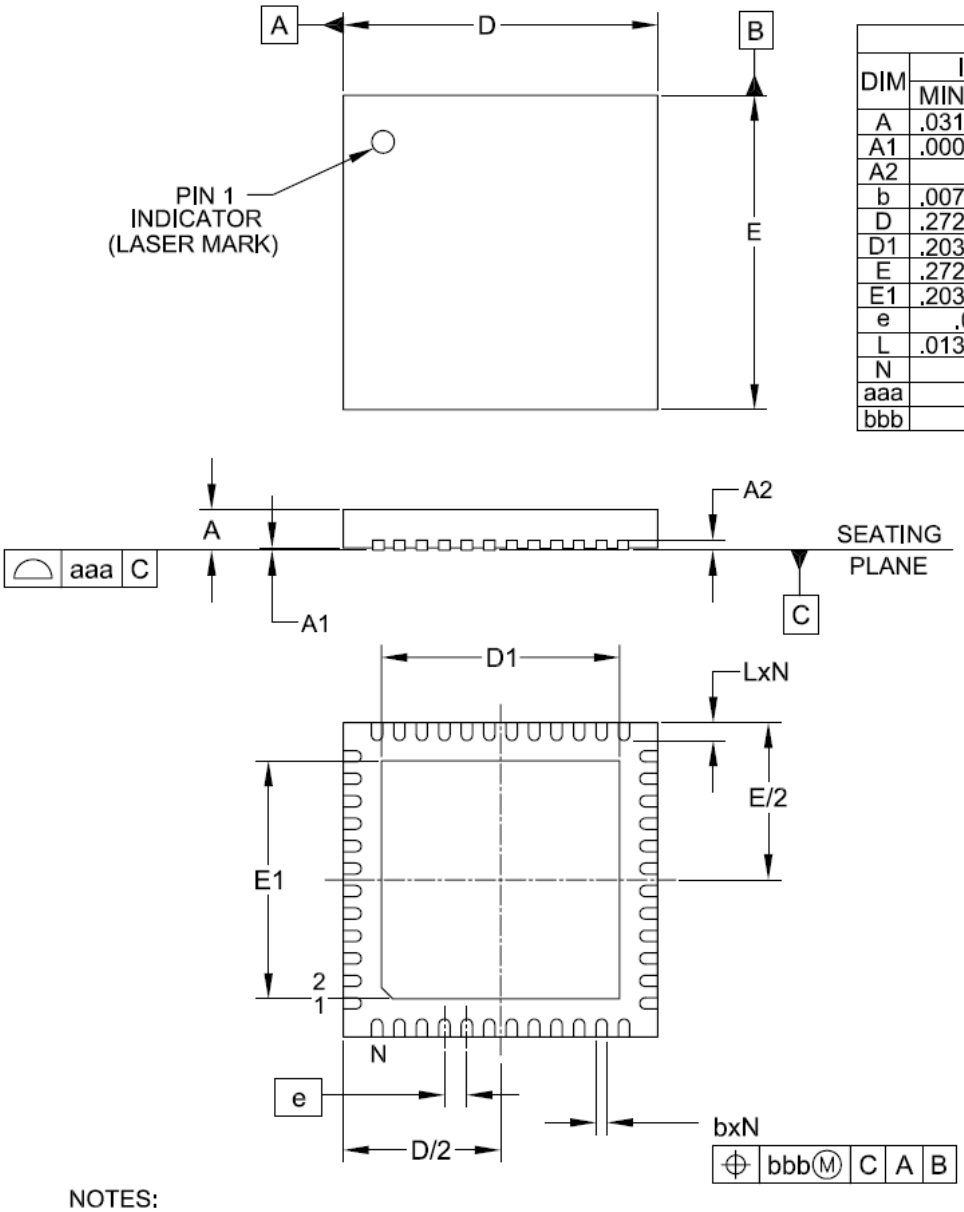


5) Power-up Sequence



Package Information

Figure 21 QFN48 Package.



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2		(.008)			(0.20)	
b	.007	.009	.012	0.18	0.23	0.30
D	.272	.276	.280	6.90	7.00	7.10
D1	.203	.209	.213	5.15	5.30	5.40
E	.272	.276	.280	6.90	7.00	7.10
E1	.203	.209	.213	5.15	5.30	5.40
e		.020 BSC			0.50 BSC	
L	.013	.016	.018	0.35	0.40	0.45
N		48			48	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

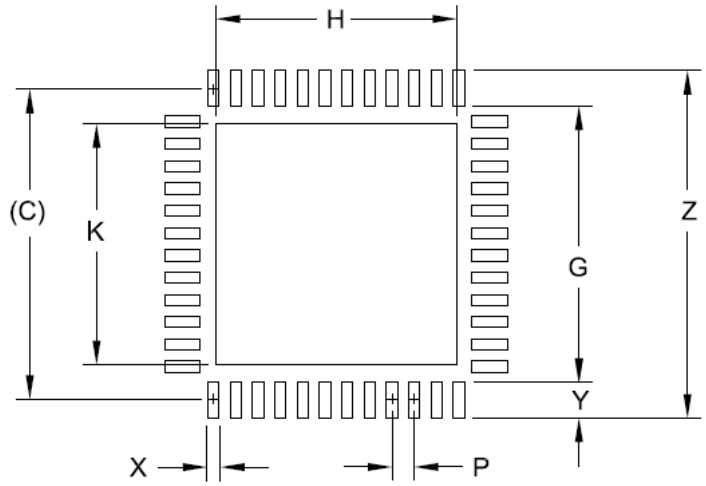
Thermal Conditions

The device is rated for full temperature range when this package is used with a 4-layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

As the device includes a large thermal die paddle ground connection which must be soldered to the PCB in addition to the pins, giving improved pull-off strength and thermal dissipation characteristics as well as the necessary grounding.

Although not essential for the ACS8946, one technique that may be used to improve heat dissipation from through the large centre pad is to include a thermal landing the same size as the centre pad on the component side of the board (and one on the opposite side of the PCB) connected to analog ground using a number of thermal vias, approximately 0.33 mm diameter. These vias should be completely connected (flooded over) to the thermal landing(s) as well as to internal ground planes if using a multi-layer PCB. 3 x 3 vias pitched at 1.27 mm between via centres would be more than sufficient for the ACS8946 if this method were adopted.

Figure 22 Typical 48 Pin QFN PCB Footprint



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.274)	(6.95)
G	.240	6.10
H	.213	5.40
K	.213	5.40
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.307	7.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Abbreviations

CML	Current Mode Logic
CMU	Clock Multiplier Unit
ESD	Electrostatic Discharge
ESR	Effective Series Resistance
HBM	Human Body Model
I/O	Input - Output
JAM PLL	Jitter Attenuating, Multiplying Phase Locked Loop
GbE	Gigabit Ethernet
JAM PLL	Jitter Attenuating, Multiplying PLL
LC/P	Line Card Protection
LDO	Low Voltage Drop-out
LVDS	Low Voltage Differential Signal
LVPECL	Low Voltage (3.3 V) PECL
OC-3/12/48	Optical Carrier Signal Level 3/12/48 155.52 Mbps/ 622.08 Mbps/ 2.488 Gbps
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
p-p	peak-to-peak
rms	root-mean-square
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
STM-1/4/16	Synchronous Transport Module Levels 1/4/16: 155.52 Mbps/ 622.08 Mbps 2.488 Gbps (SDH)
STS-12/48	Synchronous Transport Signal Level: 12/48, 622.08 Mbps/2.488 Gbps (SONET)
UI	Unit Interval
uP (µP)	Microprocessor
VCO	Voltage Controlled Oscillator
WEEE	Waste Electrical and Electronic Equipment (directive)

References and Related Standards

[1] EN 300 462-7-1 v1.1.2 (06/2001)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 7-1: Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications

[2] ETSI EN 302 084 V1.1.1 (2000-02)
Transmission and Multiplexing (TM); The control of jitter and wander in transport networks

[3] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[4] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[5] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[6] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[7] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[8] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[9] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[10] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

[11] RoHS Directive 2002/95/EC: Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

[12] Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC): Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE)

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Revision Status/History

The Revision Status, as shown in top center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet), within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release of the ACS8946 datasheet. Changes made for this document revision are given below.

Table 30 Revision History

Revision	Reference	Description of Changes
Rev. 0.01/June 2005	All Pages	First draft with outline content ahead of measured data.
Rev. 0.02/July 2005	All Pages	Completely revised.
Rev. 0.03/July 2005	All Pages	Completely revised.
Rev. 1.00/November 2005	All pages	Updated doc to Preliminary to reflect status of device. Minor changes and additions throughout.
Rev. 2.00/February 2006	All pages	Completely revised.
Rev. 3/November 2006	All pages	Completely revised and raised to Final status.

Notes

Ordering Information

Table 31 Parts List

Part Number	Description
ACS8946	JAM PLL Jitter Attenuating, Multiplying Phase Locked Loop, with Protection Switch, for OC-12/STM-4 and GbE.
ACS8946T	Lead (Pb)-free packaged version of ACS8946; RoHS and WEEE compliant.
ACS8946EVB	ACS8946 Evaluation Board.

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech for such use.

Right to change- Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

Contacts

For Additional Information, contact the following:

Semtech Corporation Advanced Communications Products

E-mail: sales@semtech.com acsupport@semtech.com

Internet: http://www.semtech.com

USA: 200 Flynn Road, Camarillo, CA 93012-8790
Tel: +1 805 498 2111, Fax: +1 805 498 3804

FAR EAST: 12F No. 89 Sec. 5, Nanking E. Road, Taipei, 105, TWN, R.O.C.
Tel: +886 2 2748 3380 Fax: +886 2 2748 3390

EUROPE: Semtech Ltd., Units 2 and 3, Park Court, Premier Way,
Abbey Park Industrial Estate, Romsey, Hampshire, SO51 9DN
Tel: +44 (0)1794 527 600 Fax: +44 (0)1794 527 601

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