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# STD10NM65N - STF10NM65N STP10NM65N - STU10NM65N

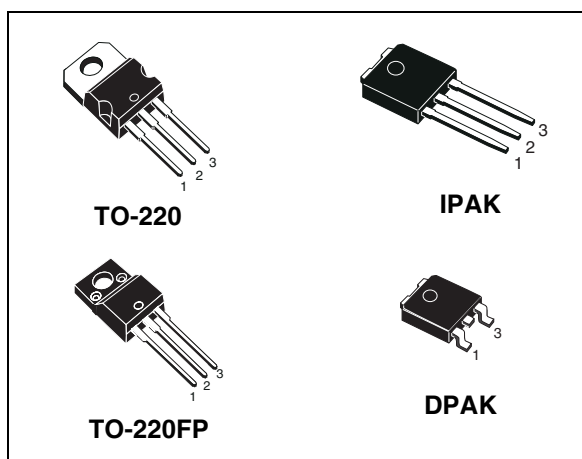
N-channel 650 V, 0.43  $\Omega$ , 9 A MDmesh™ II Power MOSFET  
TO-220, TO-220FP, IPAK, DPAK

## Features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD10NM65N	710 V	< 0.48 $\Omega$	9 A
STF10NM65N	710 V	< 0.48 $\Omega$	9 A <sup>(1)</sup>
STP10NM65N	710 V	< 0.48 $\Omega$	9 A
STU10NM65N	710 V	< 0.48 $\Omega$	9 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



## Application

- Switching applications

## Description

This series of devices implements the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

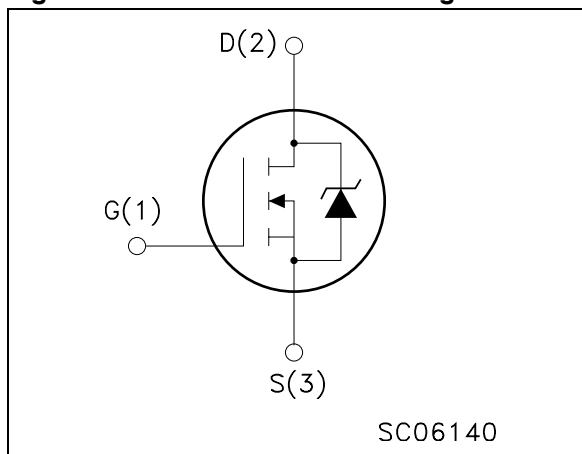


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10NM65N	10NM65N	DPAK	Tape & reel
STF10NM65N	10NM65N	TO-220FP	Tube
STP10NM65N	10NM65N	TO-220	Tube
STU10NM65N	10NM65N	IPAK	Tube

## Contents

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Electrical ratings

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220/IPAK DPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	650		V
$V_{GS}$	Gate-source voltage	$\pm 25$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	$g^{(1)}$	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.7	$5.7^{(1)}$	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36	$36^{(1)}$	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )	--	2500	V
$T_{stg}$	Storage temperature	-55 to 150		$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150		$^\circ\text{C}$

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 9\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	TO-220	IPAK	DPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38			5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	--	50	--	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	100	--	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300				$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	200	mJ

Electrical characteristics

STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N

## 2 Electrical characteristics

(T<sub>CASE</sub>=25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	650			V
dv/dt <sup>(1)</sup>	Drain source voltage slope	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 9 A, V <sub>GS</sub> = 10 V	25			V/ns
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = max rating V <sub>DS</sub> = max rating, @125 °C			1 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		0.43	0.48	Ω

1. Characteristics value at turn off on inductive load

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> =15 V, I <sub>D</sub> = 4.5 A		7.5		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0		850 53 4		pF pF pF
C <sub>oss eq.</sub> <sup>(2)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 520 V		90		pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 9 A, V <sub>GS</sub> = 10 V, <i>(see Figure 19)</i>		25 14 4		nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**
**Electrical characteristics**
**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$ , $I_D = 4.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ <i>(see Figure 18)</i>		12		ns	
$t_r$	Rise time			8		ns	
$t_{d(off)}$	Turn-off delay time				50		ns
$t_f$	Fall time				20		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$I_{SD}$	Source-drain current				9	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				36	A	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9\text{ A}$ , $V_{GS} = 0$			1.3	V	
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ <i>(see Figure 20)</i>		330		ns	
$Q_{rr}$	Reverse recovery charge				3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				19		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ <i>(see Figure 20)</i>		430		ns	
$Q_{rr}$	Reverse recovery charge				4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				19		A

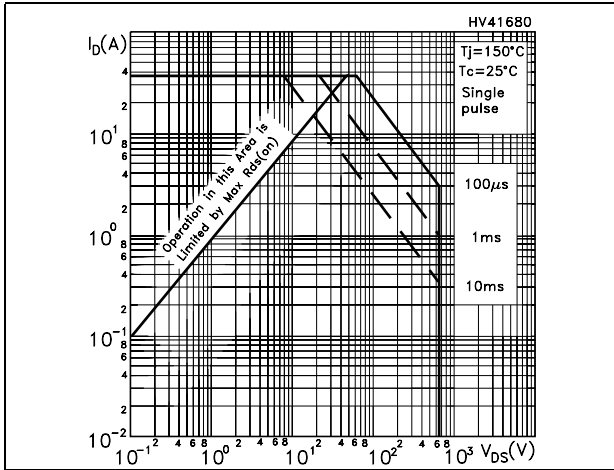
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

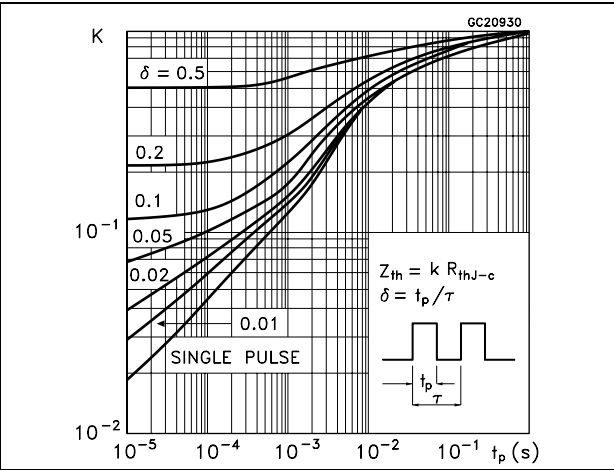
**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

**2.1 Electrical characteristics (curves)**

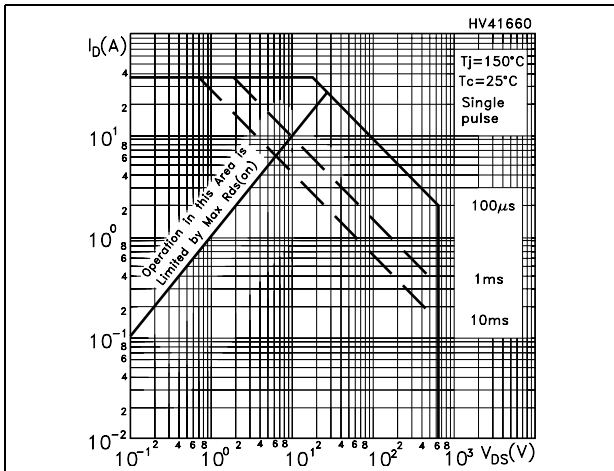
**Figure 2. Safe operating area for TO-220**



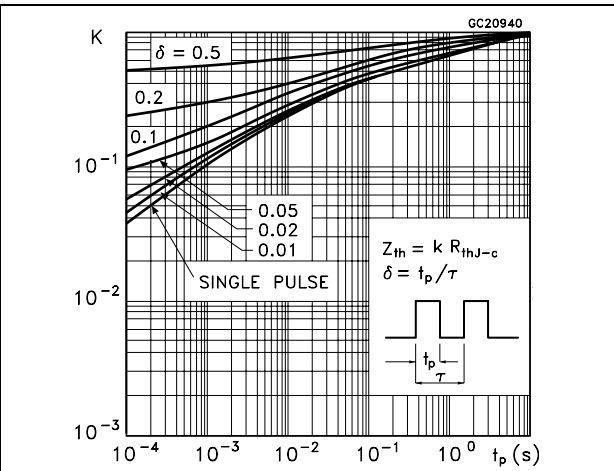
**Figure 3. Thermal impedance for TO-220**



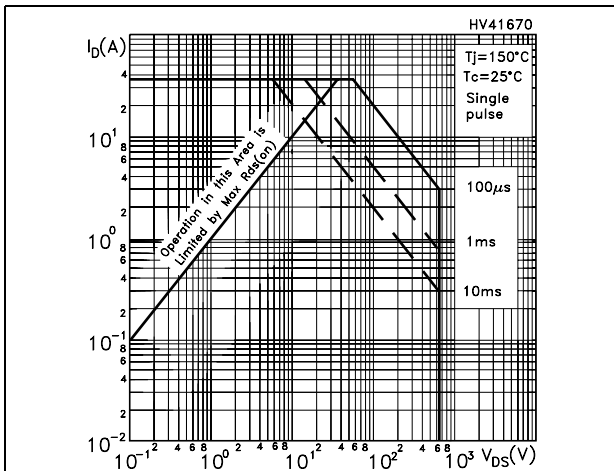
**Figure 4. Safe operating area for TO-220FP**



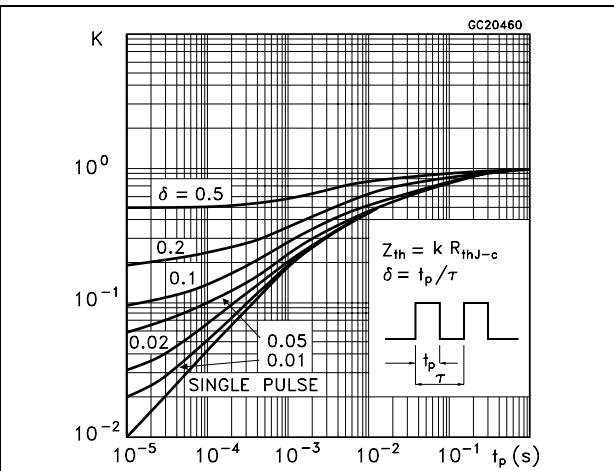
**Figure 5. Thermal impedance for TO-220FP**



**Figure 6. Safe operating area for DPAK/IPAK**



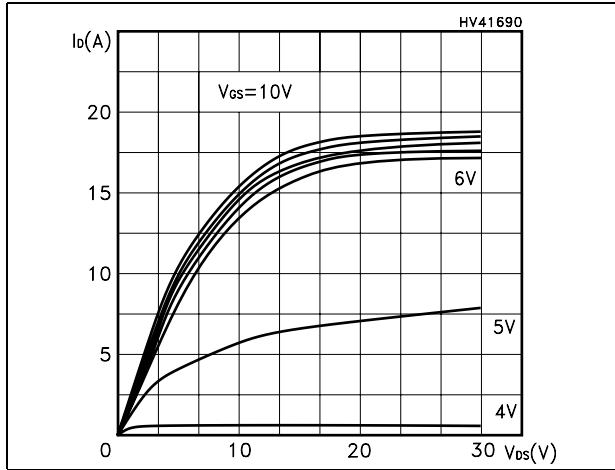
**Figure 7. Thermal impedance for DPAK/IPAK**



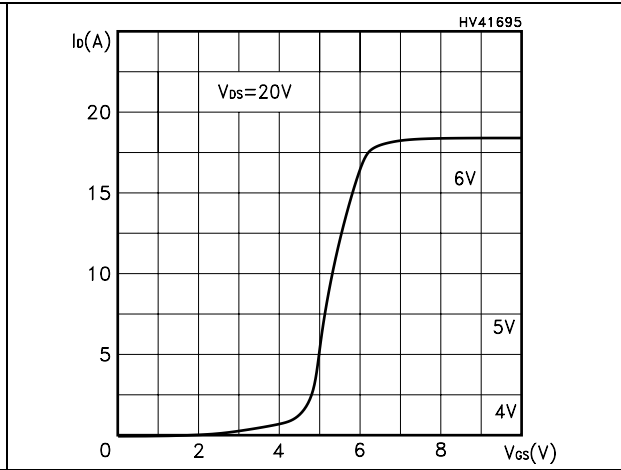
**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

**Electrical characteristics**

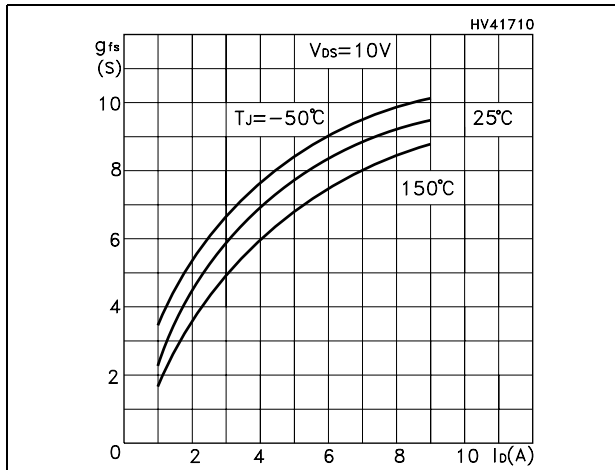
**Figure 8. Output characteristics**



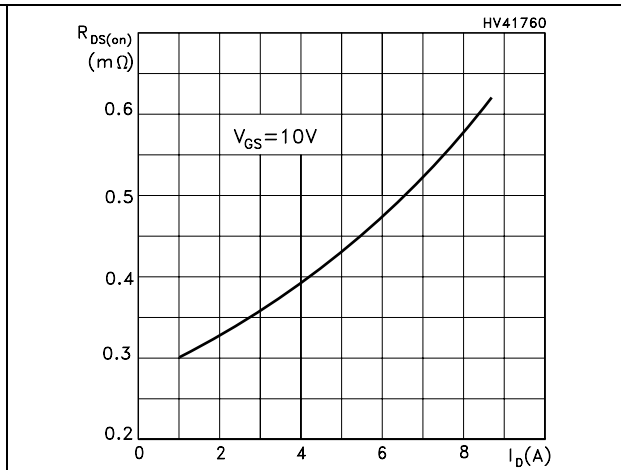
**Figure 9. Transfer characteristics**



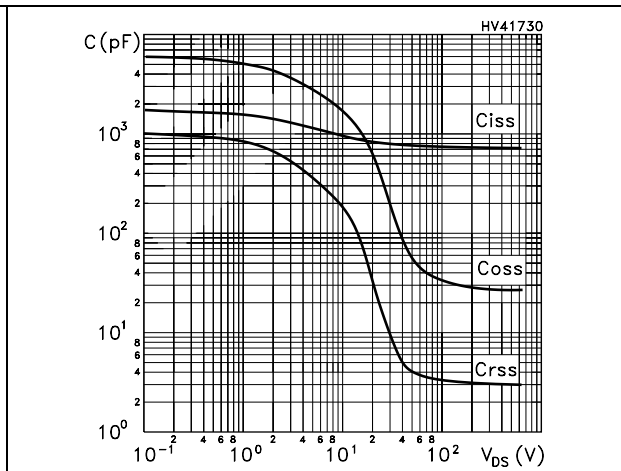
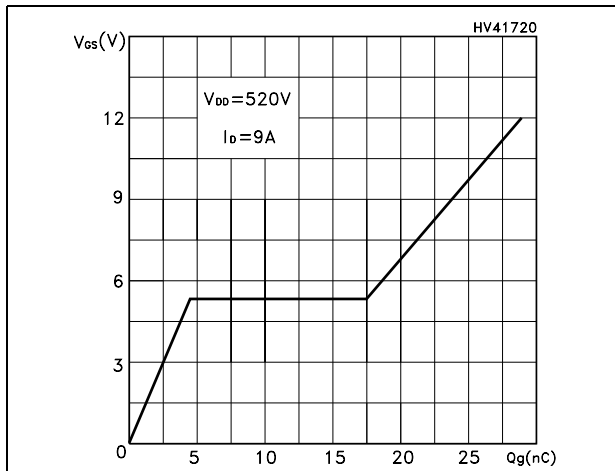
**Figure 10. Transconductance**



**Figure 11. Static drain-source on resistance**



**Figure 12. Gate charge vs gate source voltage** **Figure 13. Capacitance variations**

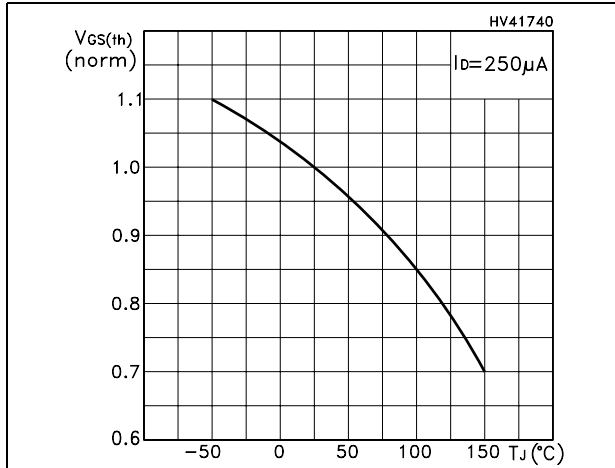




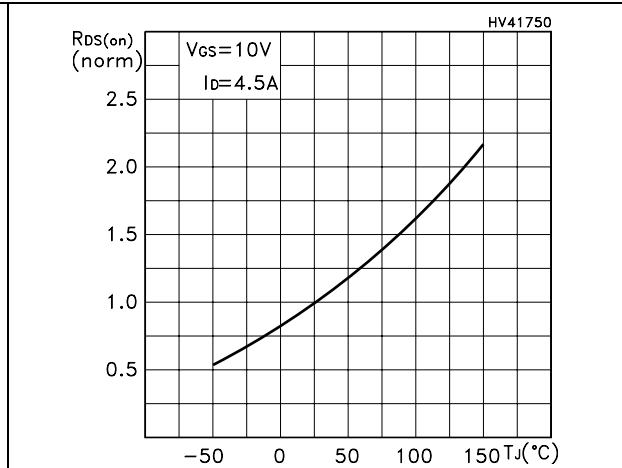
**Electrical characteristics**

**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

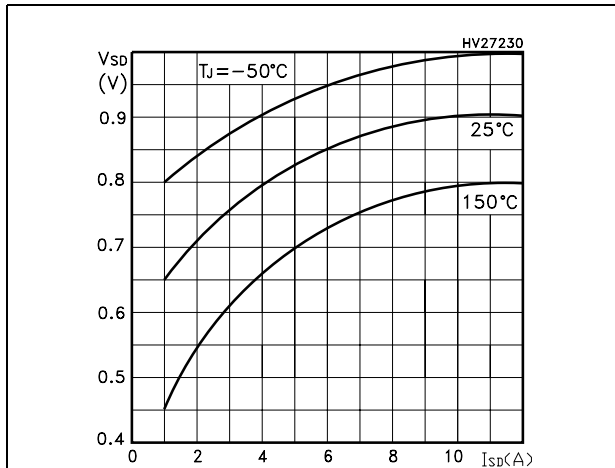
**Figure 14. Normalized gate threshold voltage vs temperature**



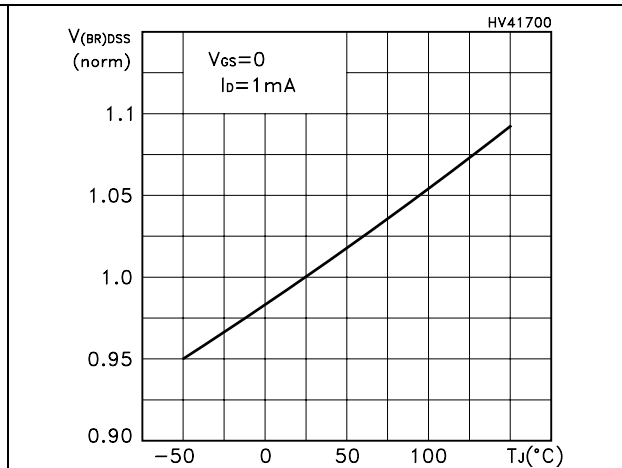
**Figure 15. Normalized on resistance vs temperature**



**Figure 16. Source-drain diode forward characteristics**



**Figure 17. Normalized BV<sub>DSS</sub> vs temperature**

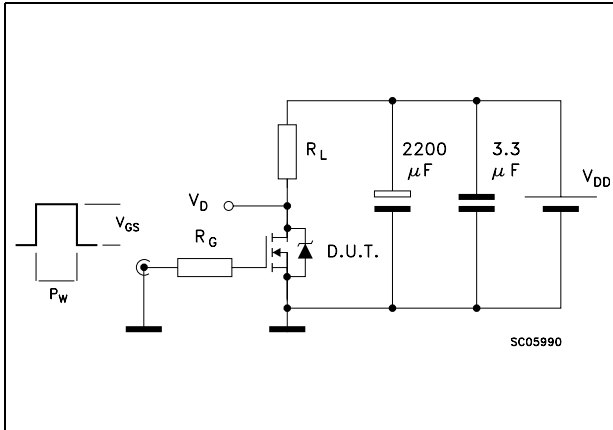


**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

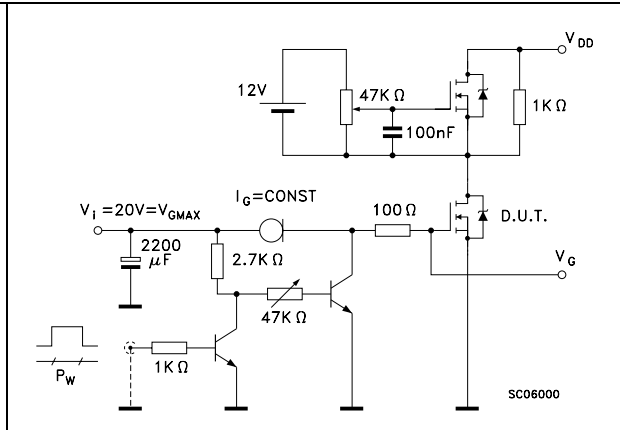
**Test circuit**

**3 Test circuit**

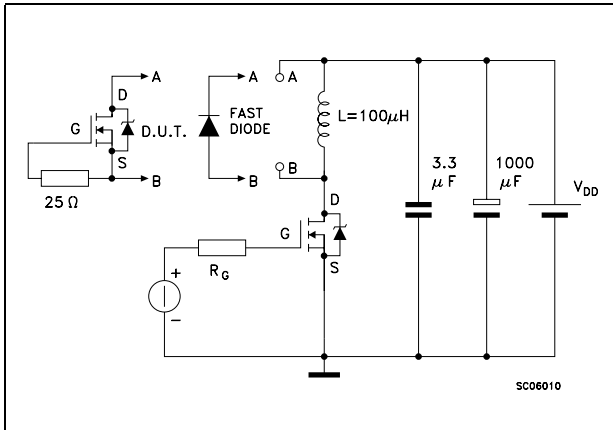
**Figure 18. Switching times test circuit for resistive load**



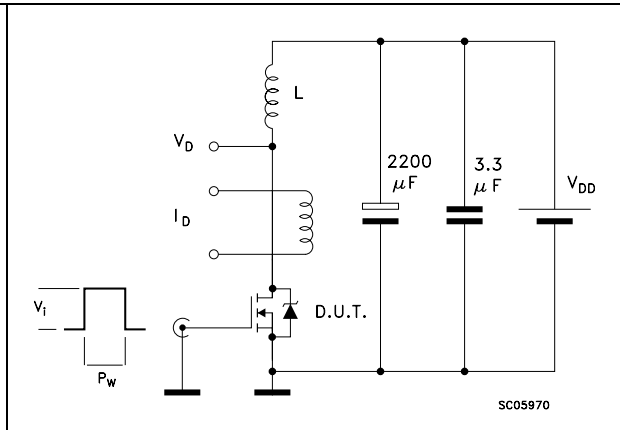
**Figure 19. Gate charge test circuit**



**Figure 20. Test circuit for inductive load switching and diode recovery times**

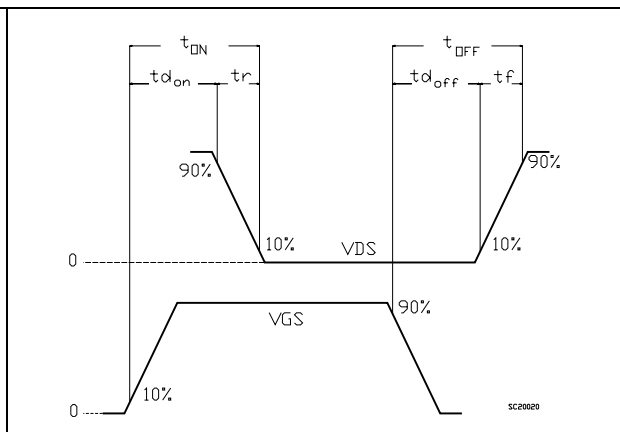
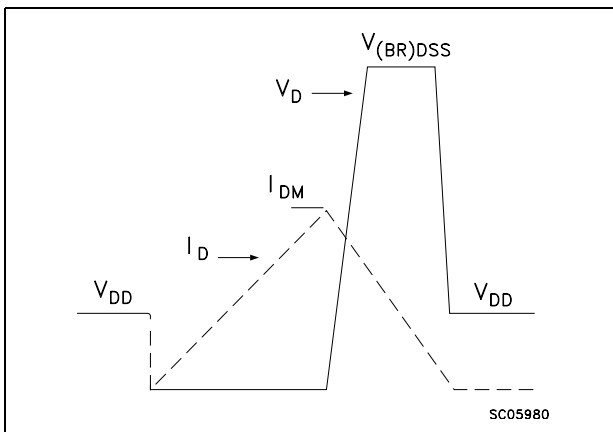


**Figure 21. Unclamped inductive load test circuit**



**Figure 22. Unclamped inductive waveform**

**Figure 23. Switching time waveform**



## 4 Package mechanical data

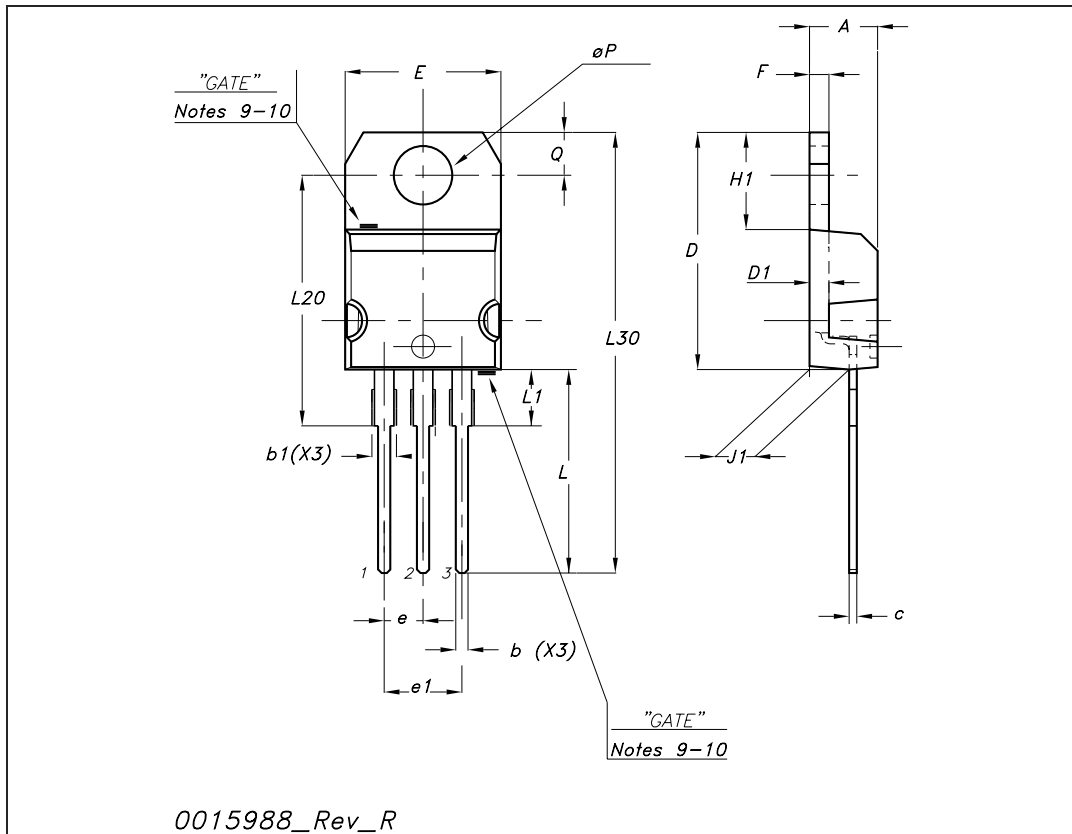
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

**Package mechanical data**

**TO-220 mechanical data**

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

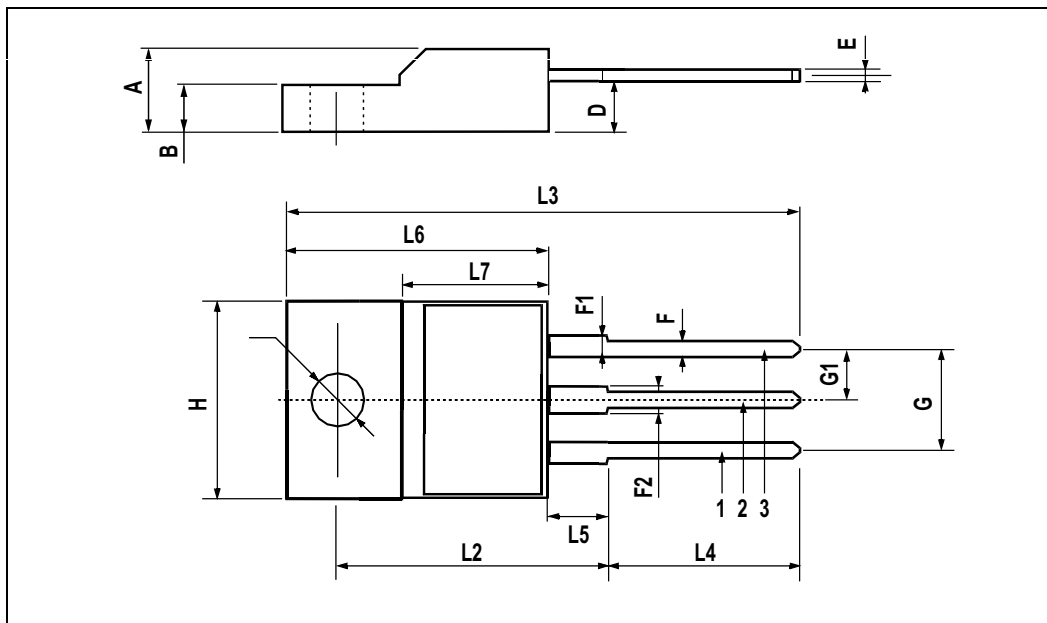


Package mechanical data

STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N

**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

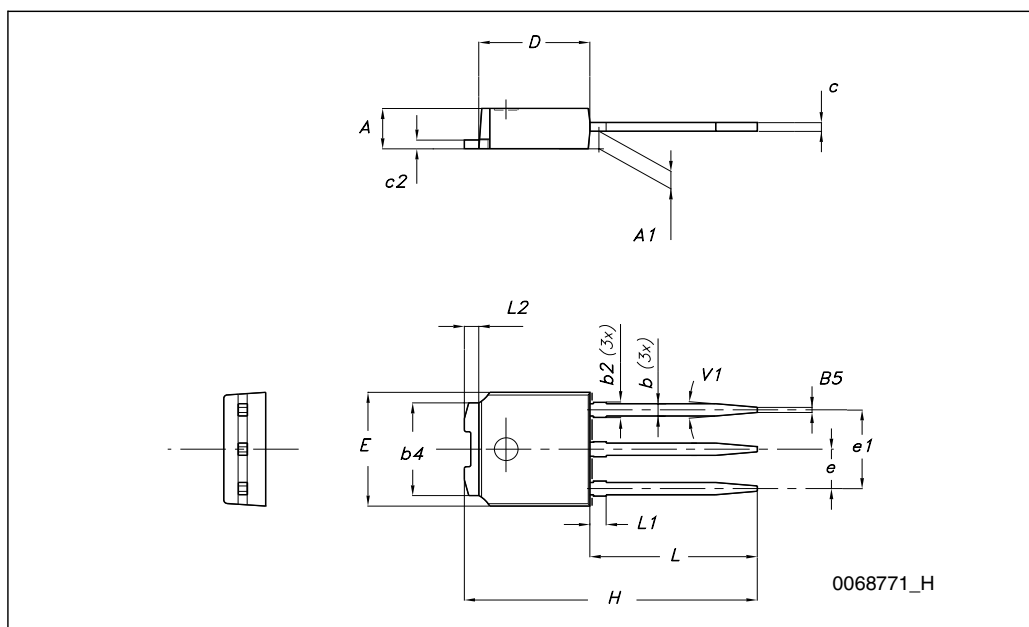


**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

**Package mechanical data**

**TO-251 (IPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	

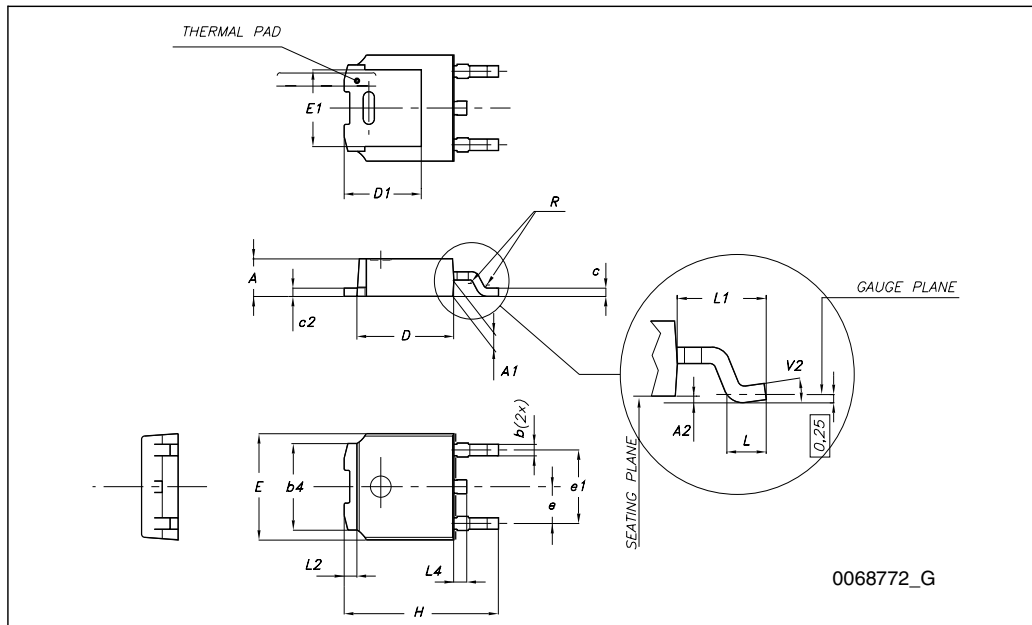


**Package mechanical data**

**STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N**

**TO-252 (DPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

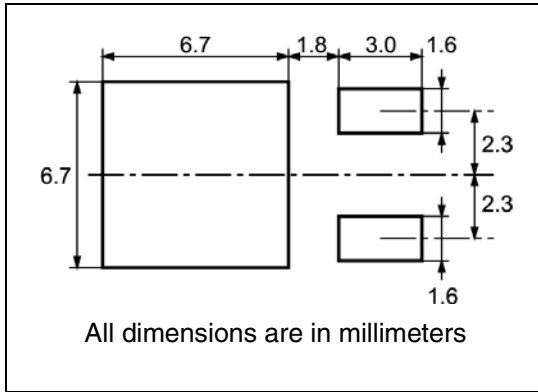


STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N

Package mechanical data

## 5 Package mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start

25mm min. width

For machine ref. only including draft and radii concentric around B<sub>0</sub>

#### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

#### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

FEED DIRECTION

Bending radius R min.



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
26-Oct-2007	1	Initial release.
07-Feb-2008	2	Document status promoted from preliminary data to datasheet.
14-Oct-2008	3	<a href="#">Table 4: Avalanche characteristics</a> has been corrected.

## STD10NM65N - STF10NM65N - STP10NM65N - STU10NM65N

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