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# VND830PEP-E

## Double channel high side driver

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VND830PEP-E	60m $\Omega$ <sup>(1)</sup>	6A <sup>(1)</sup>	36V

1. Per each channel.

- CMOS compatible inputs
- Open drain status outputs
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection (see [Application schematic on page 16](#))
- In compliance with the 2002/95/EC european directive



### Description

The VND830PEP-E is a monolithic device designed in STMicroelectronics VIPower™ M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off-state. Output shorted to  $V_{CC}$  is detected in the off-state. Device automatically turns off in case of ground pin disconnection.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VND830PEP-E	VND830PEPTR-E

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Obsolete Product(s) - Obsolete Product(s)

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Block diagram and pin description

# 1 Block diagram and pin description

Figure 1. Block diagram

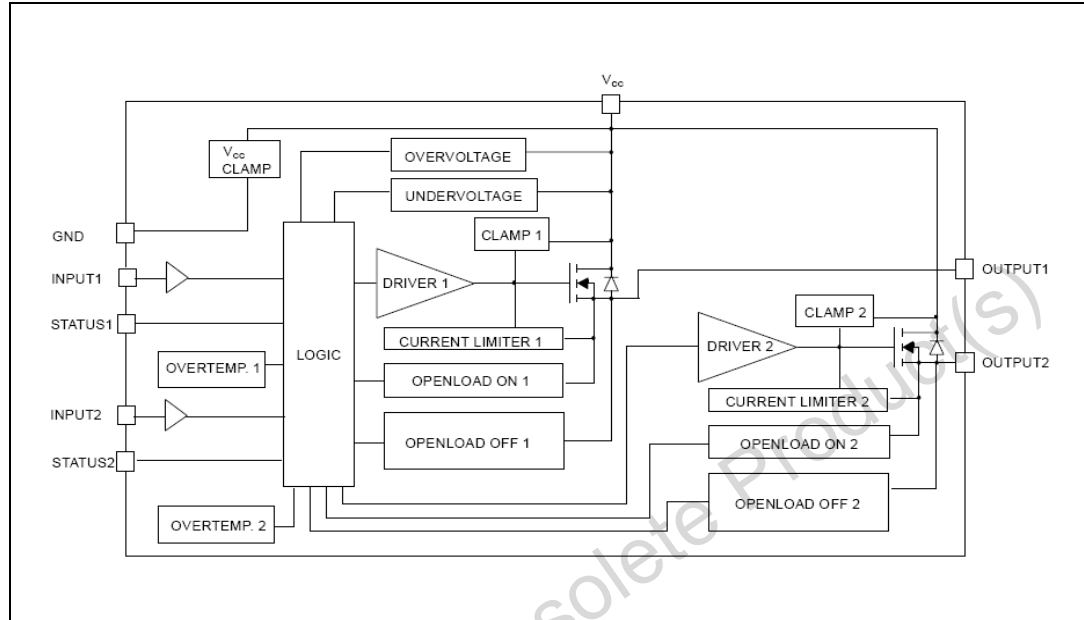


Figure 2. Configuration diagram (top view)

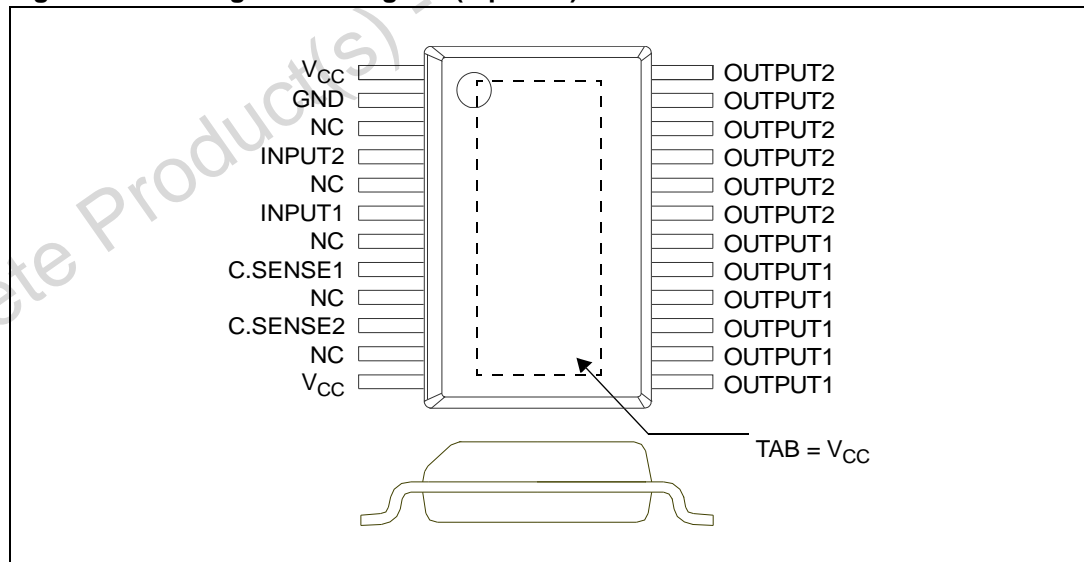


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10KΩ resistor

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## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage	41	V
-V <sub>CC</sub>	Reverse DC supply voltage	- 0.3	V
-I <sub>GND</sub>	DC reverse ground pin current	- 200	mA
I <sub>OUT</sub>	DC output current	Internally limited	A
-I <sub>OUT</sub>	Reverse DC output current	- 6	A
I <sub>IN</sub>	DC input current	+/- 10	mA
I <sub>stat</sub>	DC status current	+/- 10	mA
V <sub>ESD</sub>	Electrostatic discharge (human body model:R=1.5KΩ; C=100pF)		
	- Input	4000	V
	- Status	4000	V
	- Output	5000	V
	- V <sub>CC</sub>	5000	V
P <sub>tot</sub>	Power dissipation T <sub>C</sub> = 25°C	54	W
T <sub>j</sub>	Junction operating temperature	Internally limited	°C
T <sub>c</sub>	Case operating temperature	- 40 to 150	°C
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C

### 2.2 Thermal data

**Table 4. Thermal data (per island)**

Symbol	Parameter	Value		Unit
R <sub>thj-case</sub>	Thermal resistance junction-case (max)	2.3		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient (one chip ON) (max)	57 <sup>(1)</sup>	42 <sup>(2)</sup>	°C/W

- When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins.
- When mounted on a standard single-sided FR-4 board with 8cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins.

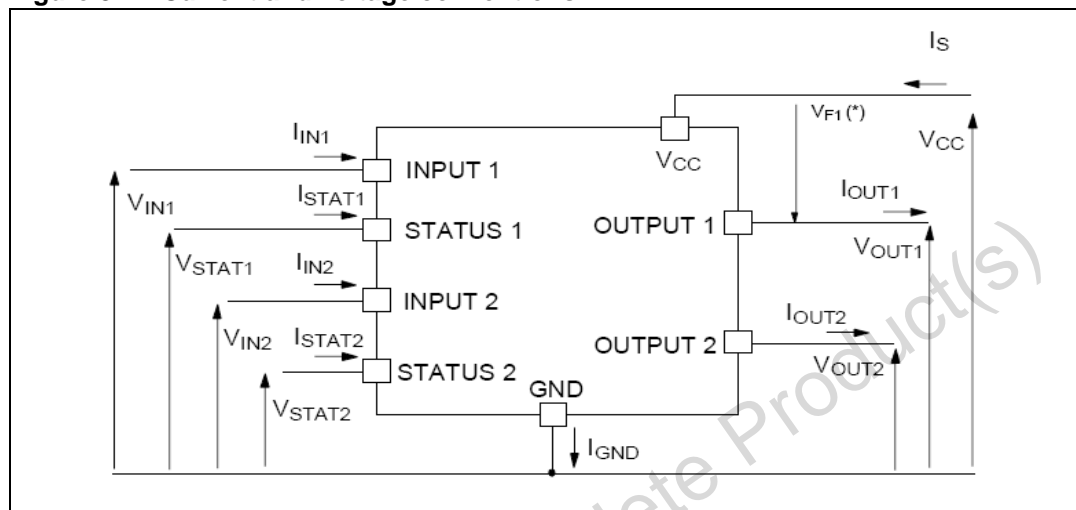
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### 2.3 Electrical characteristics

Values specified in this section are for  $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise stated.

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.

Table 5. Power output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 2A$ ; $T_j = 25^{\circ}C$ $I_{OUT} = 2A$ ; $T_j = 125^{\circ}C$			60 120	mΩ mΩ
$I_S$	Supply current	Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$		12	40	μA
		Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$ ; $T_j = 25^{\circ}C$		12	25	μA
		On-state; $V_{CC} = 13V$ ; $V_{IN} = 5V$ ; $I_{OUT} = 0A$		5	7	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V$ ; $V_{OUT} = 3.5V$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$			3	μA



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**Table 6. Switching ( $V_{CC} = 13V$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ from $V_{IN}$ rising edge to $V_{OUT} = 1.3V$	-	30	-	$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ from $V_{IN}$ falling edge to $V_{OUT} = 11.7V$	-	30	-	$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 1.3V$ to $V_{OUT} = 10.4V$	-	See Figure 14	-	$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 11.7V$ to $V_{OUT} = 1.3V$	-	See Figure 13	-	$V/\mu s$

**Table 7.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$I_{OUT} = 1.3A$ ; $T_j = 150^\circ C$	-	-	0.6	V

**Table 8. Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6 mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal Operation; $V_{STAT} = 5V$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 -0.7	8	V V

**Table 9. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25V$	1			$\mu A$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 -0.7	8	V V

**Table 10. Protections<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	$^\circ C$
$T_R$	Reset temperature		135			$^\circ C$

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Table 10. Protections<sup>(1)</sup> (continued)

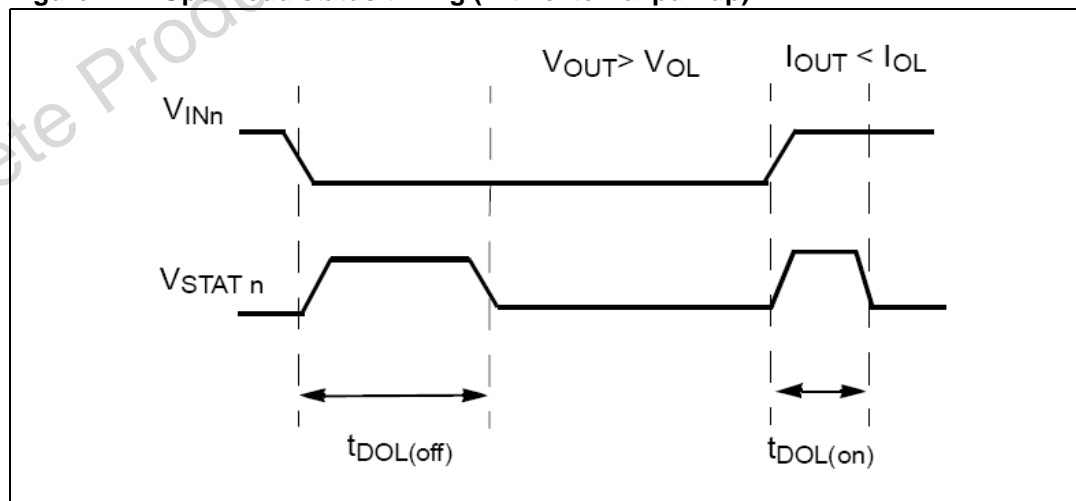
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{hyst}$	Thermal hysteresis		7	15		°C
$t_{SDL}$	Status delay in overload conditions	$T_j > T_{TSD}$			20	μs
$I_{lim}$	Current limitation	$5.5V < V_{CC} < 36V$	6	9	15 15	A A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2A; L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Open-load on-state detection threshold	$V_{IN} = 5V$	50	100	200	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0A$			200	μs
$V_{OL}$	Open-load off-state voltage detection threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	μs

Figure 4. Open-load status timing (with external pull-up)



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Figure 5. Over temperature status timing

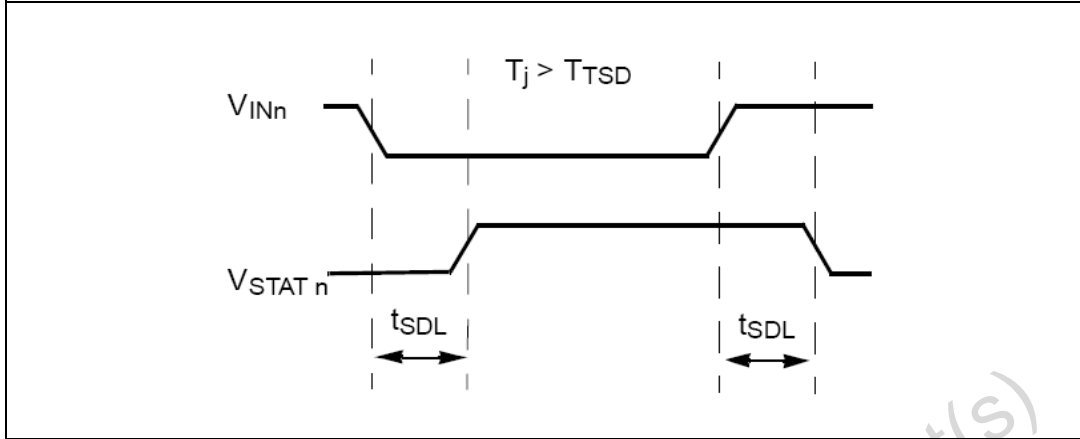


Figure 6. Switching time waveforms

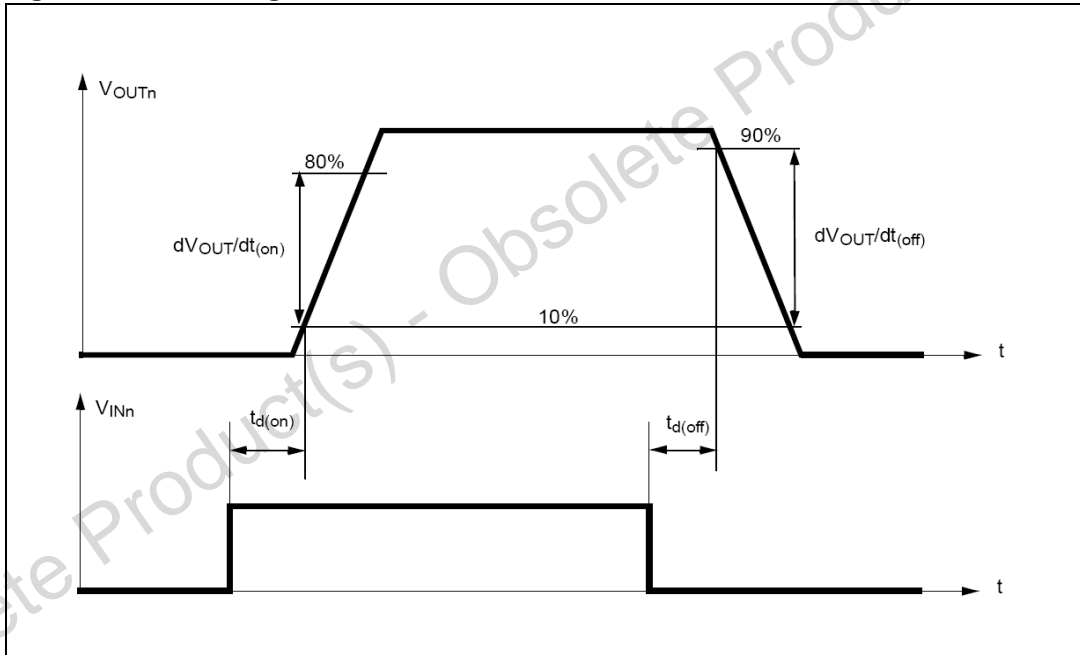


Table 12. Truth table

Conditions	Inputn	Outputn	Statusn
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H ( $T_j > T_{TSD}$ ) L
Over temperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X

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Table 12. Truth table (continued)

Conditions	Inputn	Outputn	Statusn
Overvoltage	L	L	H
	H	L	H
Output voltage > V <sub>OLn</sub>	L	H	L
	H	H	H
Output current < I <sub>OLn</sub>	L	L	H
	H	H	L

Table 13. Electrical transient requirements on V<sub>CC</sub> pin (part 1/3)

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1μs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1μs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

Table 14. Electrical transient requirements on V<sub>CC</sub> pin (part 2/3)

ISO T/R 7637/1 Test pulse	Test level			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

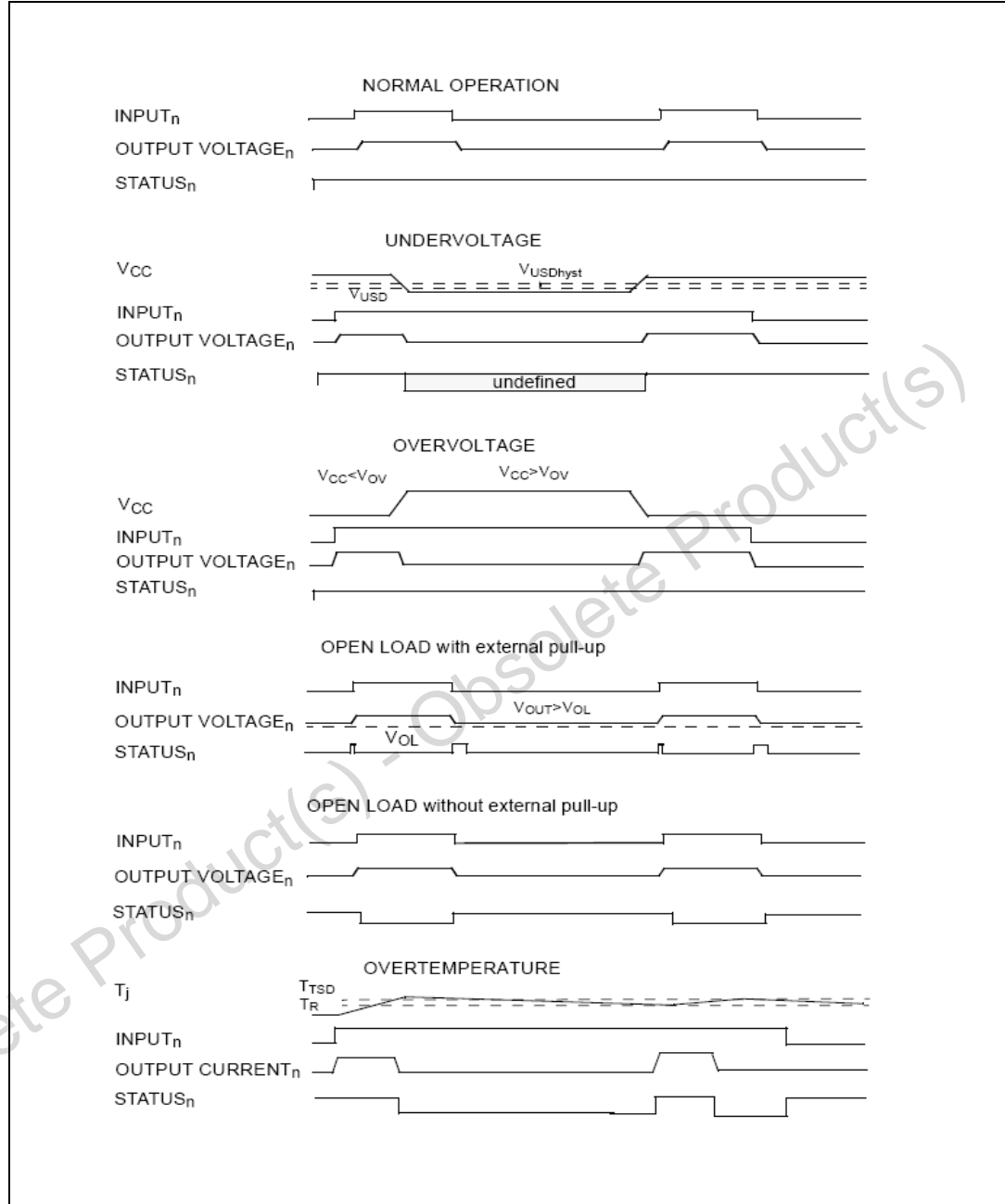
Table 15. Electrical transient requirements on V<sub>CC</sub> pin (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

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Figure 7. Waveforms



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2.4 Electrical characteristics curves

Figure 8. Off-state output current

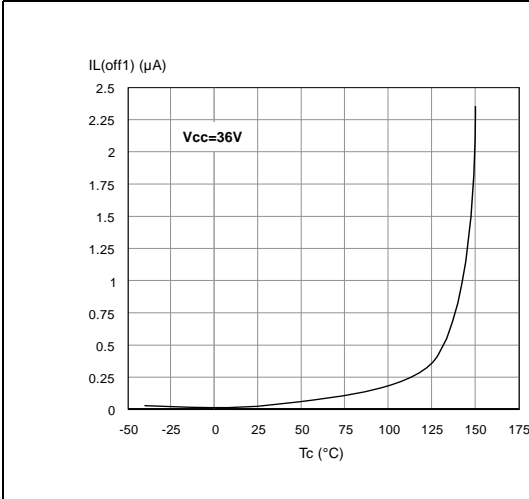


Figure 9. High level input current

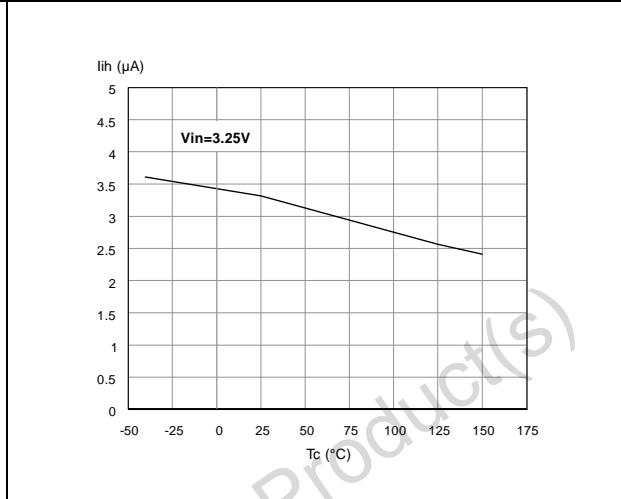


Figure 10. Input clamp voltage

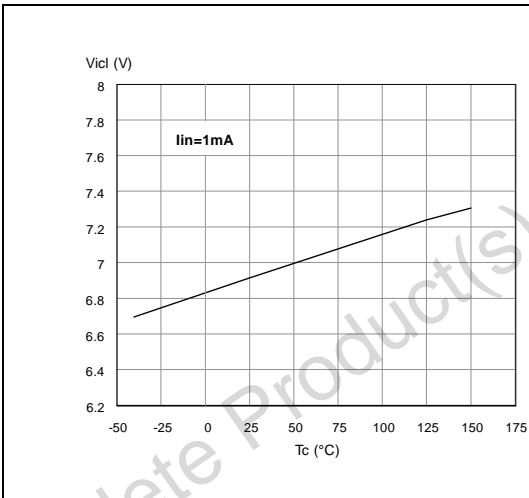


Figure 11. Status leakage current

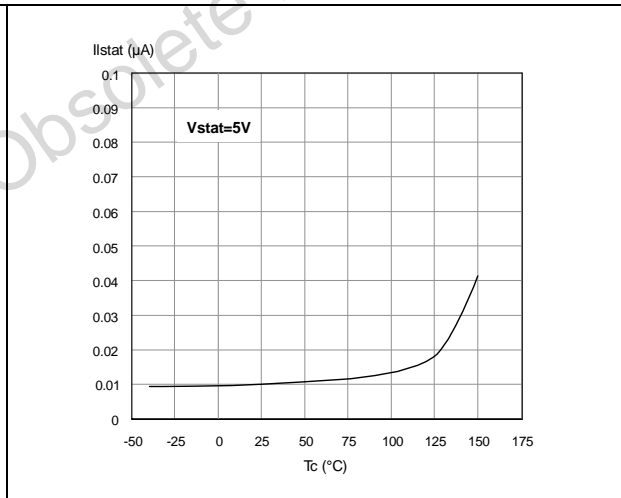


Figure 12. Status low output voltage

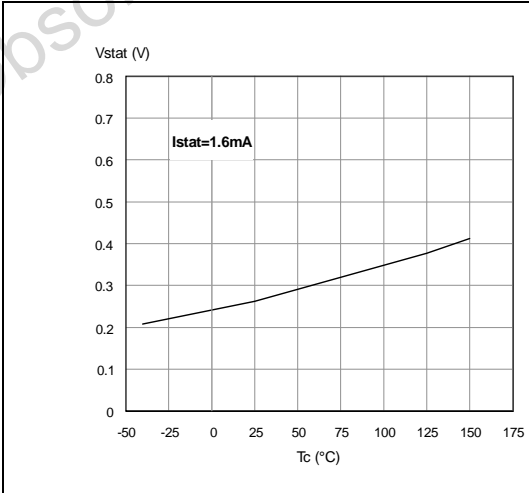
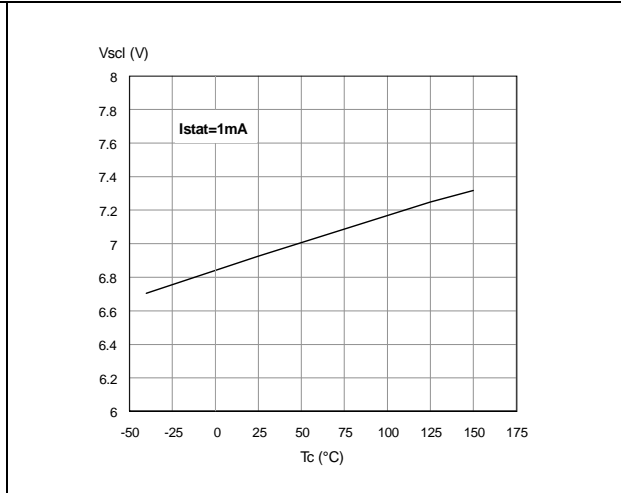


Figure 13. Status clamp voltage



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Figure 14. Turn-on voltage slope

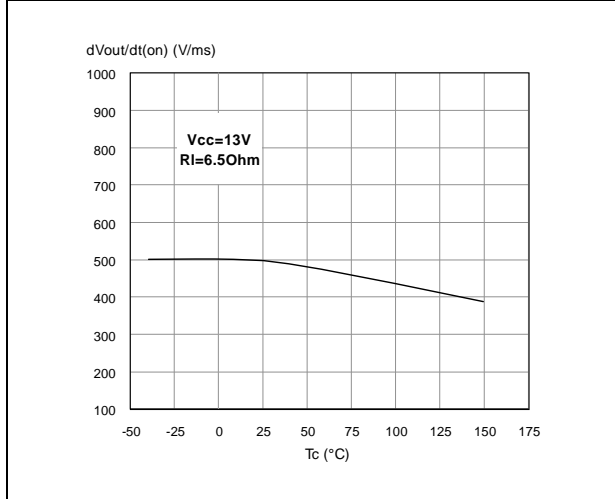


Figure 15. Turn-off voltage slope

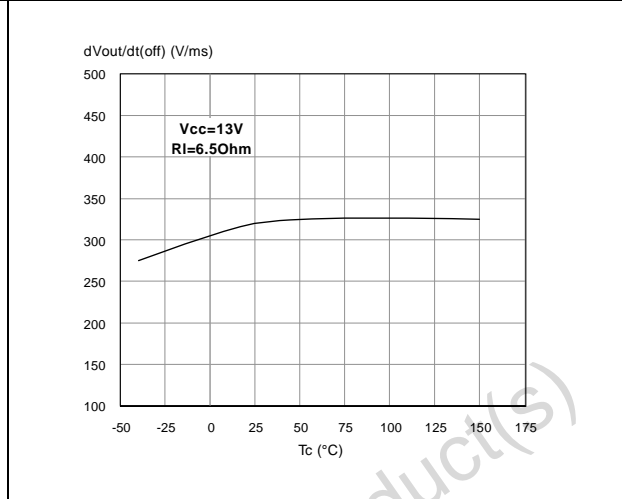


Figure 16. On-state resistance vs Tcase

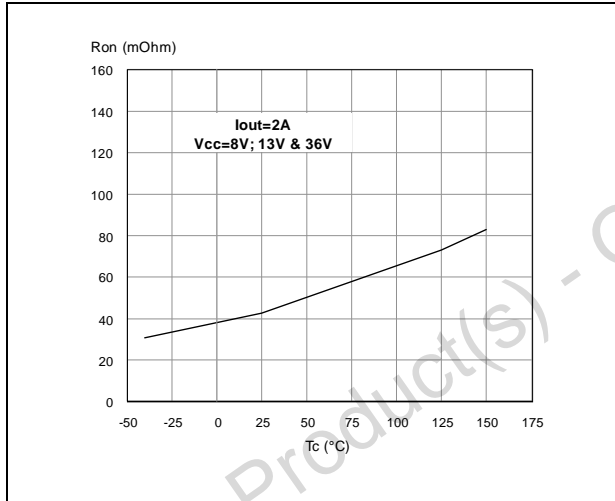


Figure 17. On-state resistance vs Vcc

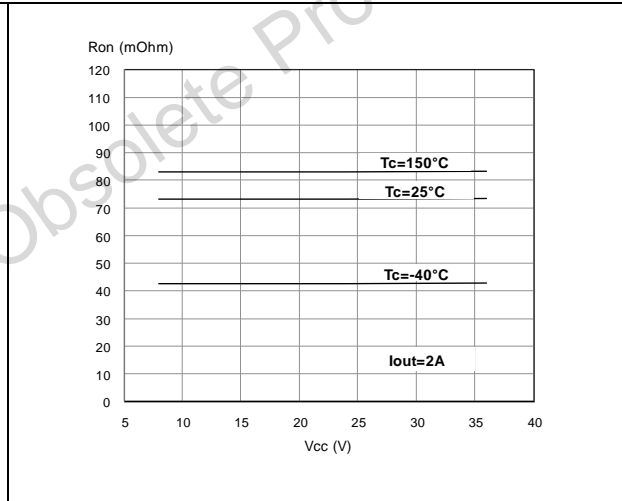


Figure 18. I<sub>LIM</sub> vs T<sub>case</sub>

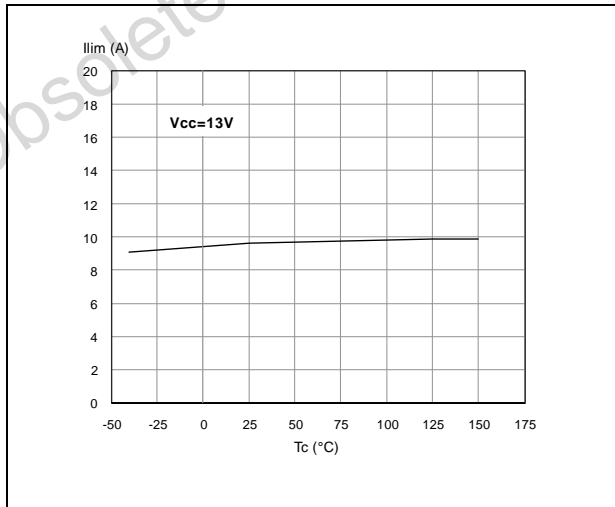
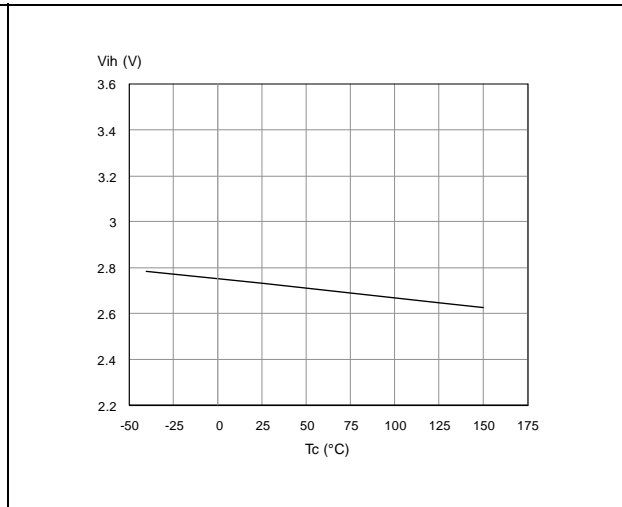


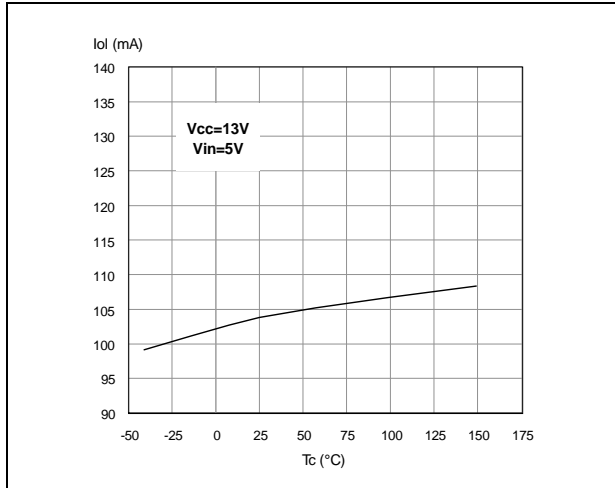
Figure 19. Input high level



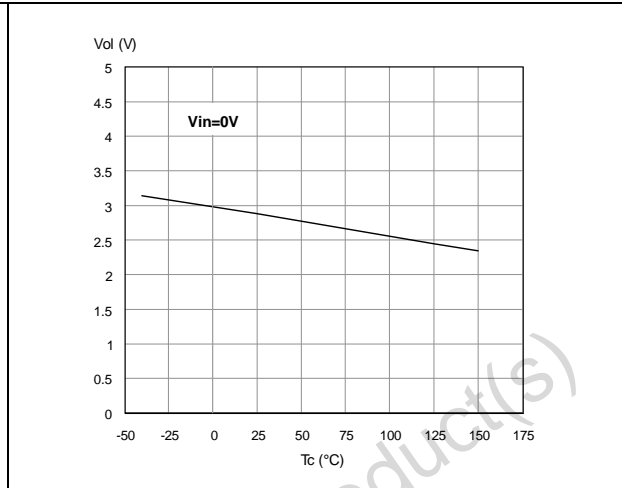
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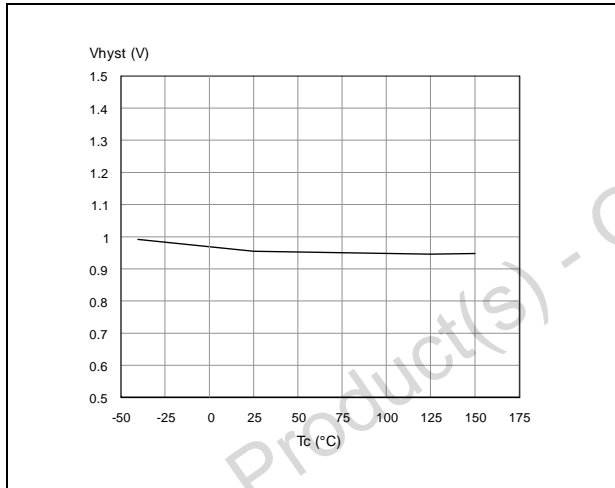
**Figure 20. Open-load on-state detection threshold**



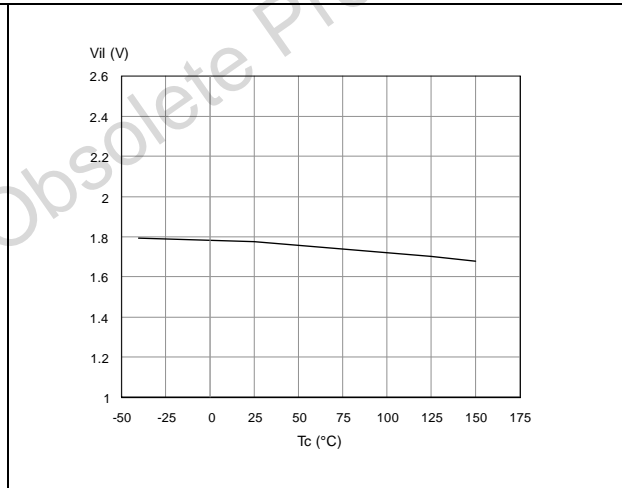
**Figure 21. Open-load off-state detection threshold**



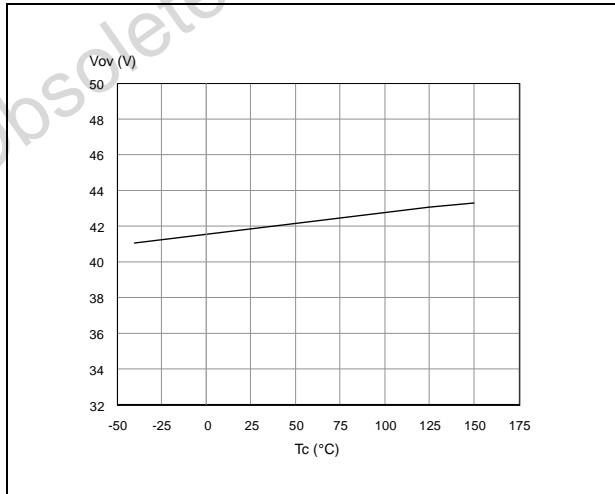
**Figure 22. Input hysteresis voltage**



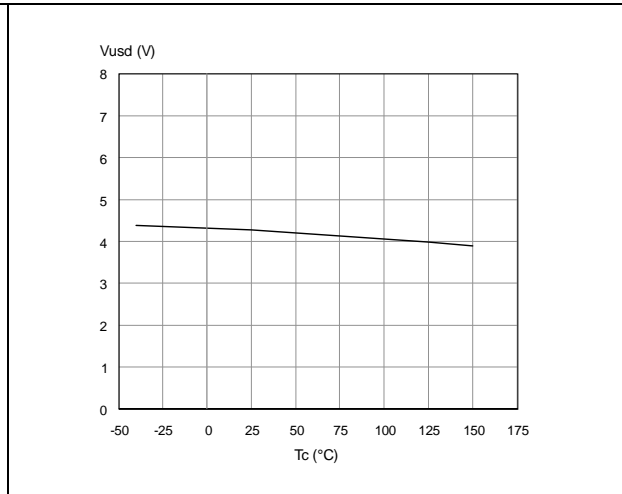
**Figure 23. Input low level**



**Figure 24. Overvoltage shutdown**



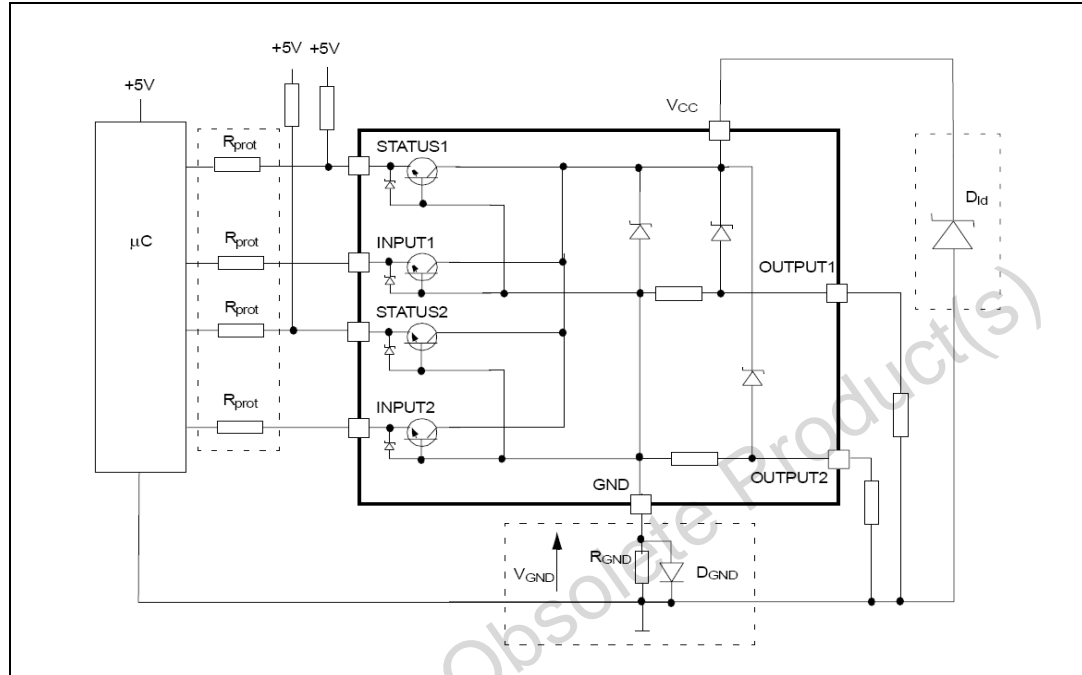
**Figure 25. Undervoltage shutdown**





### 3 Application information

Figure 26. Application schematic



#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: a resistor in the ground line ( $R_{GND}$ only)

This can be used with any type of load.

The following show how to dimension the  $R_{GND}$  resistor:

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in  $R_{GND}$  (when  $V_{CC} < 0$  during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

**VND830PEP-E**
**Application information**

If the calculated power dissipation leads to a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

**3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line**

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

**3.2 Load dump protection**

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than those shown in the ISO T/R 7637/1 table.

**3.3 MCU I/O protection**

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

**Example**

For the following conditions:

$$V_{CCpeak} = -100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

**3.4 Open-load detection in off-state**

Off-state open-load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

**Application information**

**VND830PEP-E**

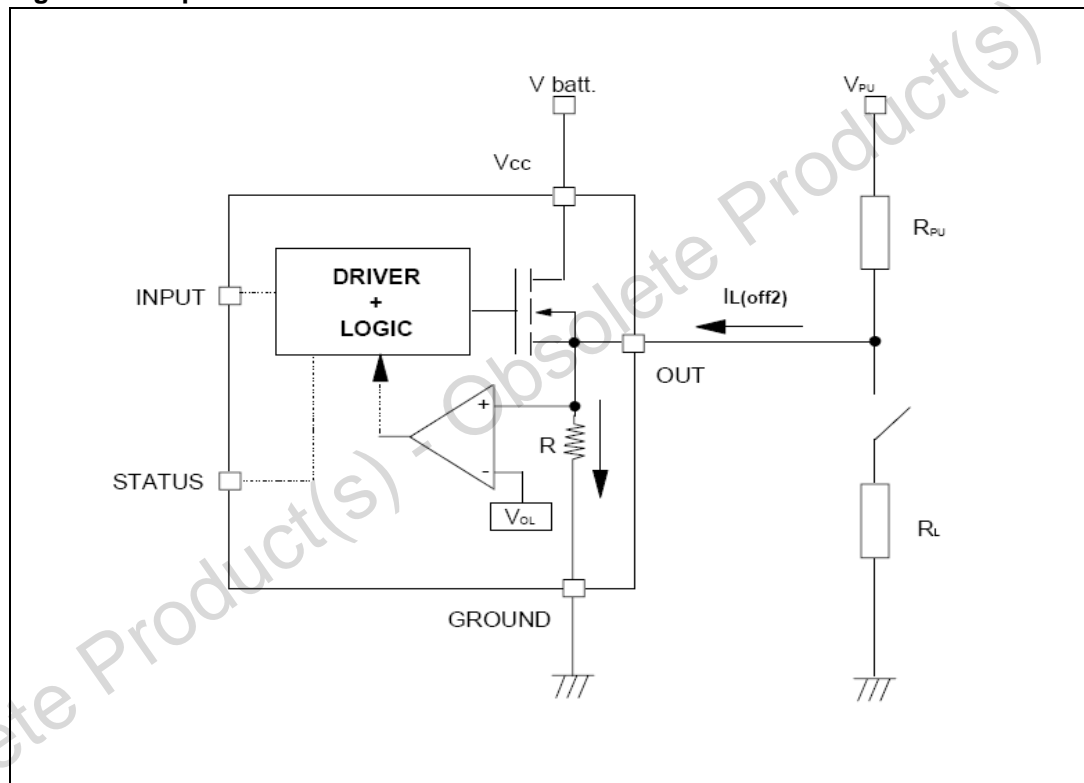
1. no false open-load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  

$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$$
2. no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  

$$R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$$

Because  $I_{s(OFF)}$  may significantly increase if  $V_{out}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched off when the module is in standby. The values of  $V_{OLmin}$ ,  $V_{OLmax}$  and  $I_{L(off2)}$  are available in the electrical characteristics section.

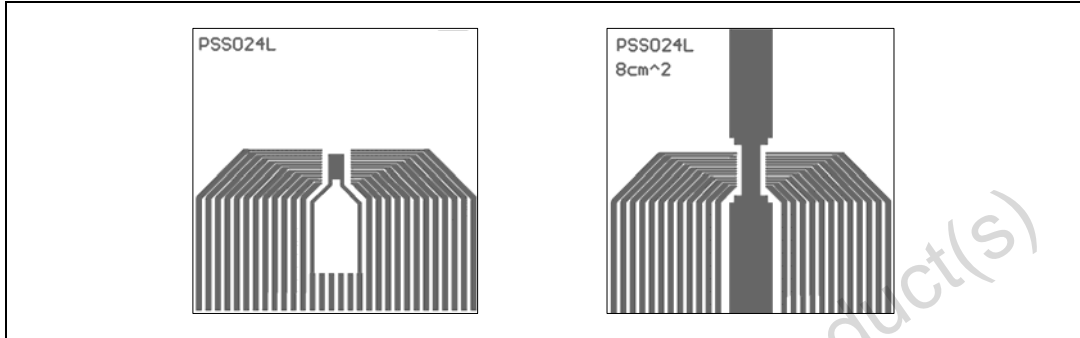
**Figure 27. Open-load detection in off-state**



## 4 Package and PC board thermal data

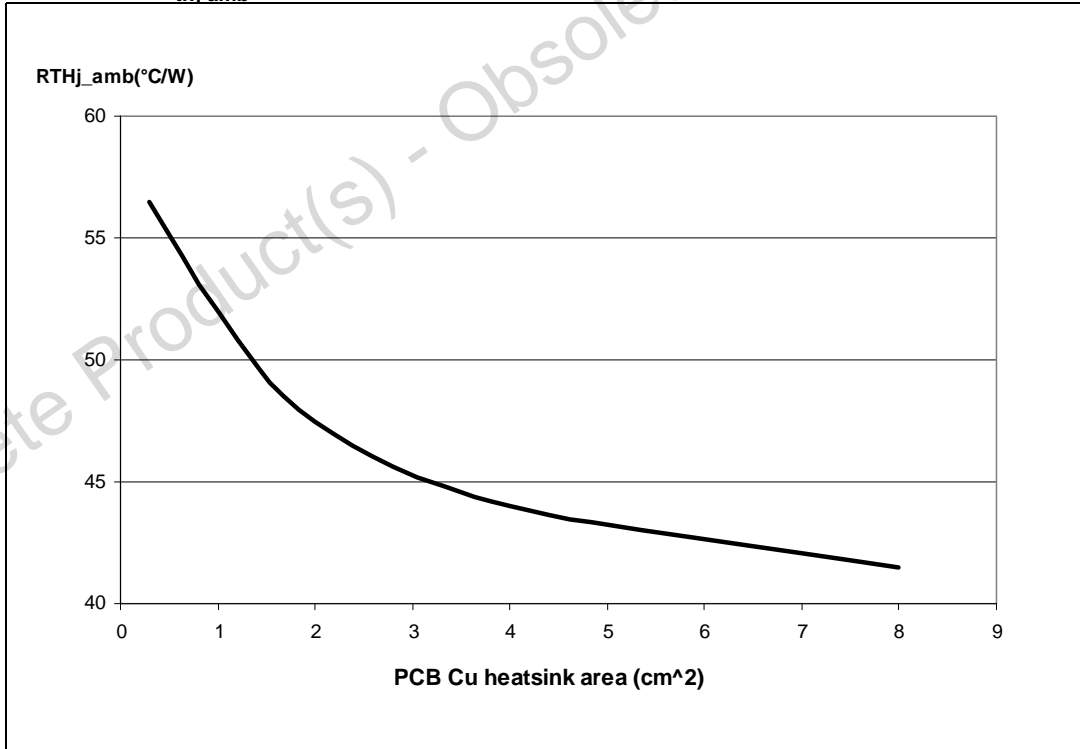
### 4.1 PowerSSO-24 thermal data

Figure 28. PowerSSO-24 PC board

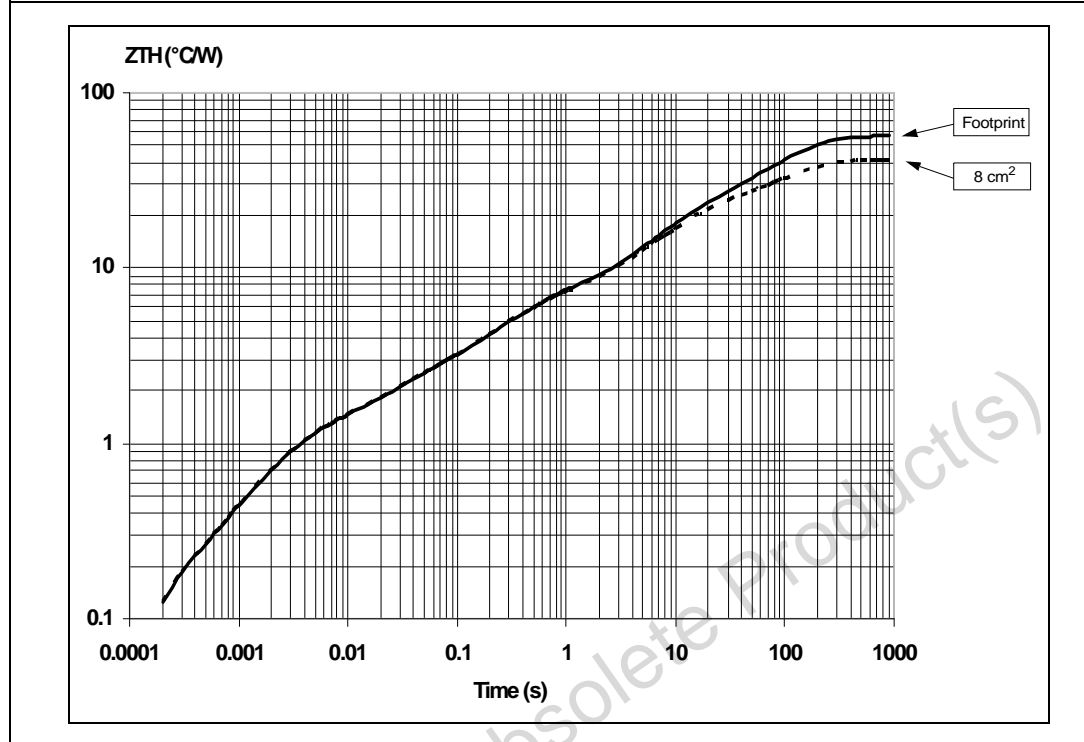


Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 78mm x 78mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

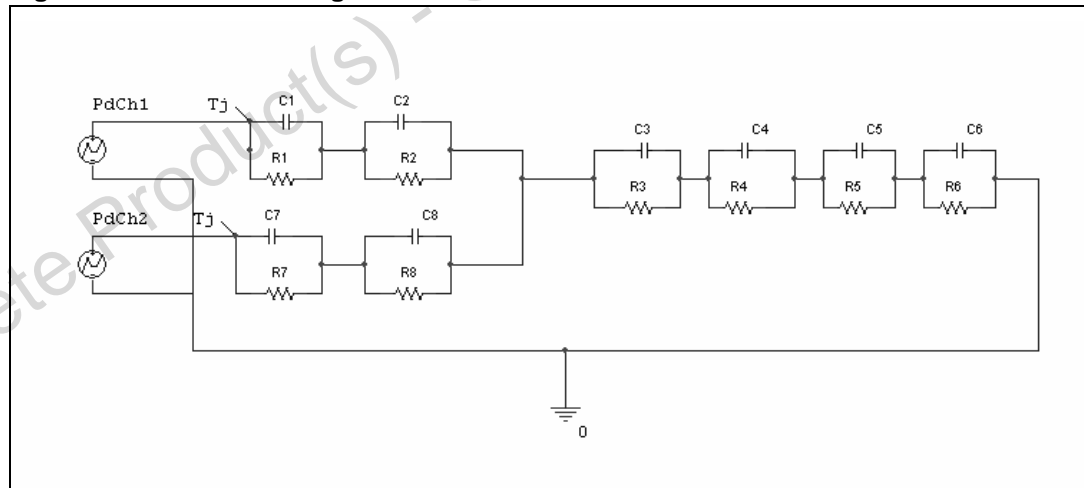
Figure 29.  $R_{thj-amb}$  vs PCB copper area in open box



**Figure 30. PowerSSO-24 thermal impedance junction ambient single pulse**



**Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24**



**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

VND830PEP-E

Package and PC board thermal data

Table 16. Thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	8
R1 = R7 (°C/W)	0.1	
R2 = R8 (°C/W)	0.9	
R3 (°C/W)	1	
R4 (°C/W)	4	
R5 (°C/W)	13.5	
R6 (°C/W)	37	22
C1 = C7 (W.s/°C)	0.0006	
C2 = C8 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.025	
C4 (W.s/°C)	0.08	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

Obsolete Product(s) - Obsolete Product(s)

## 5 Package information

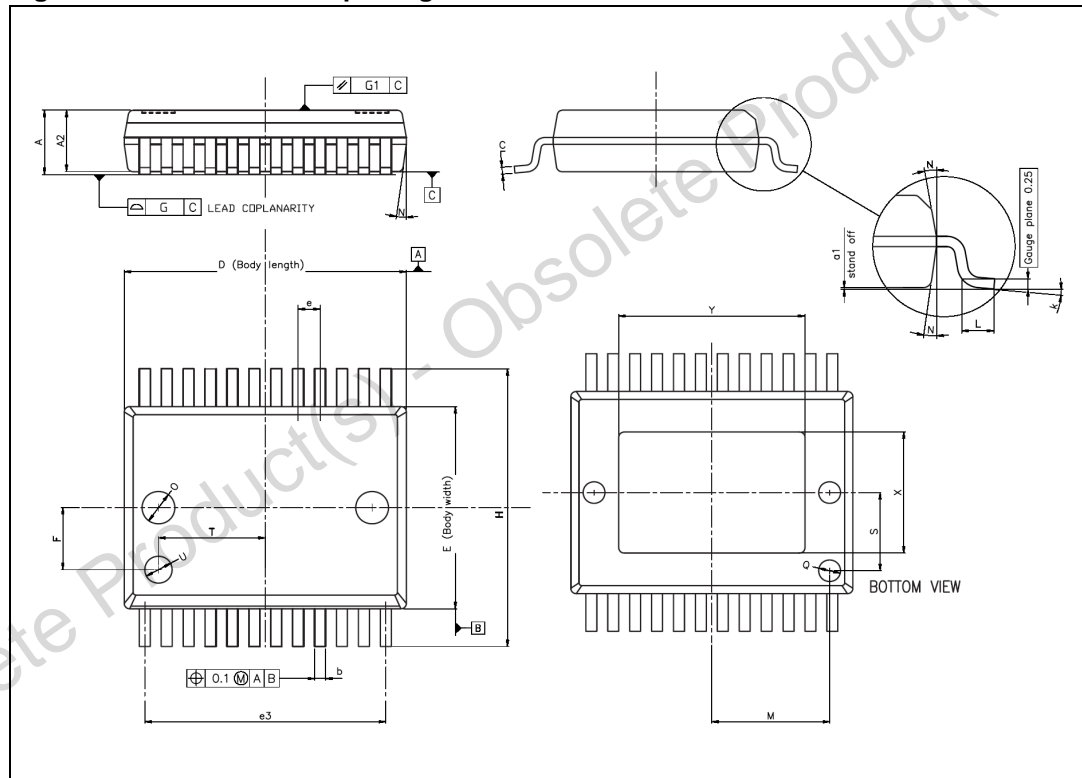
### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

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### 5.2 PowerSSO-24 mechanical data

Figure 32. PowerSSO-24 package dimensions



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Package information

Table 17. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
N			10°
X	4.1		4.7
Y	6.5		7.1



## 6 Revision history

Table 18. Document revision history

Date	Revision	Changes
04-Oct-2004	1	Initial release.
15-Nov-2004	2	Mechanical data updating. PowerSSO-24 thermal characteristics insertion
27-Nov-2004	3	PC board copper area correction.
12-Dec-2005	4	Electrical characteristics insertion. Absolute maximum ratings modification.
01-Jul-2009	5	Updated <i>Figure 17: PowerSSO-24 mechanical data</i> : <ul style="list-style-type: none"> <li>– Deleted A (min) value</li> <li>– Changed A (max) value from 2.47 to 2.45</li> <li>– Changed A2 (max) value from 2.40 to 2.35</li> <li>– Changed a1 (max) value from 0.075 to 0.1</li> <li>– Inserted F and k rows</li> </ul>
20-Sep-2013	6	Updated Disclaimer.

## VND830PEP-E

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