ALPHA & OMEGA
SEMICONDUCTOR

AO3434
30V N-Channel MOSFET

General Description

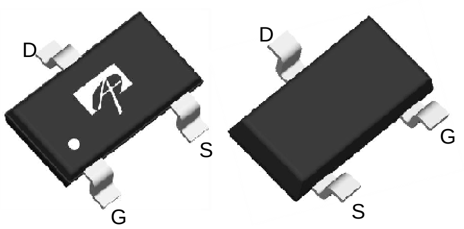
The AO3434 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

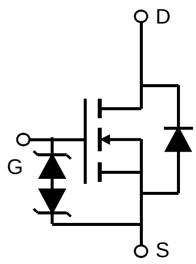
Product Summary

V_{DS} (V) = 30V
I_D = 4.2A (V$_{GS}$ = 10V)
$R_{DS(ON)}$ < 52mΩ (V$_{GS}$ = 10V)
$R_{DS(ON)}$ < 75mΩ (V$_{GS}$ = 4.5V)

ESD protected

SOT23
Top View **Bottom View**





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum 10 sec	Maximum Steady-State	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [A,F]	T_A=25℃	I_D	4.2	3.5	A
	T_A=70℃		3.3	2.8	
Pulsed Drain Current [B]		I_{DM}	30		
Power Dissipation	T_A=25℃	P_D	1.4	1.0	W
	T_A=70℃		0.9	0.64	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		100	125	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	63	80	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±16V			10	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	1.32	1.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=4.2A		43	52	mΩ
		T_J=125℃		58	74	
		V_{GS}=4.5V, I_D=2A		59	75	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4.2A		8.5		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.77	1	V
I_S	Maximum Body-Diode Continuous Current				1.8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		269	340	pF
C_{oss}	Output Capacitance			65		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1	1.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=4.2A		5.7	7.2	nC
Q_g(4.5V)	Total Gate Charge			3		nC
Q_{gs}	Gate Source Charge			1.37		nC
Q_{gd}	Gate Drain Charge			0.65		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=3.6Ω, R_{GEN}=3Ω		2.6	3.8	ns
t_r	Turn-On Rise Time			5.5	8	ns
$t_{D(off)}$	Turn-Off DelayTime			15.2	23	ns
t_f	Turn-Off Fall Time			3.7	5.5	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=4.2A, dI/dt=100A/µs		15.5	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=4.2A, dI/dt=100A/µs		7.1		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F.The current rating is based on the t≤10s thermal resistance rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

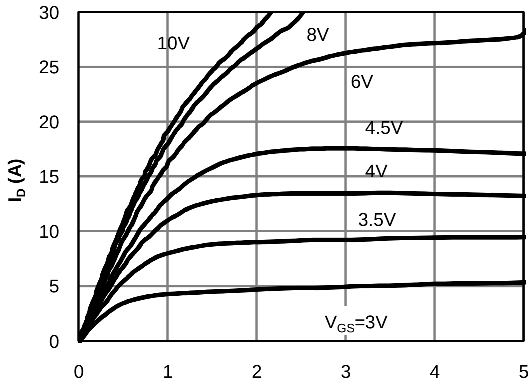


Fig 1: On-Region Characteristics

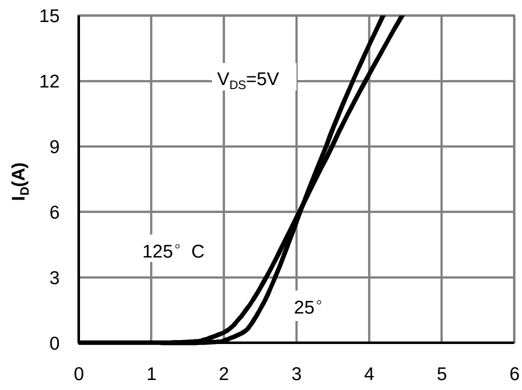


Figure 2: Transfer Characteristics

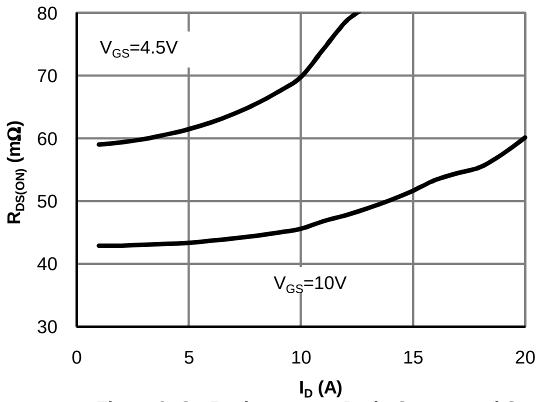


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

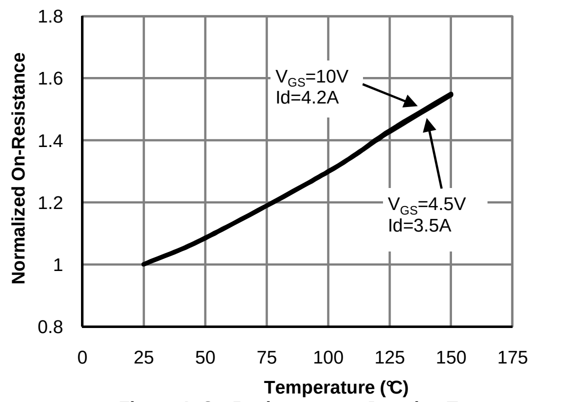


Figure 4: On-Resistance vs. Junction Temperature

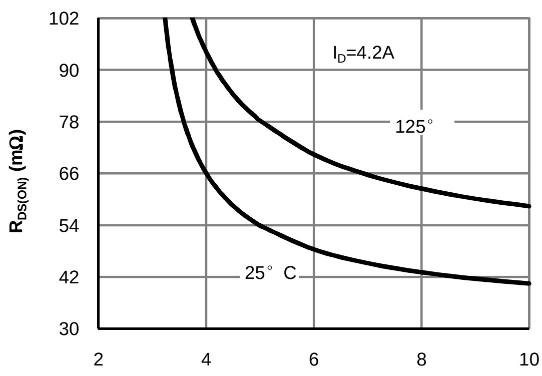


Figure 5: On-Resistance vs. Gate-Source Voltage

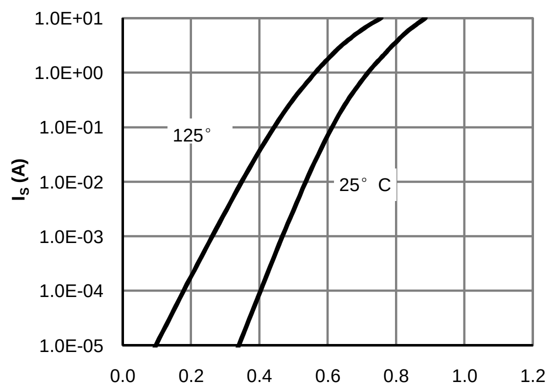


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

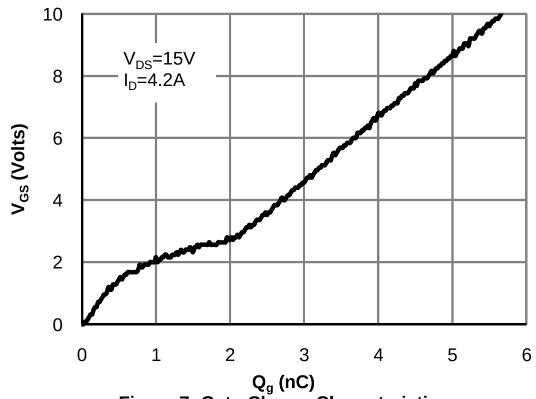


Figure 7: Gate-Charge Characteristics

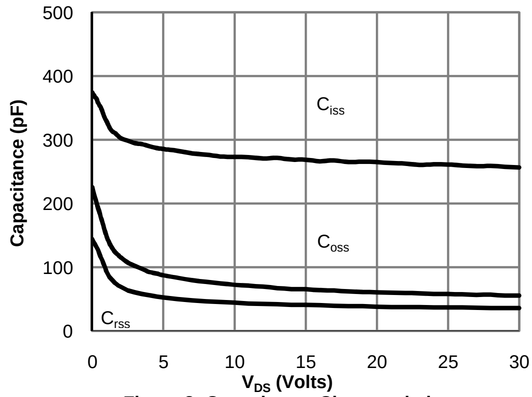


Figure 8: Capacitance Characteristics

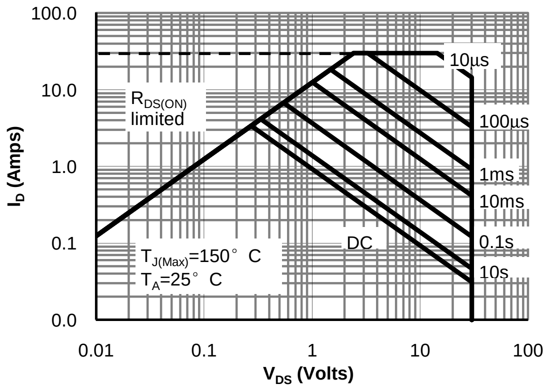


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

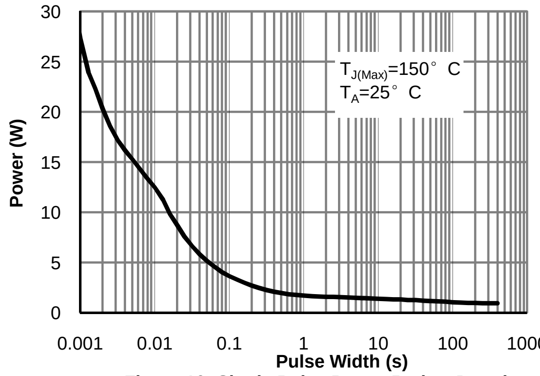


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

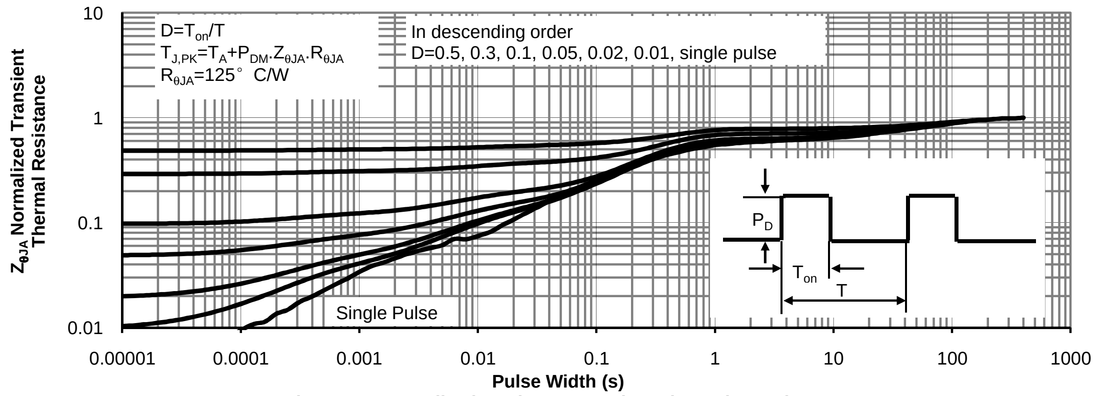


Figure 11: Normalized Maximum Transient Thermal Impedance