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AO6804

Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

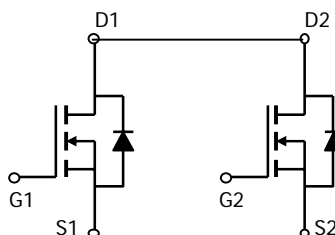
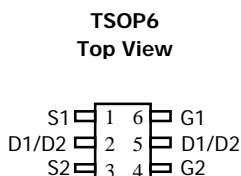


General Description

The AO6804 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. AO6804 is Pb-free (meets ROHS & Sony 259 specifications).

Features

$V_{DS} = 20V$
 $I_D = 5.0A$ ($V_{GS} = 4.5V$)
Typical R_{ds}
 $R_{DS(ON)} < 24m\Omega$ ($V_{GS} = 4.5V$)
 $R_{DS(ON)} < 26m\Omega$ ($V_{GS} = 4.0V$)
 $R_{DS(ON)} < 28m\Omega$ ($V_{GS} = 3.1V$)
 $R_{DS(ON)} < 31m\Omega$ ($V_{GS} = 2.5V$)



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	10 Sec	Steady State	Units	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 12		V	
Continuous Drain Current ^A	I_D	$T_A=25^\circ C$	5	4	A
		$T_A=70^\circ C$	4	3.2	
Pulsed Drain Current ^B	I_{DM}	25			
Power Dissipation ^A	P_D	$T_A=25^\circ C$	1.3	0.8	W
		$T_A=70^\circ C$	0.8	0.5	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10s$	$R_{\theta JA}$	76	95	$^\circ C/W$
Maximum Junction-to-Ambient ^A Steady State		118	150	$^\circ C/W$
Maximum Junction-to-Lead ^C Steady State	$R_{\theta JL}$	54	68	$^\circ C/W$

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20V, V _{GS} = 0V T _J = 55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} = 0V, V _{GS} = ±12V			±500	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.5	0.75	1.2	V
I _{D(ON)}	On state drain current	V _{GS} = 4.5V, V _{DS} = 5V	25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 4.5V, I _D = 5.0A T _J =125°C	18 25	24 33	32 43	mΩ
		V _{GS} = 4.0V, I _D = 4.5A	22	26	34	
		V _{GS} = 3.1V, I _D = 4.5A	21	28	37	mΩ
		V _{GS} = 2.5V, I _D = 4.0A	22	31	42	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 5.0A		7		S
V _{SD}	Diode Forward Voltage	I _S = 1A, V _{GS} = 0V		0.65	1	V
I _S	Maximum Body-Diode Continuous Current				1.1	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz		580	725	pF
C _{oss}	Output Capacitance			95		pF
C _{rss}	Reverse Transfer Capacitance			70		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.5	5.3	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} = 4.5V, V _{DS} = 10V, I _D = 5A		5.8	7.7	nC
Q _{gs}	Gate Source Charge			1		nC
Q _{gd}	Gate Drain Charge			1.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =10V, R _L =2.0Ω, R _{GEN} =3Ω		2.4		ns
t _r	Turn-On Rise Time			6.4		ns
t _{D(off)}	Turn-Off DelayTime			38		ns
t _f	Turn-Off Fall Time			9.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =5A, dI/dt=100A/μs		18	24
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5A, dI/dt=100A/μs		6		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using < 300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

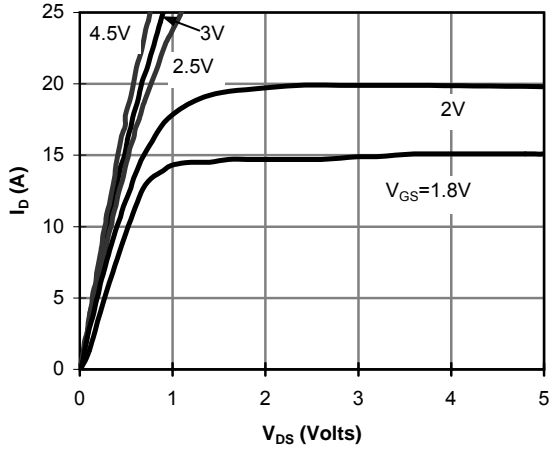


Figure 1: On-Region Characteristics

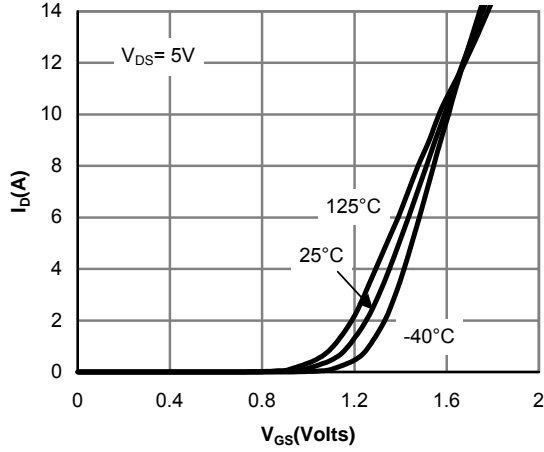


Figure 2: Transfer Characteristics

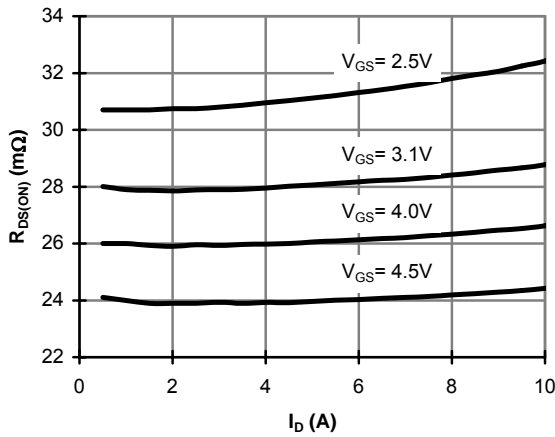


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

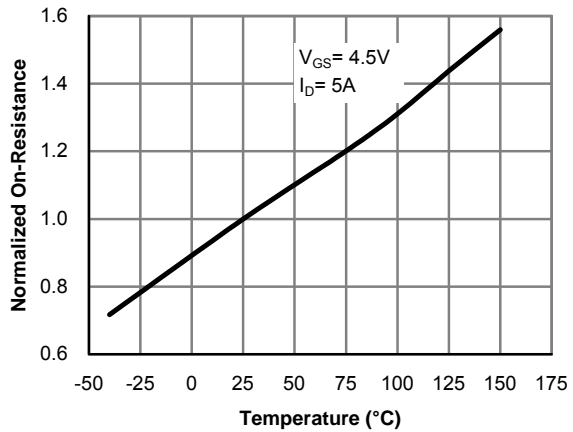


Figure 4: On-Resistance vs. Junction Temperature

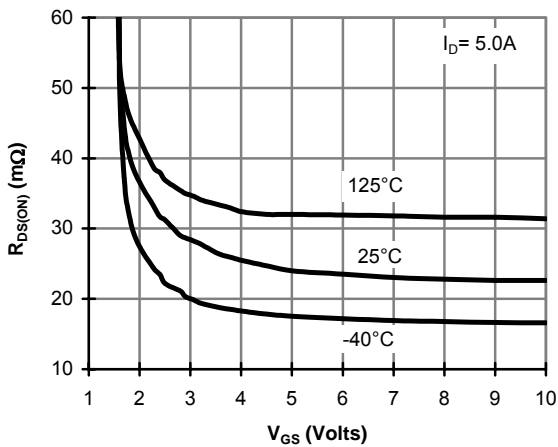


Figure 5: On-Resistance vs. Gate-Source Voltage

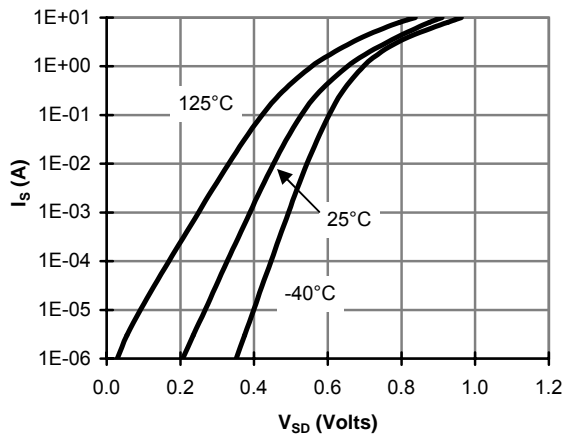


Figure 6: Body-Diode Characteristics

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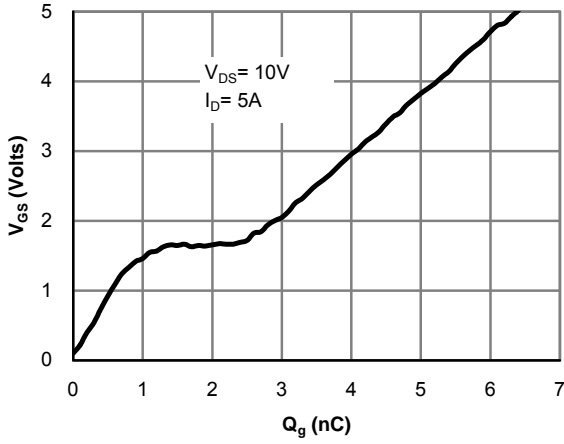


Figure 7: Gate-Charge Characteristics

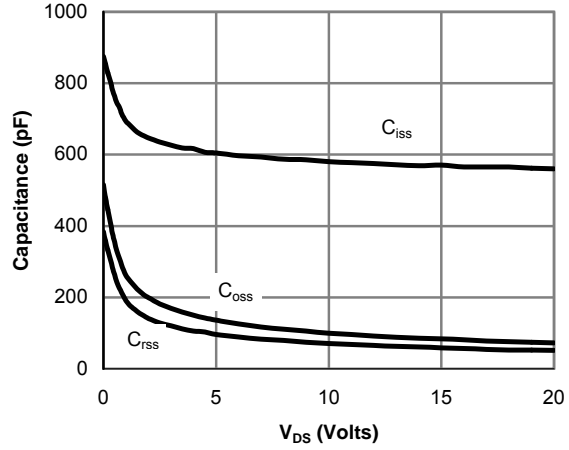


Figure 8: Capacitance Characteristics

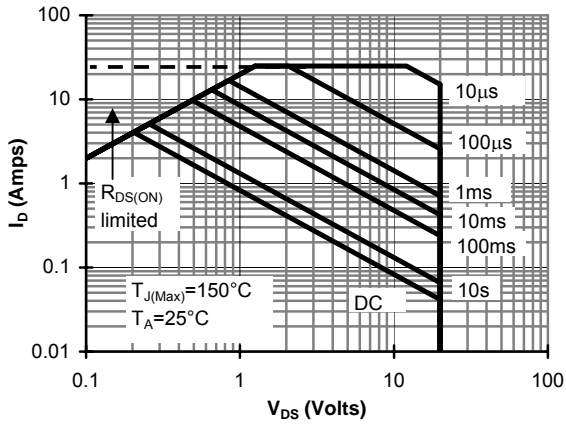


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

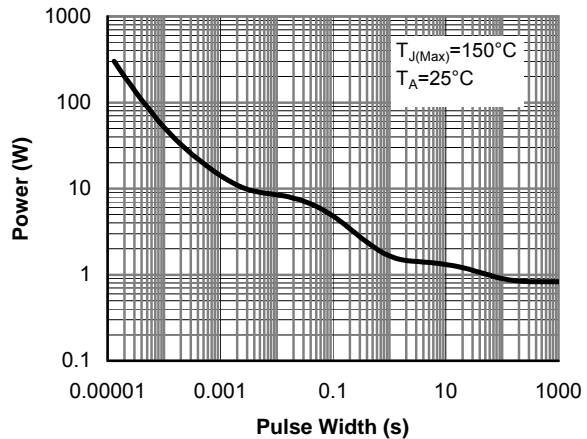


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

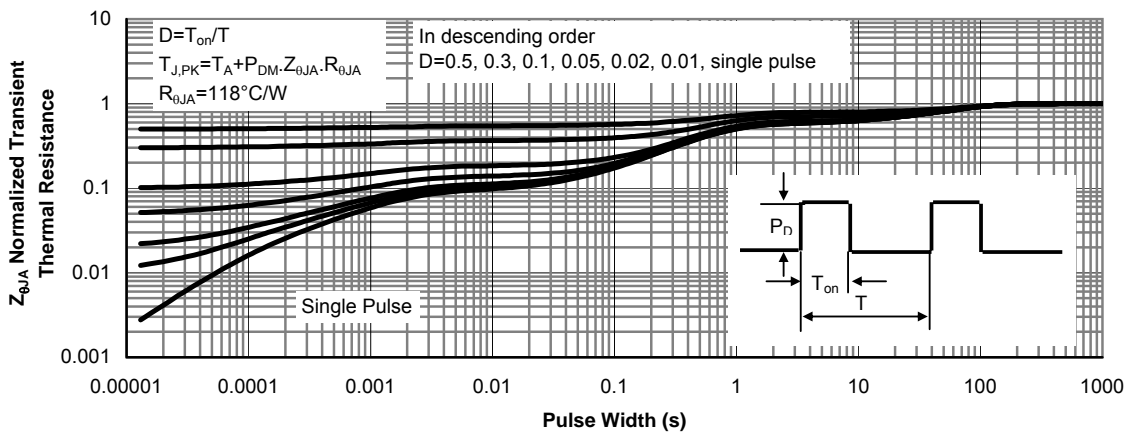


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)