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ADM2482EBRWZ-REEL7

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2.5 kV Isolated RS-485 Transceivers with Integrated Transformer Driver

ADM2482E/ADM2487E

FEATURES

- Isolated RS-485/RS-422 transceivers, configurable as half duplex or full duplex
- Integrated oscillator driver for external transformer
- ±15 kV ESD protection on RS-485 input/output pins
- Complies with TIA/EIA-485-A-98 and ISO 8482:1987(E)
- Data rate: 500 kbps/16 Mbps
- 5 V or 3.3 V operation (V_{DD1})
- 256 nodes on bus
- True fail-safe receiver inputs
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - VDE certificates of conformity
    - DIN VVDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak
- Thermal shutdown protection
- Operating temperature range: −40°C to +85°C
- Wide-body, 16-lead SOIC package

APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- Industrial field networks
- Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

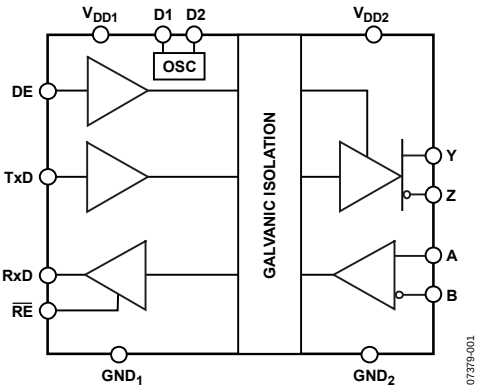

Figure 1.

GENERAL DESCRIPTION

The ADM2482E/ADM2487E are isolated data transceivers with ±15 kV ESD protection and are suitable for high speed, half-duplex or full-duplex communication on multipoint transmission lines. For half-duplex operation, the transmitter outputs and receiver inputs share the same transmission line. Transmitter Output Pin Y is linked externally to Receiver Input Pin A, and Transmitter Output Pin Z to Receiver Input Pin B. The parts are designed for balanced transmission lines and comply with TIA/EIA-485-A-98 and ISO 8482:1987(E).

The devices employ the Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. An on-chip oscillator outputs a pair of square waveforms that drive an external transformer to provide isolated power. The logic side of the device is powered with either a 5 V or a 3.3 V supply, and the bus side is powered with an isolated 3.3 V supply.

The ADM2482E/ADM2487E driver has an active high enable, and the receiver has an active low enable. The driver output enters a high impedance state when the driver enable signal is low. The receiver output enters a high impedance state when the receiver enable signal is high.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation. The part is fully specified over the industrial temperature range of −40°C to +85°C and is available in a 16-lead, wide-body SOIC package.

Rev. A

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5/08—Revision 0: Initial Version

SPECIFICATIONS

Each voltage is relative to its respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current, Logic Side	I_{DD1}					
TxD/RxD Data Rate < 500 kbps				3.5	mA	Unloaded output
ADM2487E TxD/RxD Data Rate = 500 kbps				4	mA	Half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 25
ADM2482E TxD/RxD Data Rate = 16 Mbps				6.0	mA	Half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 25
Power Supply Current, Bus Side	I_{DD2}					
TxD/RxD Data Rate < 500 kbps				17	mA	Unloaded output
ADM2487E TxD/RxD Data Rate = 500 kbps				40	mA	V_{DD2} = 3.6 V, half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 25
ADM2482E TxD/RxD Data Rate = 16 Mbps				50	mA	V_{DD2} = 3.6 V, half-duplex configuration, $R_{TERMINATION}$ = 120 Ω, see Figure 25
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0		5.0	V	R_L = 100 Ω (RS-422), see Figure 19
		1.5		5.0	V	R_L = 54 Ω (RS-485), see Figure 19
	$\|V_{OD3}\|$	1.5		5.0	V	−7 V ≤ V_{TEST} ≤ +12 V, see Figure 20
Δ$\|V_{OD}\|$ for Complementary Output States	Δ$\|V_{OD}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 19
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 19
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 19
Short-Circuit Output Current	I_{OS}			250	mA	
Output Leakage Current (Y, Z)	I_O			125	µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = 12 V
		−100			µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
Logic Inputs						
Input Threshold Low	V_{IL}	0.25 × V_{DD1}			V	DE, $\overline{RE}$, TxD
Input Threshold High	V_{IH}			0.7 × V_{DD1}	V	DE, $\overline{RE}$, TxD
Input Current	I_I	−10	+0.01	+10	µA	DE, $\overline{RE}$, TxD
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		15		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			125	µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = 12 V
		−125			µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = −7 V
Line Input Resistance	R_{IN}	96			kΩ	−7 V < V_{CM} < +12 V
Logic Outputs						
Output Voltage Low	V_{OLRxD}		0.2	0.4	V	I_{ORxD} = 1.5 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OHRxD}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{ORxD} = −1.5 mA, V_A − V_B = 0.2 V
Short-Circuit Current	I_{OS}			100	mA	
Tristate Output Leakage Current	I_{OZR}			±1	µA	V_{DD1} = 5.0 V, 0 V < V_O < V_{DD1}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
TRANSFORMER DRIVER						
Oscillator Frequency	f_{OSC}	400	500	600	kHz	V_{DD1} = 5.0 V
		230	330	430	kHz	V_{DD1} = 3.3 V
Switch-On Resistance	R_{ON}		0.5	1.5	Ω	
Start-Up Voltage	V_{START}		2.2	2.5	V	
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C, unless otherwise noted.

Table 2. ADM2482E

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Propagation Delay	t_{DPLH}, t_{DPHL}			100	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Output Skew	t_{DSKEW}			8	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Rise Time/Fall Time	t_{DR}, t_{DF}			15	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Enable Time	t_{ZL}, t_{ZH}			120	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 22 and Figure 28
Disable Time	t_{LZ}, t_{HZ}			150	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 22 and Figure 28
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			110	ns	C_L = 15 pF, see Figure 23 and Figure 27
Output Skew	t_{SKEW}			8	ns	C_L = 15 pF, see Figure 23 and Figure 27
Enable Time	t_{ZL}, t_{ZH}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 29
Disable Time	t_{LZ}, t_{HZ}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 29

Table 3. ADM2487E

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Propagation Delay	t_{DPLH}, t_{DPHL}	250		700	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Output Skew	t_{DSKEW}			100	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Rise Time/Fall Time	t_{DR}, t_{DF}	200		1100	ns	R_{DIFF} = 54 Ω, C_L = 100 pF, see Figure 21 and Figure 26
Enable Time	t_{ZL}, t_{ZH}			2.5	µs	R_L = 110 Ω, C_L = 50 pF, see Figure 22 and Figure 28
Disable Time	t_{LZ}, t_{HZ}			200	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 22 and Figure 28
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			200	ns	C_L = 15 pF, see Figure 23 and Figure 27
Output Skew	t_{SKEW}			30	ns	C_L = 15 pF, see Figure 23 and Figure 27
Enable Time	t_{ZL}, t_{ZH}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 29
Disable Time	t_{LZ}, t_{HZ}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 29

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	Thermocouple located at center of package underside

[1] Device considered a 2-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 5. ADM2482E/ADM2487E Approvals

Organization	Approval Type	Notes
UL	Recognized under the component recognition program of underwriters laboratories, Inc.	In accordance with UL 1577, each ADM2482E/ADM2487E is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA)
VDE	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	In accordance with DIN V VDE V 0884-10, each ADM2482E/ADM2487E is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC)

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (External Clearance)	L(I01)	5.15 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	5.5 min	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material group (DIN VDE 0110: 1989-01, Table 1)

VDE 0884-2 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits. An asterisk (*) on packages denotes DIN V VDE V 0884-10 approval.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated				
Mains Voltage				
≤150 V rms			I to IV	
≤300 V rms			I to III	
≤400 V rms			I to II	
Climatic Classification			40/85/21	
Pollution Degree	(DIN VDE 0110: 1989-01, see Table 1)		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage		V_{PR}		
	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m =			
Method b1	1 sec, partial discharge < 5 pC		1050	V peak
Method a:			896	V peak
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC			
Method a			672	V peak
After Input and/or Safety Test, Subgroup 2/3):	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC			
Highest Allowable Overvoltage[1]		V_{TR}	4000	V peak
SAFETY-LIMITING VALUES[2]				
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S[3]		R_S	$>10^9$	Ω

[1] Transient overvoltage, t_{TR} = 10 sec.
[2] The safety-limiting value is the maximum value allowed in the event of a failure. See Figure 3 for the thermal derating curve.
[3] V_{IO} = 500 V.

ABSOLUTE MAXIMUM RATINGS

Each voltage is relative to its respective ground; T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD1}	−0.5 V to +6 V
V_{DD2}	−0.5 V to +6 V
Digital Input Voltages (DE, $\overline{RE}$, TxD)	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltages	
RxD	−0.5 V to V_{DD1} + 0.5 V
D1, D2	13 V
Driver Output/Receiver Input Voltage Range	−9 V to +14 V
Average Output Current per Pin	−35 mA to +35 mA
ESD (Human Body Model) on A, B, Y, and Z pins	±15 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

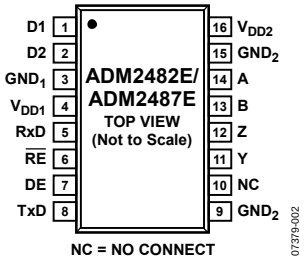

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Transformer Driver Terminal 1.
2	D2	Transformer Driver Terminal 2.
3	GND_1	Ground, Logic Side.
4	V_{DD1}	Power Supply, Logic Side (3.3 V or 5 V). Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
5	RxD	Receiver Output Data. This output is high when (A – B) > +200 mV and low when (A – B) < –200 mV. The output is tristated when the receiver is disabled, that is, when $\overline{RE}$ is driven high.
6	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver; driving it high disables the receiver.
7	DE	Driver Enable Input. Driving this input high enables the driver; driving it low disables the driver.
8	TxD	Transmit Data.
9	GND_2	Ground, Bus Side.
10	NC	No Connect. This pin must be left floating.
11	Y	Driver Noninverting Output.
12	Z	Driver Inverting Output.
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.
15	GND_2	Ground, Bus Side.
16	V_{DD2}	Power Supply, Bus Side (Isolated 3.3 V Supply). Decoupling capacitor to GND_2 required; capacitor value should be between 0.01 µF and 0.1 µF.

TYPICAL PERFORMANCE CHARACTERISTICS

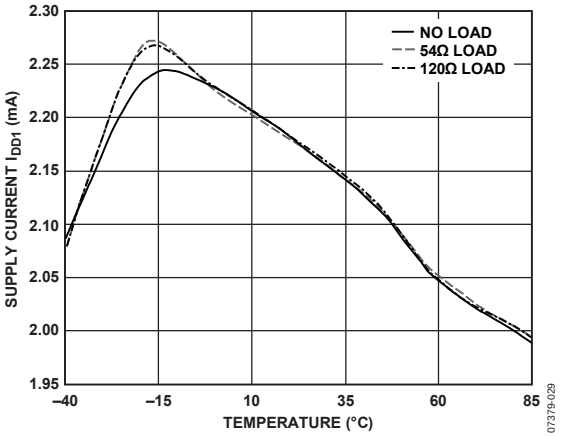

Figure 3. ADM2487E I_{DD1} Supply Current vs. Temperature (Data Rate = 500 kbps, V_{DD1} = 5 V, V_{DD2} = 3.3 V, DE = 1 V, $\overline{RE}$ = 0 V)

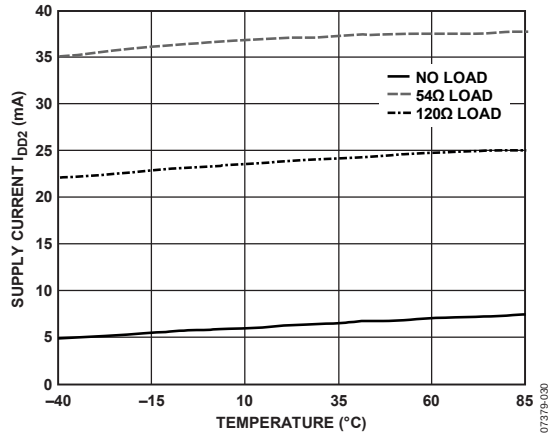

Figure 4. ADM2487E I_{DD2} Supply Current vs. Temperature (See Figure 25) (Data Rate = 500 kbps, V_{DD1} = 5 V, V_{DD2} = 3.3 V, DE = 1 V, $\overline{RE}$ = 0 V)

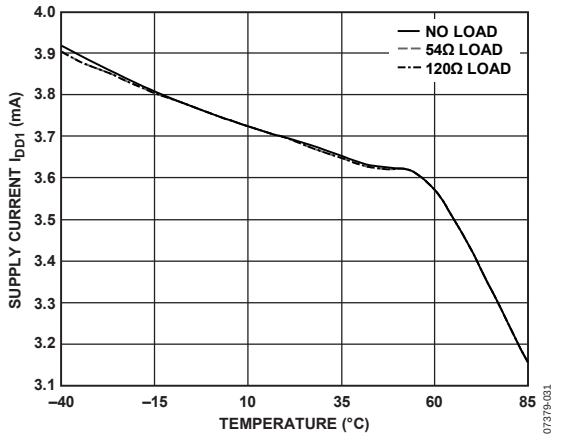

Figure 5. ADM2482E I_{DD1} Supply Current vs. Temperature (Data Rate = 16 Mbps, V_{DD1} = 5 V, V_{DD2} = 3.3 V, DE = 1 V, $\overline{RE}$ = 0 V)

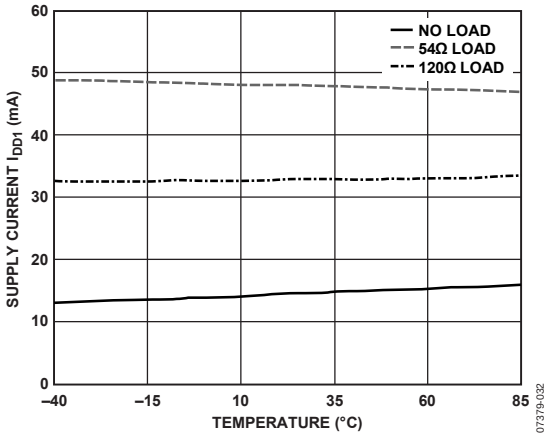

Figure 6. ADM2482E Supply Current vs. Temperature (See Figure 25) (Data Rate = 16 Mbps, V_{DD1} = 5 V, V_{DD2} = 3.3 V, DE = 1, $\overline{RE}$ = 0 V)

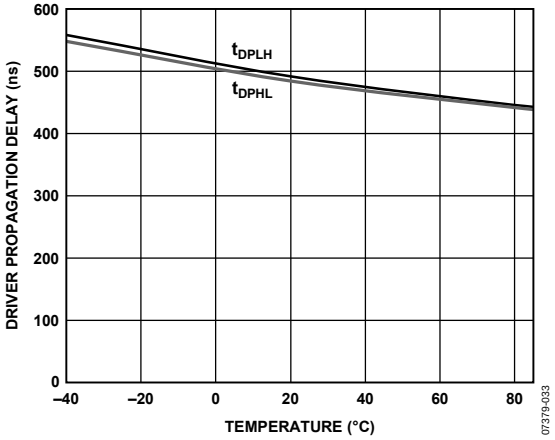

Figure 7. ADM2487E Driver Propagation Delay vs. Temperature

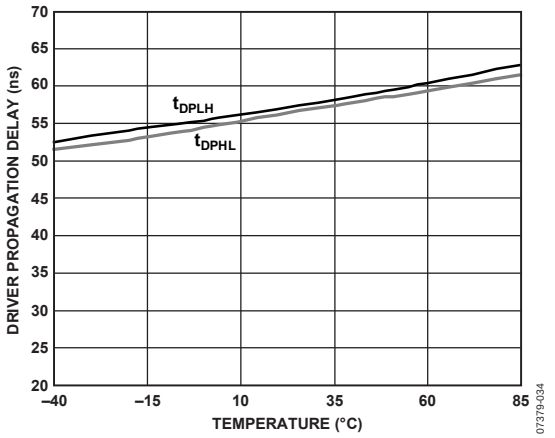

Figure 8. ADM2482E Driver Propagation Delay vs. Temperature

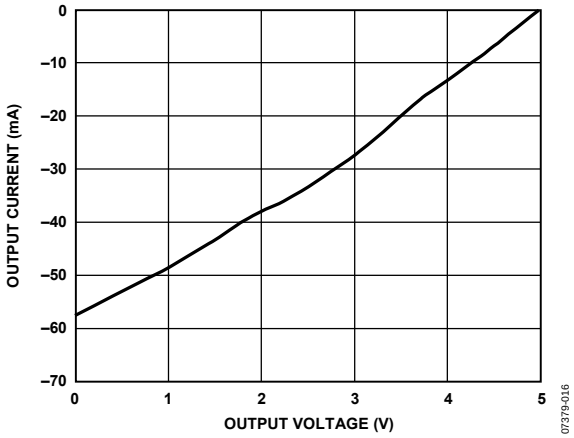

Figure 9. Output Current vs. Receiver Output High Voltage

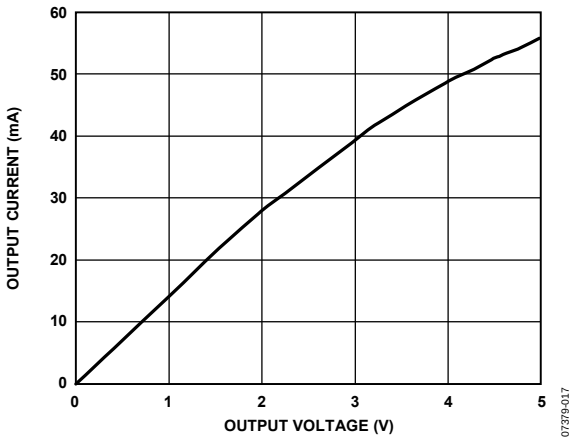

Figure 10. Output Current vs. Receiver Output Low Voltage

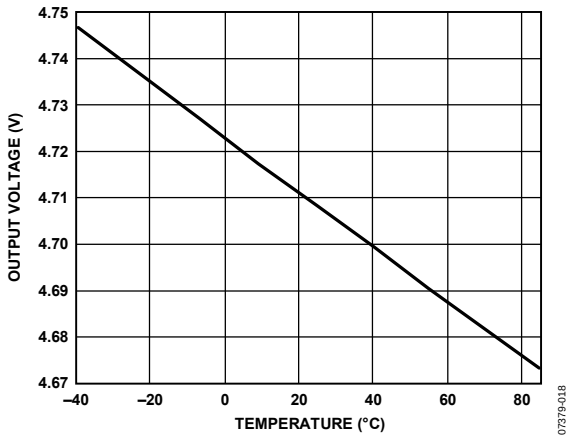

Figure 11. Receiver Output High Voltage vs. Temperature
(I_{DD2} = −4 mA)

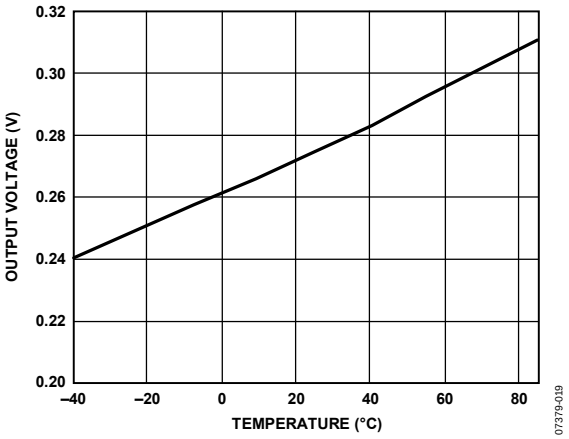

Figure 12. Receiver Output Low Voltage vs. Temperature
(I_{DD2} = 4 mA)

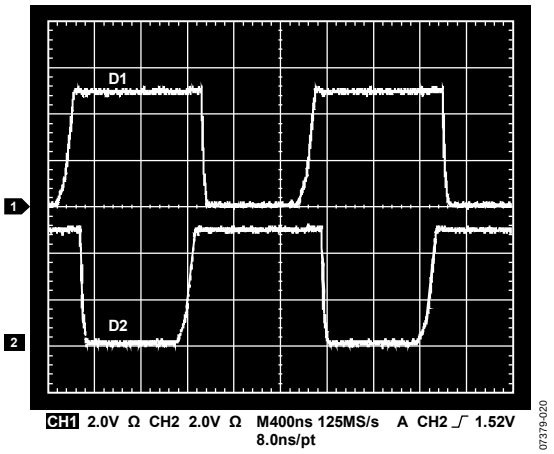

Figure 13. Switching Waveforms
(50 Ω Pull-Up to V_{DD1} on D1 and D2)

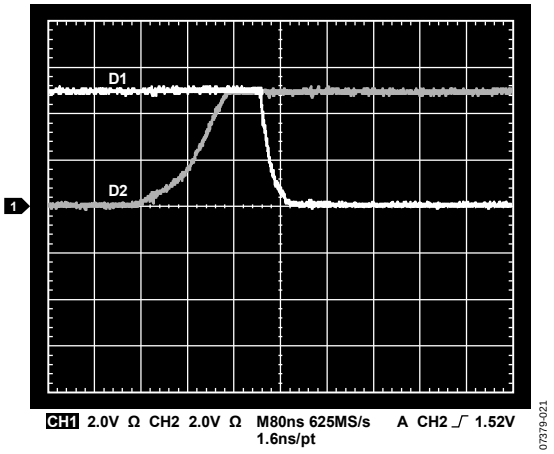

Figure 14. Switching Waveforms
(Break-Before-Make, 50 Ω Pull-Up to V_{DD1} on D1 and D2)

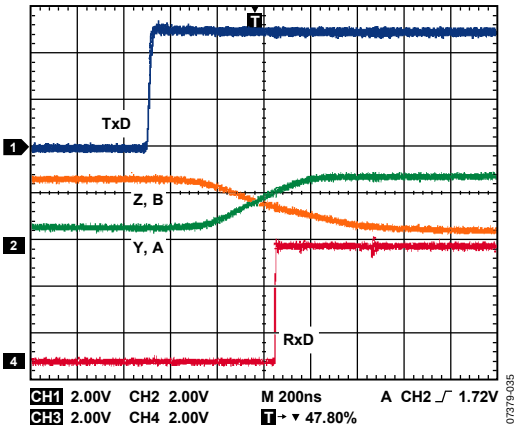

Figure 15. ADM2487E Driver/Receiver Propagation Delay, Low to High (R_{DIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

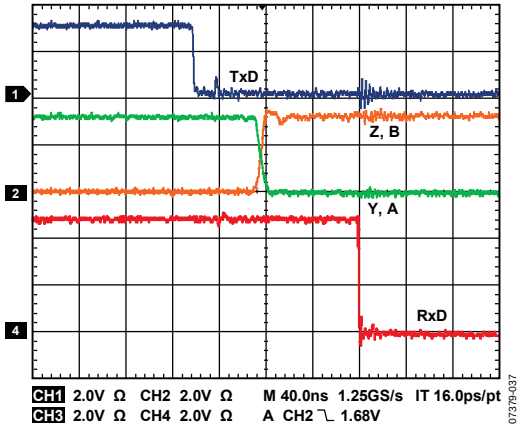

Figure 17. ADM2482E Driver/Receiver Propagation Delay, High to Low (R_{DIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

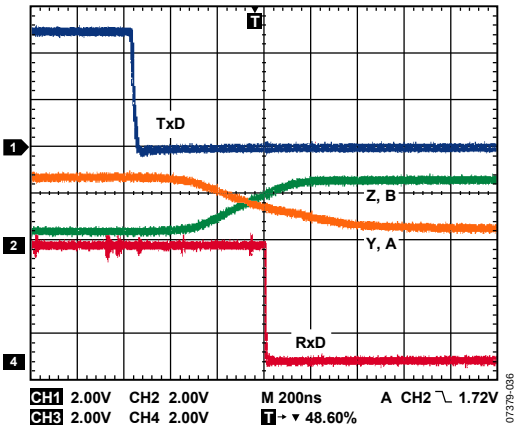

Figure 16. ADM2487E Driver/Receiver Propagation Delay, High to Low (R_{DIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

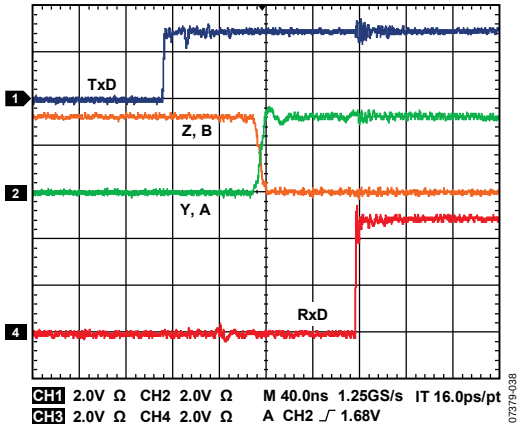

Figure 18. ADM2482E Driver/Receiver Propagation Delay, Low to High (R_{DIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

TEST CIRCUITS

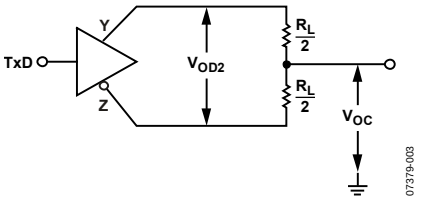

Figure 19. Driver Voltage Measurement

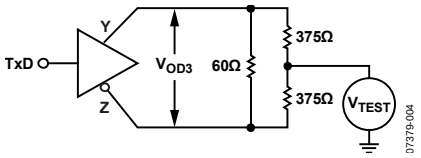

Figure 20. Driver Voltage Measurement

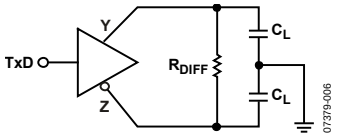

Figure 21. Driver Propagation Delay

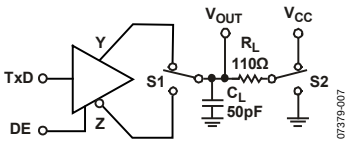

Figure 22. Driver Enable/Disable

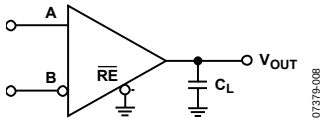

Figure 23. Receiver Propagation Delay

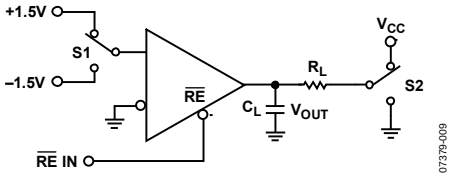

Figure 24. Receiver Enable/Disable

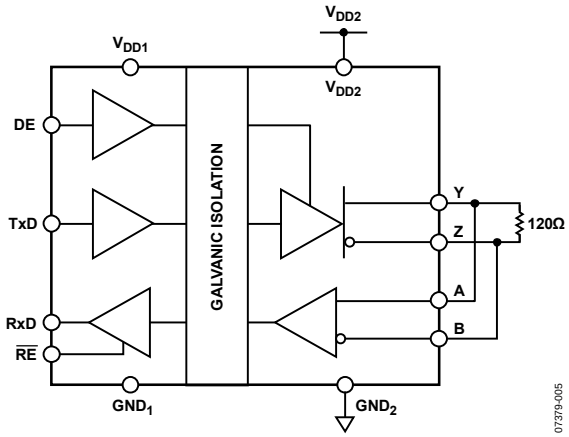

Figure 25. Supply Current Measurement Test Circuit

SWITCHING CHARACTERISTICS

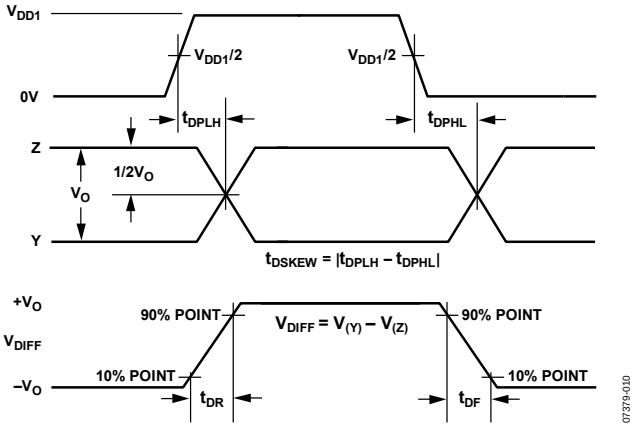

Figure 26. Driver Propagation Delay, Rise/Fall Timing

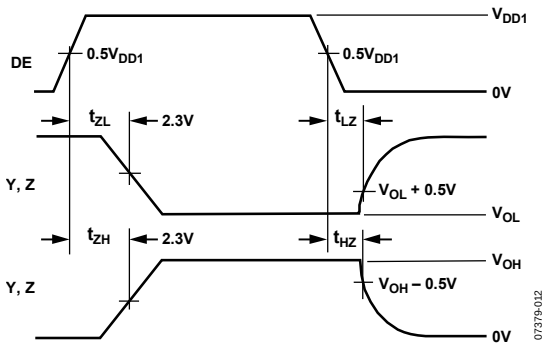

Figure 28. Driver Enable/Disable Timing

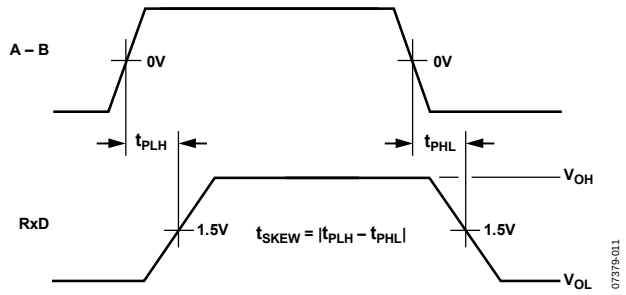

Figure 27. Receiver Propagation Delay

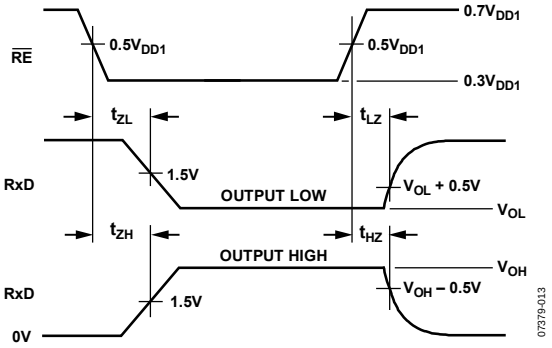

Figure 29. Receiver Enable/Disable Timing

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2482E/ADM2487E, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 30). Driver input and data enable applied to the TxD and DE pins, respectively, and referenced to logic ground (GND_1) are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

*i*Coupler *Technology*

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow pulses (~1 ns) to be sent to the decoder, via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, then the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 10).

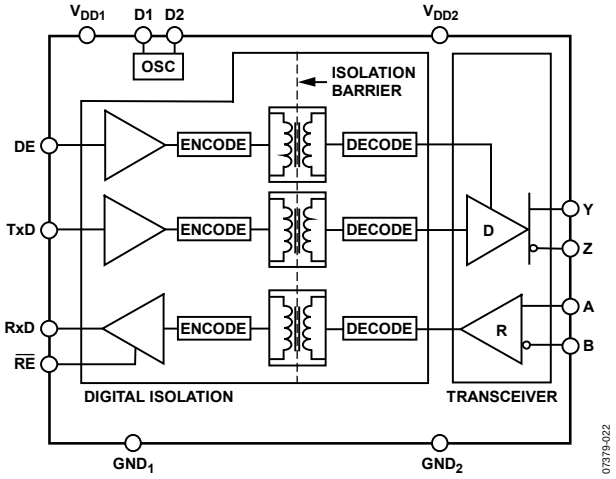

Figure 30. ADM2482E/ADM2487E Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use the abbreviations found in Table 10.

Table 10. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 11. Transmitting

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	Y	Z
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	L	X	Z	Z
Off	Off	X	X	Z	Z

Table 12. Receiving

Supply Status		Inputs		Outputs
V_{DD1}	V_{DD2}	A – B	$\overline{RE}$	RxD
On	On	>−0.03 V	L or NC	H
On	On	<−0.2 V	L or NC	L
On	On	−0.2 V < A – B < −0.03 V	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2482E/ADM2487E contain thermal shutdown circuitry that protects the parts from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

TRUE FAIL-SAFE RECEIVER INPUTS

The receiver inputs have a true fail-safe feature that ensures that the receiver output is high when the inputs are open or shorted. During line idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistance at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between −200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between −30 mV and −200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V, the receiver output is guaranteed to be high.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the *i*Coupler is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM2482E/ADM2487E is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 31.

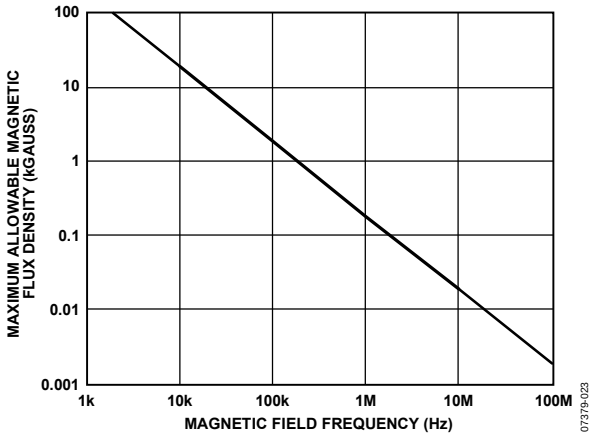

Figure 31. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 32 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM2482E/ADM2487E transformers.

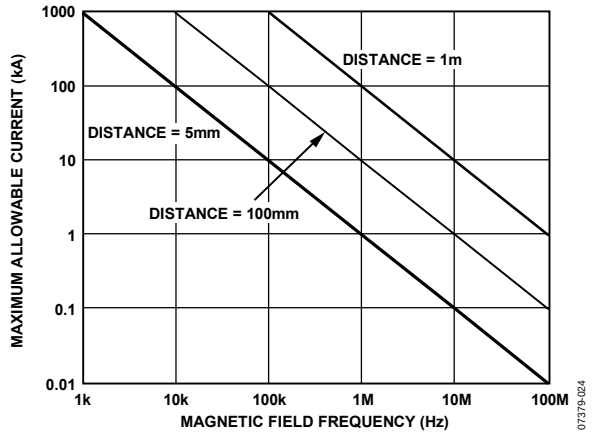

Figure 32. Maximum Allowable Current for Various Current-to-ADM2482E/ADM2487E Spacings

With combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry.

Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The isolated RS-485 transceiver of the ADM2482E/ADM2487E requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 33).

Bypass capacitors are most conveniently connected between Pin 3 and Pin 4 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value must be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

Bypassing Pin 9 and Pin 16 is also recommended unless the ground pair on each package side is connected close to the package.

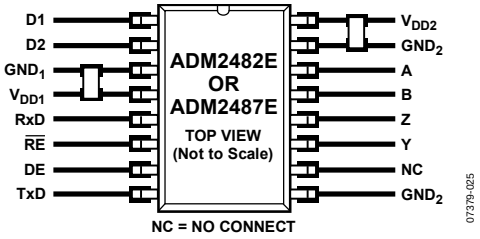

Figure 33. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care must be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout must be designed such that any coupling that does occur equally affects all pins on a given component side.

Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

TRANSFORMER SUPPLIERS

The transformer primarily used with the ADM2482E/ADM2487E must be a center-tapped transformer winding. The turns ratio of the transformer must be set to provide the minimum required output voltage at the maximum anticipated load with the minimum input voltage. Table 13 shows ADM2482E/ADM2487E transformer suppliers.

Table 13. Transformer Supplies

Manufacturer	Primary Voltage 3.3 V	Primary Voltage 5 V
Coilcraft	DA2303-AL	GA3157
Murata	782482/33VC	782482/53VC

ISOLATED POWER SUPPLY CIRCUIT

The ADM2482E/ADM2487E integrate a transformer driver that, when used with an external transformer and linear voltage regulator (LDO), generates an isolated 3.3 V power supply to be supplied between V_{DD2} and GND_2, as shown in Figure 34.

Pin D1 and Pin D2 of the ADM2482E/ADM2487E drive a center-tapped Transformer T1. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 LDO provides a regulated 3.3 V power supply to the ADM2482E/ADM2487E bus side circuitry (V_{DD2}).

When the ADM2482E/ADM2487E are powered by 3.3 V on the logic side, a step-up transformer is required to compensate for the forward voltage drop of the Schottky diodes and the voltage drop across the regulator. The transformer turns ratio should be chosen to ensure just enough headroom for the ADP3330 LDO to output a regulated 3.3 V output under all operating conditions.

If the ADM2482E/ADM2487E are powered by 5 V on the logic side, then a step-down transformer should be used. For optimum efficiency, the transformer turns ratio should be chosen to ensure just enough headroom for the ADP3330 LDO to output a regulated 3.3 V output under all operating conditions.

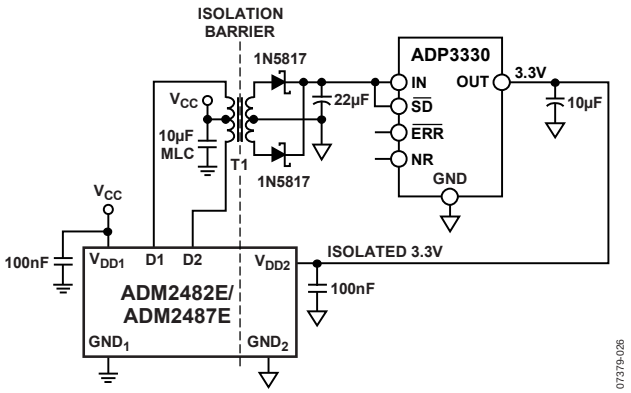

Figure 34. Applications Diagram

TYPICAL APPLICATIONS

Figure 35 and Figure 36 show typical applications of the ADM2482E/ADM2487E in half-duplex and full-duplex RS-485 network configurations. Up to 256 transceivers can be connected to the RS-485 bus. To minimize reflections, the line must be terminated at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. For a half-duplex operation, this means that both ends of the line must be terminated, because either end can be the receiving end.

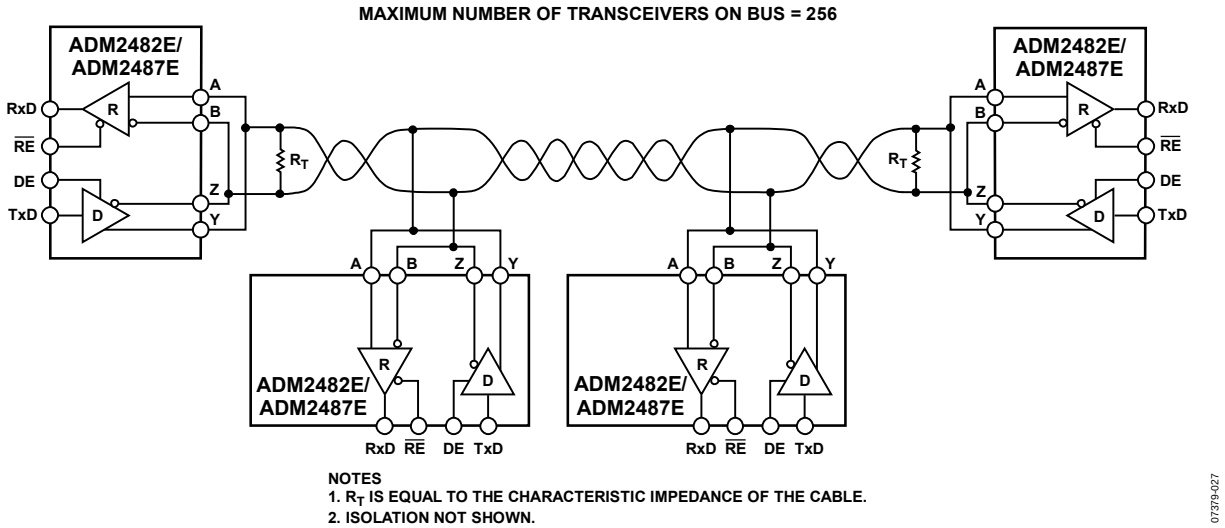

Figure 35. ADM2482E/ADM2487E Typical Half-Duplex RS-485 Network

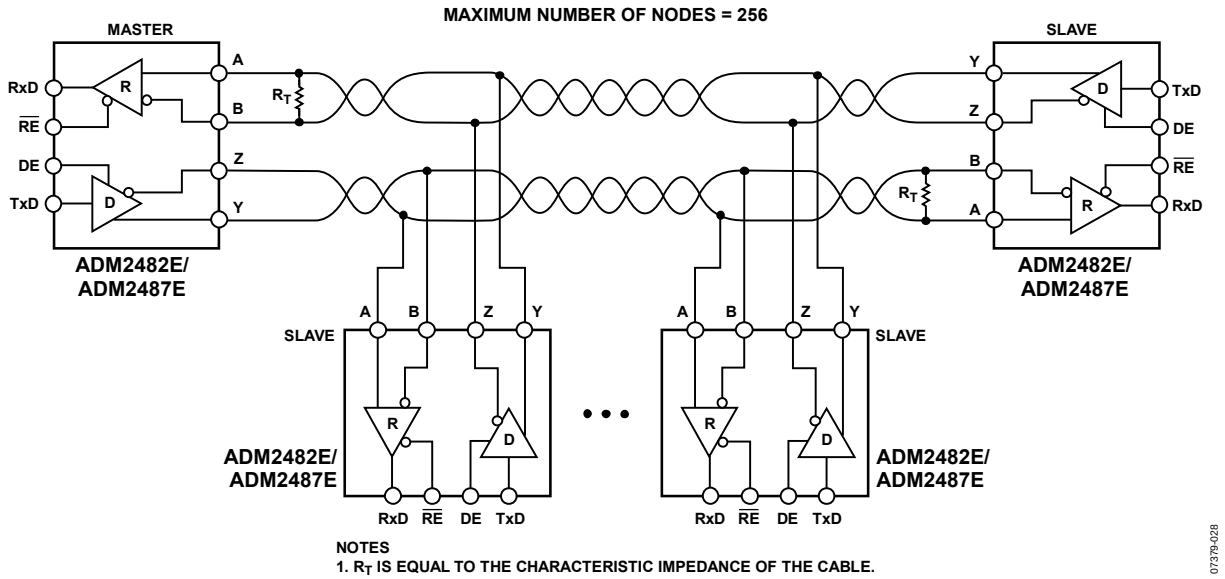

Figure 36. ADM2482E/ADM2487E Typical Full-Duplex RS-485 Network

OUTLINE DIMENSIONS

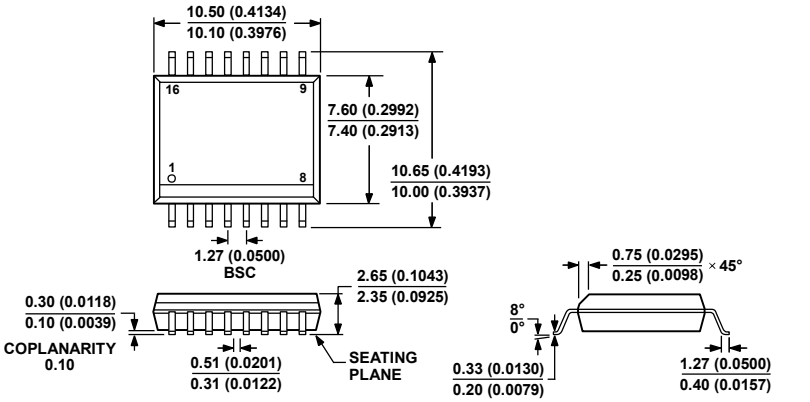

Figure 37. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2482EBRWZ[1]	16	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM2482EBRWZ-REEL7[1]	16	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM2487EBRWZ[1]	0.5	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM2487EBRWZ-REEL7[1]	0.5	−40°C to +85°C	16-Lead SOIC_W	RW-16
EVAL-ADM2482EEB3Z			Evaluation Board, 3.3 V Supply	
EVAL2482EEB5Z			Evaluation Board, 5 V Supply	
EVAL-ADM2487EEB3Z			Evaluation Board, 3.3 V Supply	
EVAL2487EEB5Z			Evaluation Board, 5 V Supply	

[1] Z = RoHS Compliant Part.

NOTES

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