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Intersil
ISL8510IRZ

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Data Sheet | December 15, 2008 | FN6516.2

Dual Output Controller with 1A Standard Buck PWM and LDO

The ISL8510 is a high-performance, dual output controller that provides a single, high frequency power solution for a variety of point of load applications. The ISL8510 integrates a 1A standard buck PWM controller and switching MOSFET with one 500mA LDO.

The PWM controller in the ISL8510 drives an internal switching N-Channel power MOSFET and requires an external Schottky diode to generate an output voltage from 0.6V to 20V. The integrated power switch is optimized for excellent thermal performance up to 1A of output current. The standard buck input voltage range supports a fixed 5V or variable 5.5V to 25V range. The PWM regulator switches at a fixed frequency of 500kHz and utilizes simple voltage mode control with input voltage feed forward to provide flexibility in component selection and minimize solution size. Protection features include overcurrent, undervoltage, and thermal overload protection integrated into the IC. The ISL8510 power-good signal output indicates loss of regulation on the PWM output.

The ISL8510 features one adjustable LDO regulator using internal PMOS transistors as pass devices. The enable pin (EN_LDO) controls the LDO output. A single power-good signal output indicates loss of regulation on the LDO output. Independent overcurrent and thermal fault shutdown monitors are integrated into the “LDO Regulator Capacitor Selection” on page 16.

The ISL8510 is available in a small 4mmx4mm Quad Flat No Lead (QFN) package.

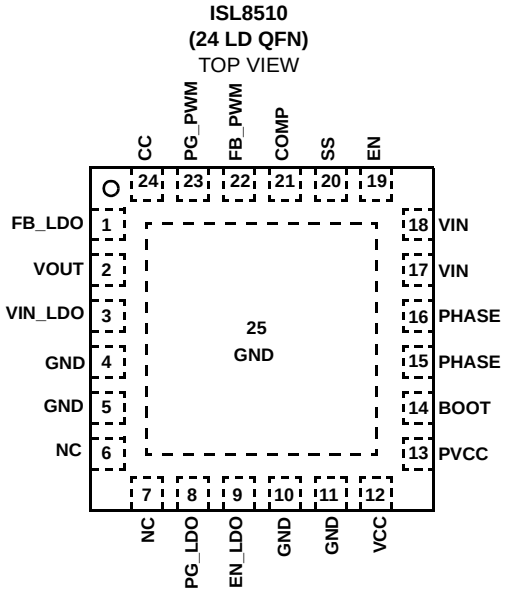
Features

- Standard Buck Controller with Integrated Switching Power MOSFET + 1 LDO
- Integrated Boot Diode
- Input Voltage Range
  - Fixed 5V ±10%
  - Variable 5.5V to 25V
- PWM Output Voltage Adjustable from 0.6V to 20V with Continuous Output Current up to 1A
- Voltage Mode Control with Voltage Feed Forward
- Fixed 500kHz Switching Frequency
- Externally Adjustable Soft-Start Time
- Output Undervoltage Protection
- LDO Adjustable Options
  - LDO, 0.6V to 4.2V 500mA
- Individual Enable Inputs
- Two PGOOD Outputs (PWM and LDO)
- Overcurrent Protection
- Thermal Overload Protection
- Internal 5V LDO regulator
- Pb-Free (RoHS Compliant)

Applications

- General Purpose
- WLAN Cards-PCMCIA, Cardbus32, MiniPCI Cards-Compact Flash Cards
- Hand-Held Instruments

Pinout



Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8510IRZ*	85 10IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Schematics

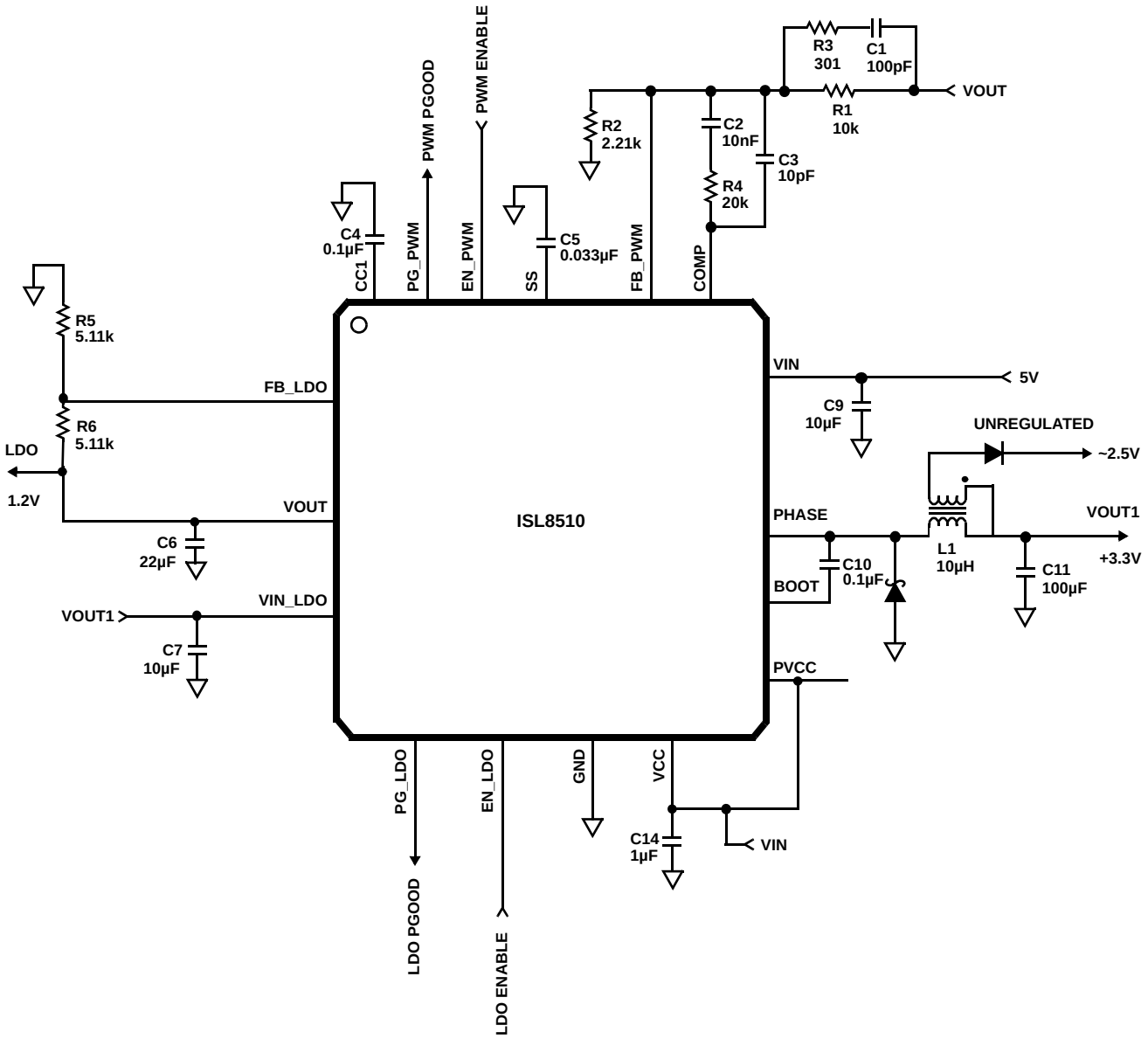


FIGURE 1. V_{IN} RANGE FROM 4.5V TO 5.5V

Typical Application Schematics (Continued)

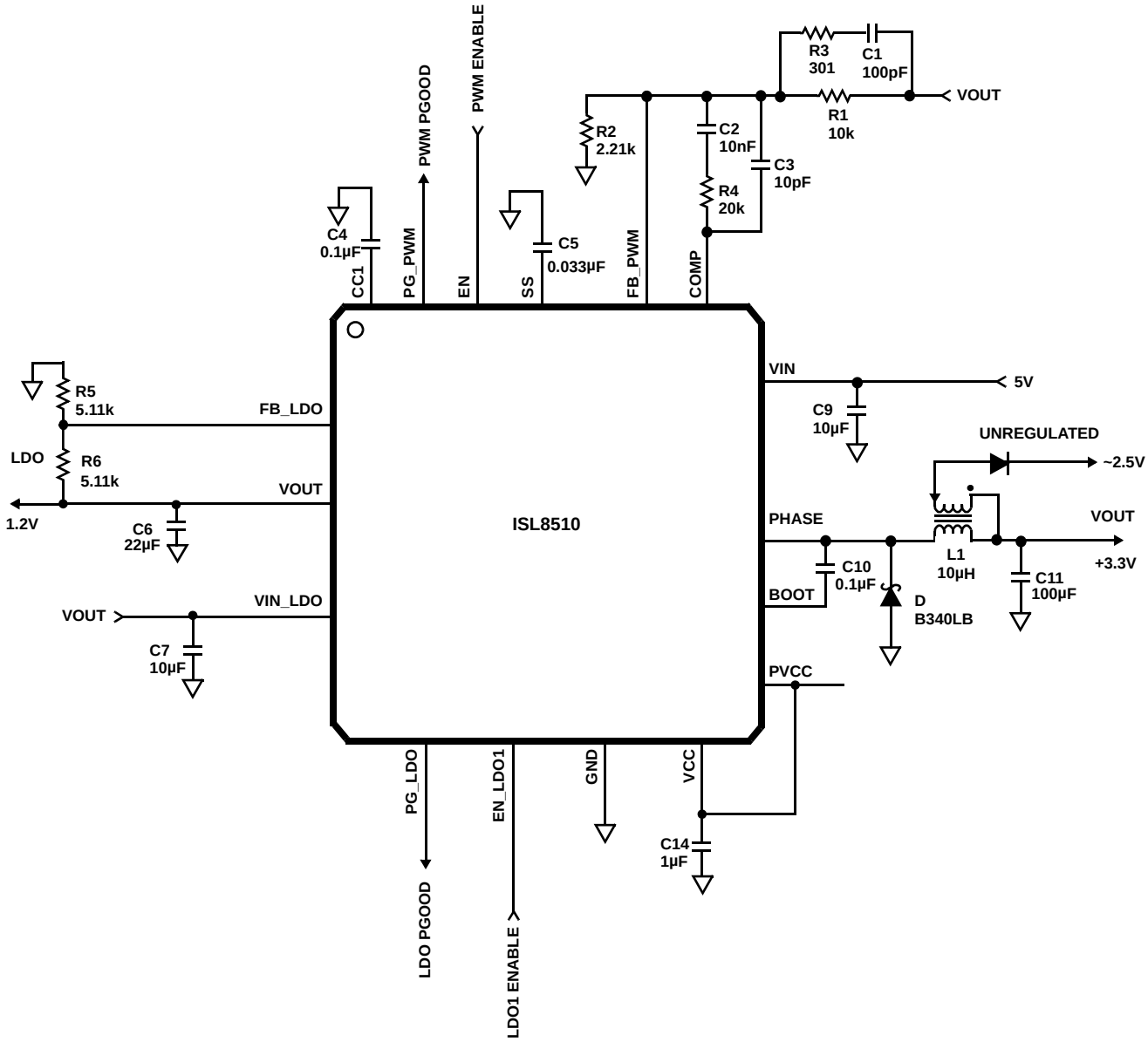
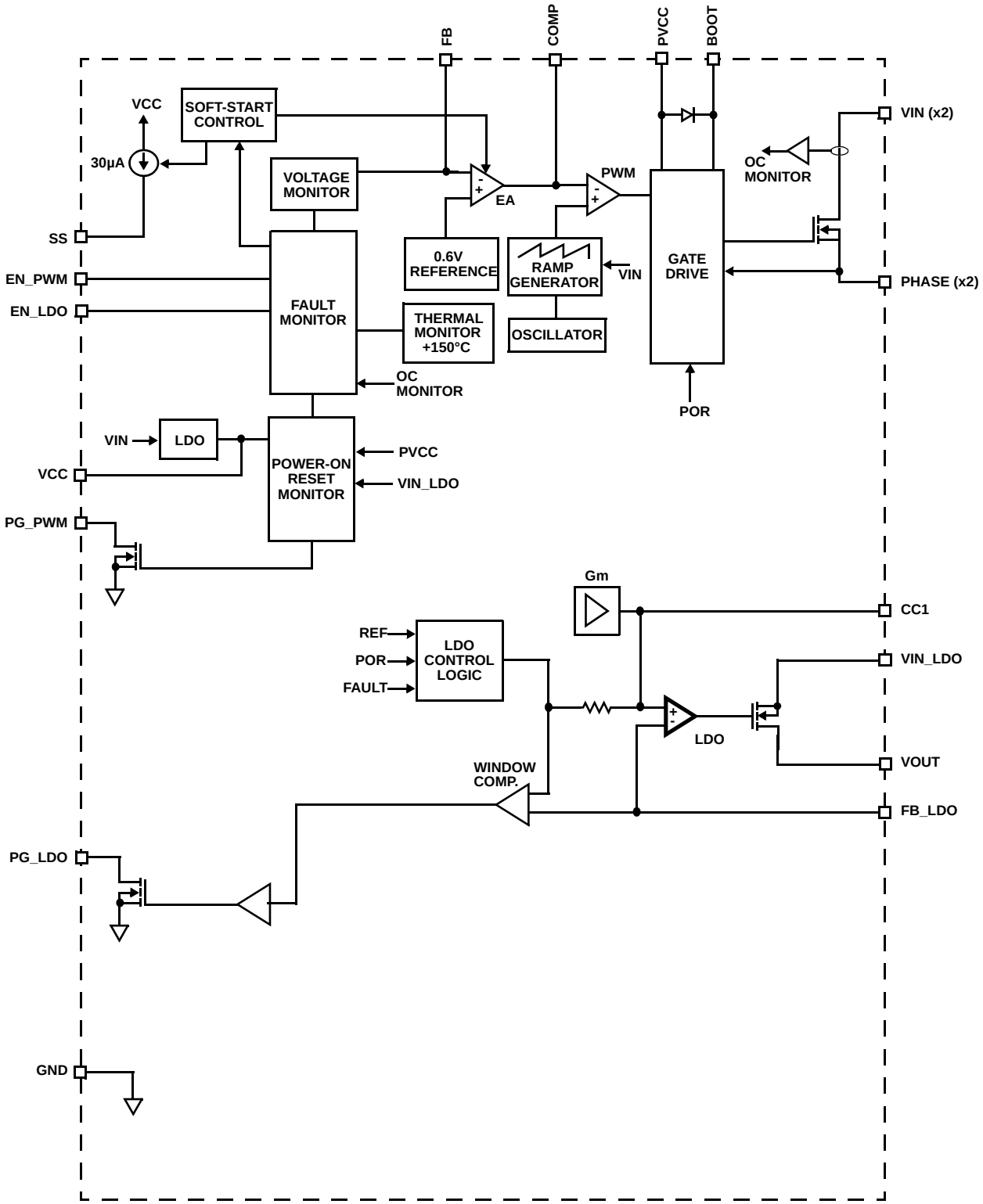


FIGURE 2. V_{IN} RANGE FROM 5.5V TO 25V

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

VIN to GND . . . . . GND -0.3V to +26V
VIN_LDO to GND. . . . . GND -0.3V to +6V
BOOT to GND . . . . . GND -0.3V to +33V
PHASE to BOOT . . . . . -6V to +0.3V
VCC to GND . . . . . GND -0.3V to +6V
VOUT, LDO . . . . . GND -0.3V to +6V
FB_PWM, FB_LDO to GND. . . . . GND -0.3V to +6V
PG_PWM, PG_LDO to GND . . . . . GND -0.3V to +6V
EN, EN_LDO to GND. . . . . GND -0.3V to +6V
CC to GND. . . . . GND -0.3V to +6V
VCC Output Current. 50mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 2, 3).	36	5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Ambient Temperature Range. . . . . -40°C to +85°C
Junction Temperature Range. . . . . -40°C to +125°C
Pb-free Reflow Profile . . . . . See Link Below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. An accidental short between VCC and GND may cause excessive heating and permanent damage to the device.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless Otherwise Noted, Typical Specifications are Measured at the Following Conditions: T_A = +25°C, V_{IN} = 6V to 25V. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
VIN Voltage Range	VIN		5.5		25	V
		VIN connected to VCC	4.5	5.0	5.5	V
VIN_LDO Voltage Range		(Note 7)	1.8		4.6	V
VIN Operating Supply Current	I_{OP}	(Note 4)		2.5	3.5	mA
VIN Shutdown Supply Current	I_{SD}	EN_PWM = EN_LDO = GND		70	100	µA
POWER-ON RESET						
VCC POR Threshold		Rising Edge	4.25	4.40	4.50	V
		Hysteresis		260		mV
VIN_LDO POR Threshold		Rising Edge		1.2		V
		Hysteresis		200		mV
INTERNAL VCC LDO						
VCC Output Voltage Range		V_{IN} = 6V to 25V, I_{VCC} = 0mA to 50mA	4.5	5.00	5.5	V
REFERENCE						
Reference Voltage	V_{FB}	V_{IN} = 6V to 25V, I_{REF} = 0	0.590	0.6	0.609	V
STANDARD BUCK PWM REGULATOR						
FB_PWM Line Regulation		I_{OUT} = 0mA, V_{IN} = 6V to 25V	-0.5		0.5	%
OSCILLATOR and PWM MODULATOR						
Nominal Switching Frequency	f_{SW}	T_A = -40°C to +85°C, V_{CC} = 5V	450	500	550	kHz
Modulator Gain	A_{MOD}	V_{IN} = 12V (A_{MOD} = 10/V_{IN})	0.73	0.86	0.99	V/V
Peak-to-Peak Sawtooth Amplitude	V_{RAMP}	V_{IN} = 12V (V_{P-P} = V_{IN}/10)		1.2		V
PWM Ramp Offset Voltage	V_{OFFSET}		0.70	0.8	0.91	V
Maximum Duty Cycle	DC_{MAX}	COMP >4V	80	83		%
ERROR AMPLIFIER						
Open-Loop Gain				88		dB
Gain Bandwidth Product	GBWP			15		MHz
Slew Rate	SR	COMP = 10pF		5		V/µs

Electrical Specifications

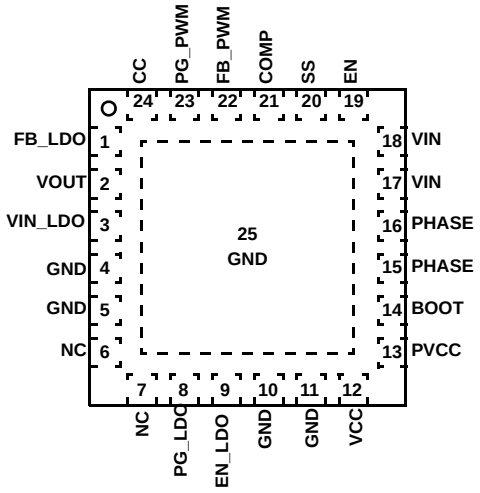
Unless Otherwise Noted, Typical Specifications are Measured at the Following Conditions: T_A = +25°C, V_{IN} = 6V to 25V. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE SECTION						
EN_PWM Threshold		Rising Edge	1.2	1.7	2.2	V
		Hysteresis		350		mV
EN_LDO Logic Input Threshold		Rising Edge	1.2	1.7	2.2	V
		Hysteresis		400		mV
EN_LDO Logic Input Current			-1		1	µA
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		150		°C
	T_{HYS}	Hysteresis		15		°C
PWM UV Trip Level	V_{UV}	Referred to Nominal VOUT	65	70	75	%
PWM UVP Propagation Delay				360		ns
PWM OCP Threshold		(Note 5)	1.85	2.70	3.00	A
OCP Blanking Time				150		ns
POWER-GOOD						
PG_PWM Trip Level Referred to Nominal VOUT		Falling Edge, 15mV Hysteresis	84	88	92	%
		Rising Edge, 15mV Hysteresis	107	110	113	%
PG_PWM and PG_LDO Propagation Delay				160		ns
PG_PWM Low Voltage		ISINK = 4mA			0.3	V
PG_PWM Leakage Current		V_{PG_PWM} = 5.5V, V_{FB_PWM} = 0.6V	-1		1	µA
PG_LDO Trip Level Referred to Nominal VOUT		Lower Level, Falling Edge, 15mV Hysteresis	81	85	88	%
PG_LDO Low Voltage		ISINK = 4mA			0.3	V
PG_LDO Leakage Current		V_{PG_LDO} = 5V, V_{FB_LDO} = 600mV	-1		1	µA
SOFT-START SECTION						
Soft-Start Threshold			0.8	1.0	1.2	V
Soft-Start Threshold to Enable PG			2.8	2.95	3.1	V
Soft-Start Voltage High				3.3		V
Soft-Start Charging Current			25	30	35	µA
Soft-Start Pull-down		V_{SS} = 3.0V		25		mA
POWER MOSFET						
$r_{DS(ON)}$		I_{OUT} = 100mA		120	350	mΩ
LDO						
FB_LDO Voltage Accuracy		I_{OUT} = 10mA	-1.5		1.5	%
FB Leakage Current		V_{FB} = 0V	-200	-80		nA
Output Current Limit			550	800	1000	mA
Dropout Voltage		I_{OUT} = 450mA, V_{OUT} >2V (Note 6)		150	300	mV
FB_LDO Line Regulation		I_{OUT} = 0mA, VIN_LDO = 2.0V ~ 4.6V	-0.6		0.6	%/V
FB_LDO Load Regulation		I_{OUT} = 10mA to 500mA		±0.5		%

NOTES:

4. Test Condition: V_{IN} = 15V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
5. Limits established by characterization and are not production tested.
6. The dropout voltage is defined as minimum amount V_{IN} must exceed a desired V_{OUT} operating point. $V_{LDO} = V_{IN\_LDO} - V_{OUT}$.
7. The input voltage V_{CC} must be higher than V_{IN_LDO} or the LDO will not function.

Pin Descriptions



VIN

The input supply for the PWM regulator power stage and the source for the internal linear regulator that provides bias for the IC. Place a ceramic capacitor from VIN to GND close to the IC for decoupling (typical 1µF).

PVCC

Connect this pin to VCC.

GND

Ground connect for the IC and thermal relief for the package. The exposed pad must be connected to GND and soldered to the PCB. All voltage levels are measured with respect to this pin.

VCC

Internal 5V linear regulator output provides bias to all the internal control logic. The ISL8510 may be powered directly from a 5V (±10%) supply at this pin. When used as a 5V supply input, this pin must be externally connected to VIN. The VCC pin must always be decoupled to GND with a ceramic bypass capacitor (minimum 1µF) located close to the pin.

TABLE 1. INPUT SUPPLY CONFIGURATION

INPUT	PIN CONFIGURATION
5.5V to 25V	Connect the input supply to the VIN pin only. The VCC pin will provide a 5V output from the internal linear regulator.
5V ±10%	Connect the input supply to the VIN and VCC pins.

FB _PWM AND COMP

The standard buck regulator employs a single voltage control loop. FB_PWM is the negative input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB_PWM. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. Connecting an AC network across COMP and FB_PWM provides loop compensation to the amplifier.

In addition, the PWM regulator power-good and undervoltage protection circuitry use FB_PWM to monitor the regulator output voltage.

PHASE

Switch node connections to internal power MOSFET source, external output inductor, and external diode cathode.

BOOT

Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn and hold on the internal N-Channel MOSFET. Connect an external capacitor from this pin to PHASE.

EN

PWM controller enable input. The PWM converter and LDO's outputs are held off when the pin is pulled to ground. When the voltage on this pin is logic high, the chip is enabled.

SS

Program pin for soft-start duration. A regulated 30µA pull-up current source charges a capacitor connected from the pin to GND. The output voltage of the converter follows the ramping voltage on the SS pin.

VIN_LDO

Input voltage pin for LDO.

VOUT

LDO output pin. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

FB_LDO

Used to set the output of LDO with the proper selection of resistor divider. The resistors should be selected to provide a minimum current of 200nA load for the LDO.

CC

Compensation capacitor connection for LDO. Connect a 0.033µF capacitor from pin to ground.

EN_LDO

The pin is threshold-sensitive enable input for the LDO. Held low, this pin disables LDO.

PG_PWM

PWM converter power-good output. Open drain logic output that is pulled to ground when the output voltage is outside regulation limits. Connect a 100kΩ resistor from this pin to VCC. Pin is low when the buck regulator output voltage is not within 10% of the respective nominal voltage, or during the soft-start interval. Pin is high impedance when the output is within regulation.

PG_LDO

Combined LDO power--good output. Connect a 100kΩ resistor from this pin to VCC.

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, VIN_LDO = V_{OUT} = 3.3V, I_{OUT} = 1A, VLDO = 1.2V, I_{LDO} = 450mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

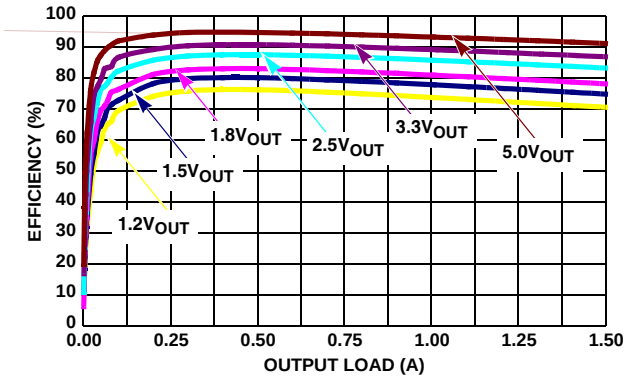


FIGURE 3. EFFICIENCY vs LOAD, V_{IN} = 7V

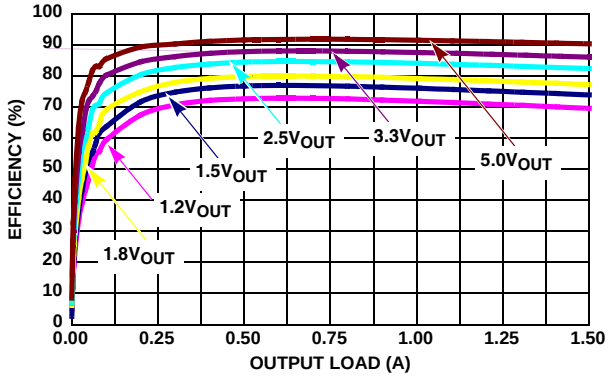


FIGURE 4. EFFICIENCY vs LOAD, V_{IN} = 12V

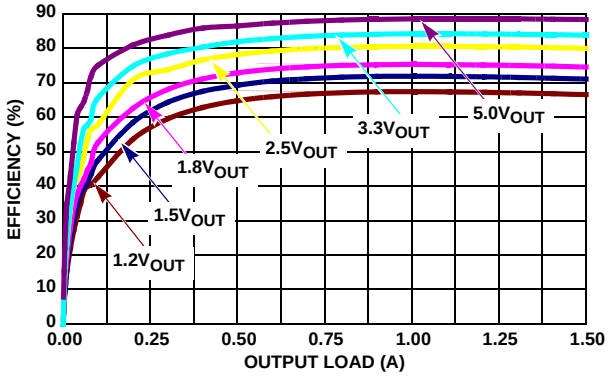


FIGURE 5. EFFICIENCY vs LOAD, V_{IN} = 25V

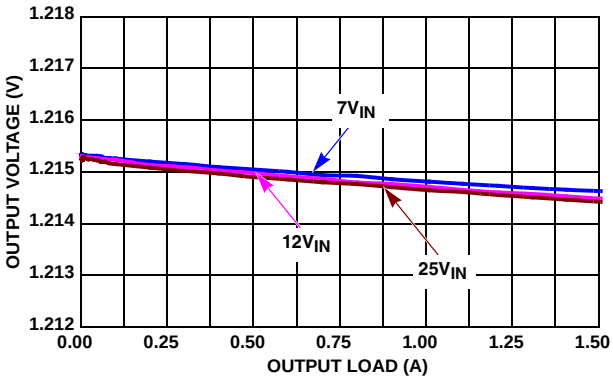


FIGURE 6. V_{OUT} REGULATION vs LOAD, 500kHz 1.2V_{OUT}

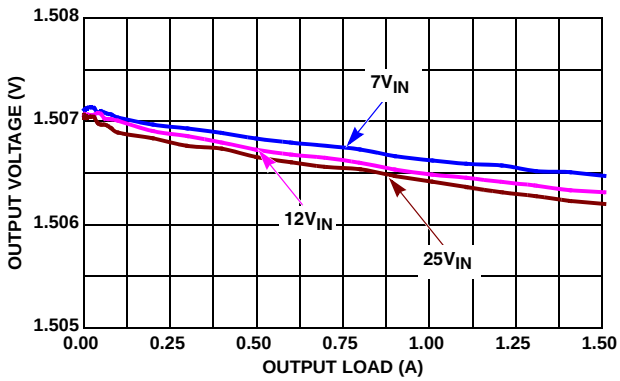


FIGURE 7. V_{OUT} REGULATION vs LOAD, 500kHz 1.2V_{OUT}

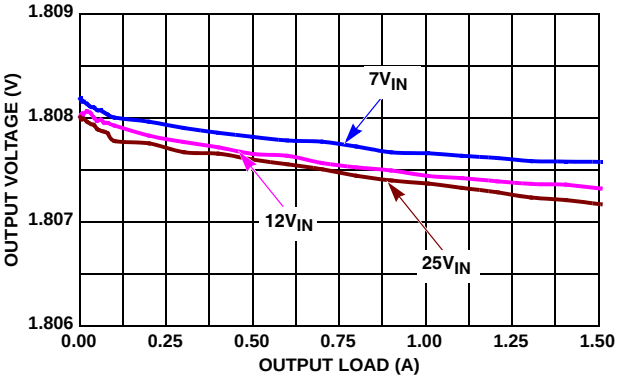


FIGURE 8. V_{OUT} REGULATION vs LOAD, 500kHz 1.8V_{OUT}

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, VIN_LDO = V_{OUT} = 3.3V, I_{OUT} = 1A, VLDO = 1.2V, I_{LDO} = 450mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

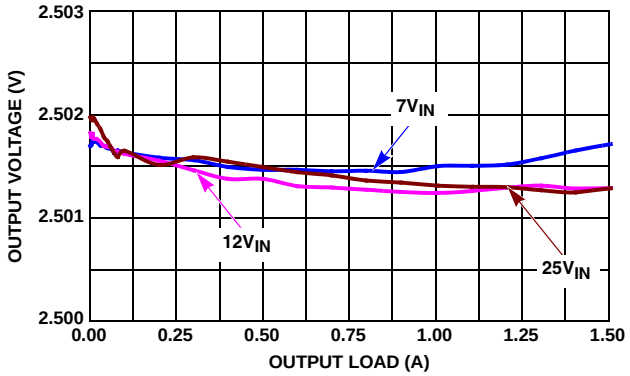


FIGURE 9. V_{OUT} REGULATION vs LOAD, 500kHz 2.5V_{OUT}

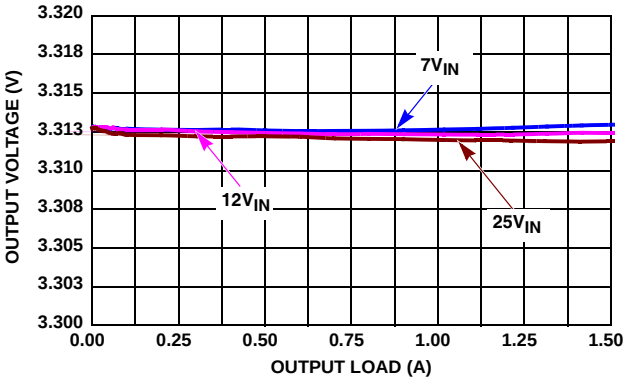


FIGURE 10. V_{OUT} REGULATION vs LOAD, 500kHz 3.3V_{OUT}

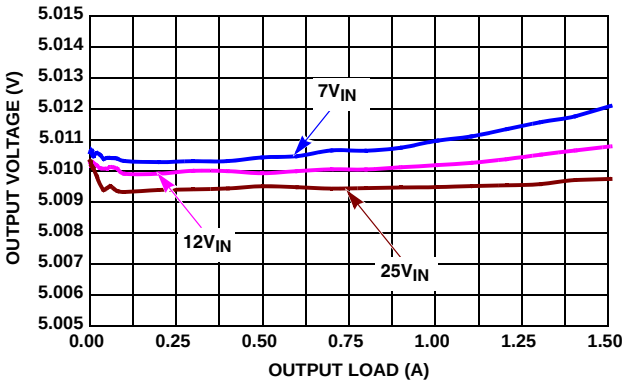


FIGURE 11. V_{OUT} REGULATION vs LOAD, 5V_{OUT}

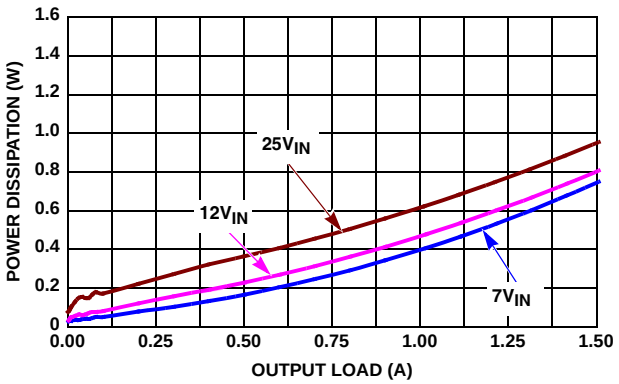


FIGURE 12. POWER DISSIPATION vs LOAD, 3.3V_{OUT}

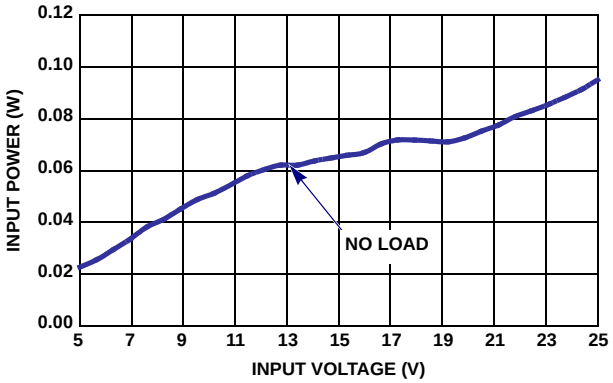


FIGURE 13. INPUT POWER vs V_{IN}, V_{OUT} = 3.3V

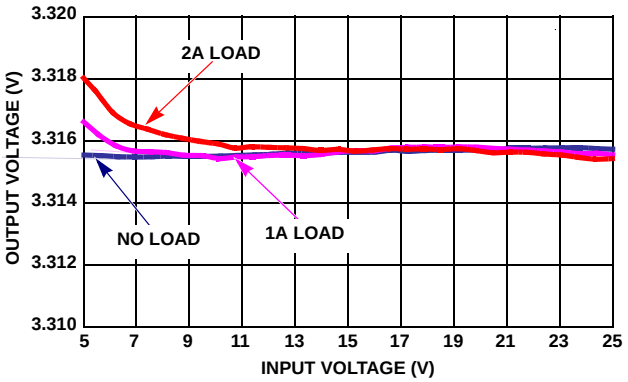


FIGURE 14. OUTPUT VOLTAGE REGULATION vs V_{IN}

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, VIN_LDO = V_{OUT} = 3.3V, I_{OUT} = 1A, VLDO = 1.2V, I_{LDO} = 450mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

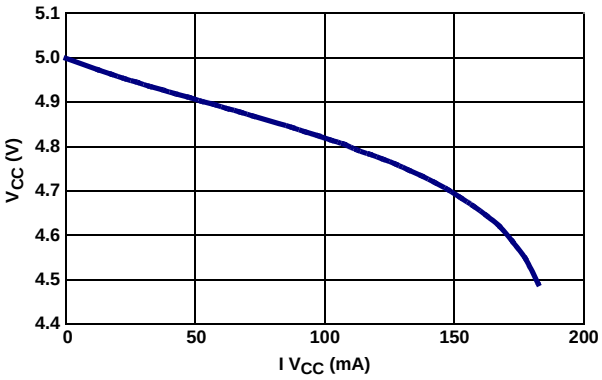


FIGURE 15. V_{CC} LOAD REGULATION

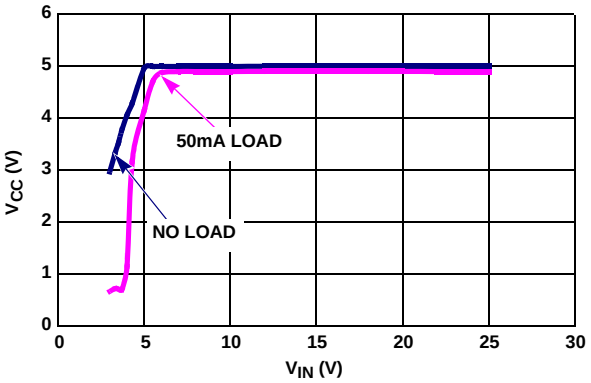


FIGURE 16. V_{CC} REGULATION WITH V_{IN}

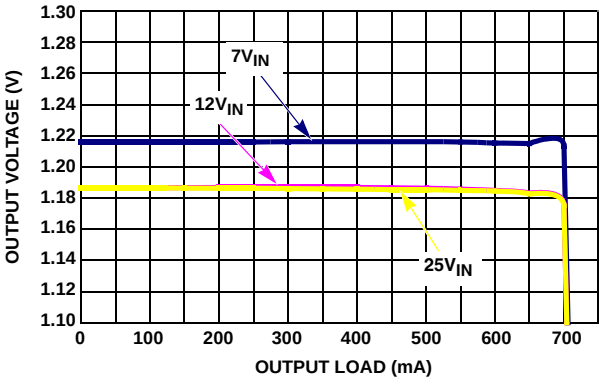


FIGURE 17. LDO vs LOAD, 500kHz, V_{IN} LDO = 3.3V

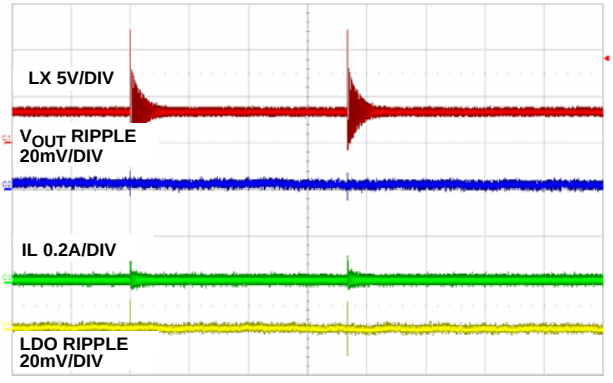


FIGURE 18. STEADY STATE OPERATION AT NO LOAD, 20µs/DIV

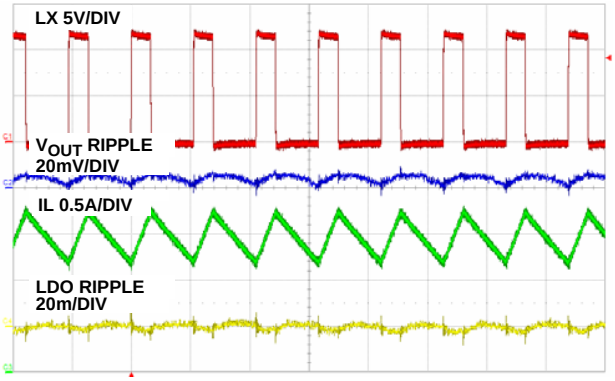


FIGURE 19. STEADY STATE OPERATION AT FULL LOAD, 2µs/DIV

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, VIN_LDO = V_{OUT} = 3.3V, I_{OUT} = 1A, VLDO = 1.2V, I_{LDO} = 450mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

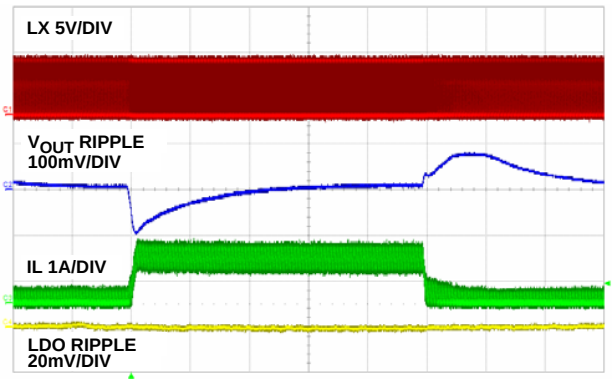


FIGURE 20. LOAD TRANSIENT, 200µs/DIV

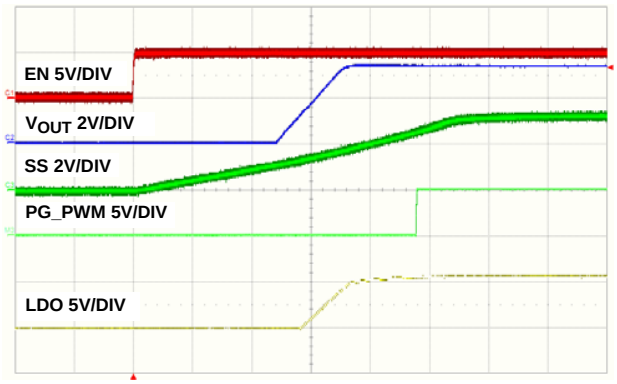


FIGURE 21. SOFT-START AT NO LOAD, 500µs/DIV

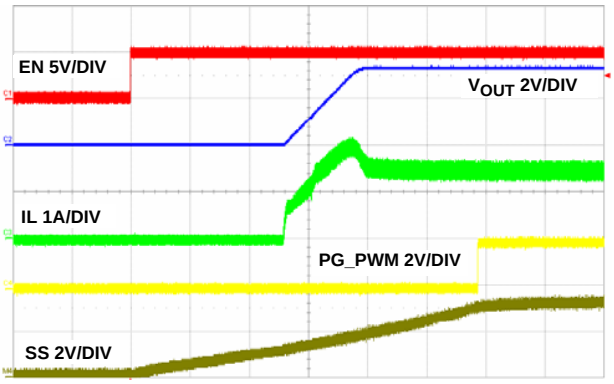


FIGURE 22. SOFT-START AT FULL LOAD, 500µs/DIV

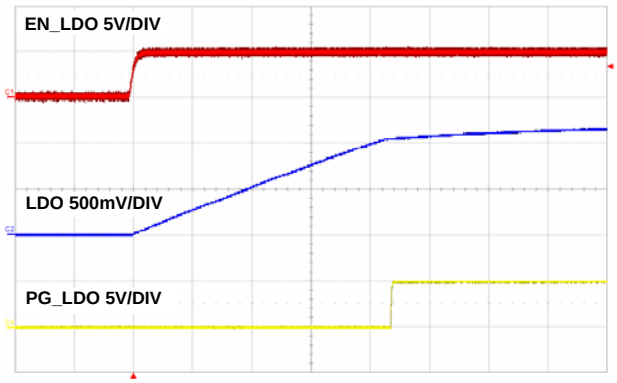


FIGURE 23. SOFT-START AT FULL LOAD, 100µs/DIV

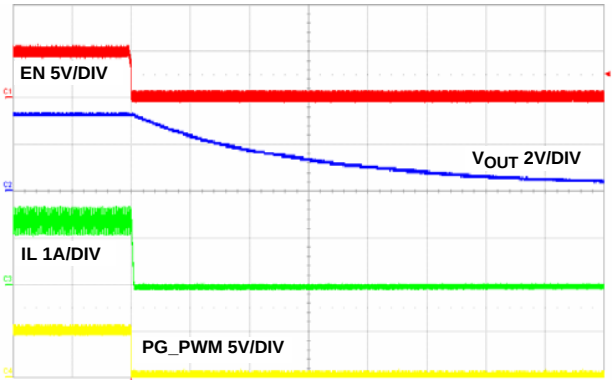


FIGURE 24. SHUT DOWN CIRCUIT, 100µs/DIV

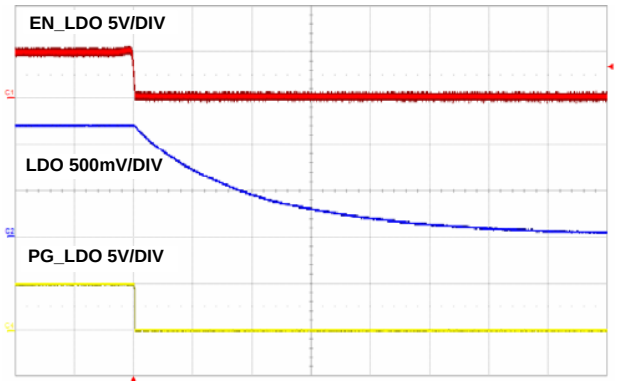


FIGURE 25. SHUT DOWN CIRCUIT, 20µs/DIV

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, VIN_LDO = V_{OUT} = 3.3V, I_{OUT} = 1A, VLDO = 1.2V, I_{LDO} = 450mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

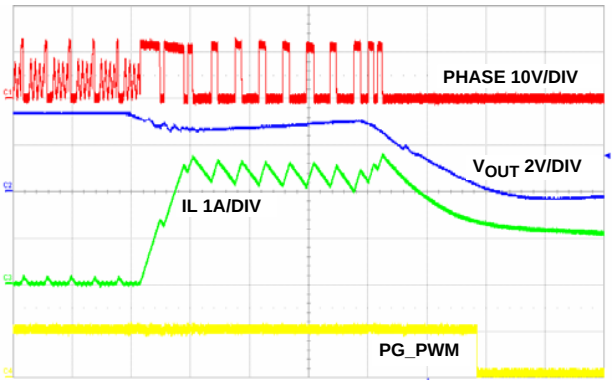


FIGURE 26. OUTPUT SHORT CIRCUIT, 5µs/DIV

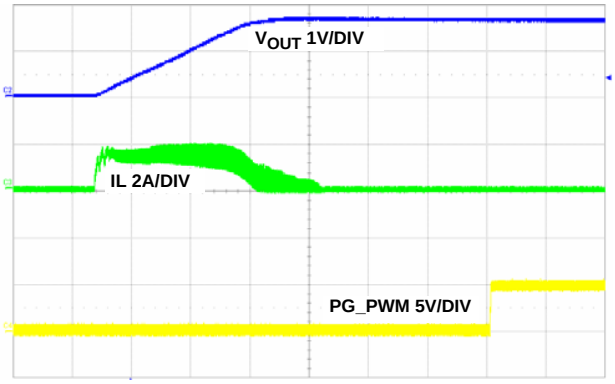


FIGURE 27. OUTPUT SHORT CIRCUIT RECOVERY, 200µs/DIV

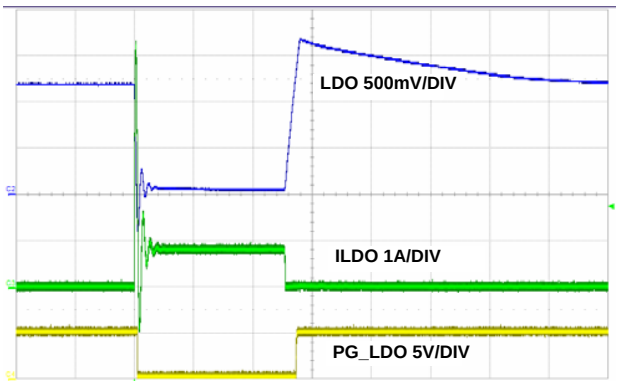


FIGURE 28. LDO SHORT CIRCUIT AND RECOVERY, 200µs/DIV

Detailed Description

The ISL8510 combines a standard buck PWM controller with an integrated switching MOSFET and one low dropout (LDO) linear regulators with internal pass devices. The buck controller drives an internal N-Channel MOSFET and requires an external diode to deliver load current up to 1A. A Schottky diode is recommended for improved efficiency and performance over a standard diode. The standard buck regulator can operate from either an unregulated DC source, such as a battery, with a voltage ranging from +5.5V to +25V, or from a regulated system rail of +5V. When operating from +5.5V or greater, the controller is biased from an internal +5V LDO voltage regulator. The converter output is regulated down to 0.6V from either input source. The LDO linear regulator can source up to 500mA continuous output current with +2V or greater input supply and +1.0V or higher output voltage. These features make the ISL8510 ideally suited for FPGA and wireless chipset power applications.

The PWM control loop uses a single output voltage loop with input voltage feed forward, which simplifies feedback loop compensation and rejects input voltage variation. External feedback loop compensation allows flexibility in output filter component selection. The regulator switches at a fixed 500kHz.

The buck regulator and LDO are provided with independent current limits. The current limit in the buck regulator is achieved by monitoring the drain-to-source voltage drop of the internal switching power MOSFET. The current limit threshold is internally set at 2A. The part also features undervoltage protection by latching the switching MOSFET driver to the OFF state during an overcurrent, when the output voltage is lower than 70% of the regulated output. This helps minimize power dissipation during a short-circuit condition. Due to only the switching power MOSFET integration, there is no overvoltage protection feature for this part.

The ISL8510 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO is 800mA typical. Neither LDO has over-voltage or undervoltage protection. When the current limit in output is reached, the output no longer regulates the voltage, but regulates the current to the value of the current limit.

+5V Internal Bias Supply (VCC)

Voltage applied to the VIN pin with respect to GND is regulated to +5V DC by an internal LDO regulator. The output of the LDO, VCC, is the bias voltage used by all the internal control and protection circuitry. The VCC pin requires a ceramic capacitor connected to GND. The capacitor serves to stabilize the LDO and to decouple load transients.

The input voltage range for the ISL8510 is specified as +5.5V to +25V or +5V ±10%. In the case of an unregulated supply case, the power supply is connected to VIN only. Once enabled, the linear regulator will turn-on and rise to +5V on VCC. In the +5V supply case, the VCC and VIN pins must be tied together to bypass the LDO. The external decoupling capacitor is still required in this mode. Do not short VCC to GND.

Operation Initialization

The power-on reset circuitry and enable inputs prevent false startup of the PWM regulator and LDO outputs. Once all the input criteria are met, the controller soft-starts the output voltage to the programmed level.

Power-On Reset and Undervoltage Lockout

The PWM portion of the ISL8510 automatically initializes upon receipt of input power. The power-on reset (POR) function continually monitors the VCC and PVCC voltages. While both are below their POR thresholds, the controller inhibits switching of the internal power MOSFET. Once exceeded, the controller initializes the internal soft-start circuitry. If either input supply drops below their falling POR threshold during soft-start or operation, the buck regulator latches off.

LDO supply inputs, VIN_LDO allows flexibility in partitioning linear regulator power. Power supplies connected to the LDO supply input must exceed the undervoltage lockout (UVLO) threshold before that LDO is initialized. If the input supply drops below the falling UVLO threshold during operation, the low dropout voltage regulator latches off.

Enable and Disable

All internal power devices are held in a high-impedance state, which ensures they remain off while in shutdown mode. Typically the enable input for a specific output is toggled high after the input supply to that regulator is active and the internal LDO has exceeded its POR threshold.

The EN_PWM pin enables the buck controller portion of the ISL8510. When the voltage on the EN_PWM pin exceeds the POR rising threshold, the controller initiates the soft-start function for the PWM regulator. If the voltage on the EN_PWM pin drops below the POR falling threshold, the buck regulator shuts down.

ILDO enable input, EN_LDO allows independent control of ISL8510 regulator. Make sure EN is on. When the voltage on either pin exceeds the POR rising threshold, the linear regulator operation is initiated for that controller. If the voltage then drops below the hysteresis level for the enable pin, the LDO shuts down.

Pulling the EN_PWM and EN_LDO pins low simultaneously puts all outputs into shutdown mode, and the supply current drops to 10µA typical.

Soft-Start

Once the input supply latch and enable threshold are met, the soft-start function is initialized. The soft-start circuitry begins sourcing 30µA, from an internal current source, which charges the external soft-start capacitor. The voltage on SS

begins ramping linearly from ground until the voltage across the soft-start capacitor reaches 3.0V. This linear ramp is applied to the non-inverting input of the internal error amplifier and overrides the nominal 0.6V reference. The output voltage reaches its regulation value when the soft-start capacitor voltage reaches 1.6V. Connect a capacitor from SS pin to ground. This capacitor, along with an internal 30µA current source sets the soft-start interval of the converter, t_{SS}.

$$C_{SS}[\mu F] = 50 \cdot t_{SS}[S] \quad \text{(EQ. 1)}$$

Upon disabling, the SS pin voltage will discharge to zero voltage.

Power-Good

PG_PWM is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG_PWM is actively held low when EN_PWM is low and during the buck regulator soft-start period. After the soft-start period terminates, PG_PWM becomes high impedance as long as the output voltage is within ±10% of the nominal regulation voltage set by FB_PWM. When V_{OUT} drops 10% below or rises 10% above the nominal regulation voltage, the ISL8510 pulls PG_PWM low. Any fault condition forces PG_PWM low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor between PG_PWM and VCC. A 100k resistor works well in most applications. Note that the PG_PWM window detector is completely independent of the undervoltage protection fault detectors and the state of LDO output.

PG_LDO is an open drain pull-down NMOS output that will sink 1mA at 0.3V max. It goes to the active low state if the LDO output is out of regulation by a value greater than 15%. When the LDO is disabled, the output is active low.

Output Voltage Selection

All three regulator output voltages can be programmed using external resistor dividers that scale the voltage feedback relative to the internal reference voltage. The scaled voltage is fed back to the inverting input of the error amplifier (refer to Figure 29).

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor, R_1, and the desired output voltage, V_{OUT}, of the regulator (see Equation 2). The value for the feedback resistor is typically between 1kΩ and 10kΩ.

$$R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated.

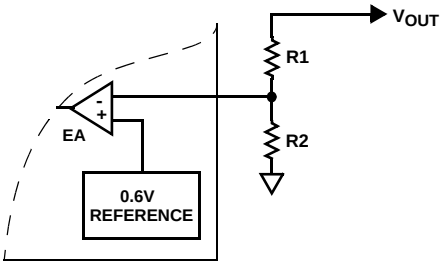


FIGURE 29. EXTERNAL RESISTOR DIVIDER

The buck output can be programmed as high as 20V. Proper heatsinking must be provided to insure that the junction temperature does not exceed +125°C.

When the output is set greater than 3.6V, it is recommended to pre-load at least 1mA and make sure that the input rise time is much faster than the V_{OUT1} rise time. This allows the BOOT capacitor adequate time to charge for proper operation.

Protection Features

The ISL8510 limits current in all on-chip power devices to limit on-chip power dissipation. Overcurrent limits on all three regulators protect internal power devices from excessive thermal damage. Undervoltage protection circuitry on the buck regulator provides a second layer of protection for the internal power device under high current conditions.

Buck Regulator Overcurrent Protection

During the PWM on-time, the current through the internal switching MOSFET is sampled and scaled through an internal pilot device. The sampled current is compared to a nominal 2A overcurrent limit. If the sampled current exceeds the overcurrent limit reference level, an internal overcurrent fault counter is set to 1 and an internal flag is set. The internal power MOSFET is immediately turned off and will not be turned on again until the next switching cycle.

The protection circuitry continues to monitor the current and turns off the internal MOSFET as described. If the overcurrent condition persists for four sequential clock cycles, the overcurrent fault counter overflows indicating an overcurrent fault condition exists. The regulator is shut down and power-good goes low. If the overcurrent condition clears prior to the counter reaching four consecutive cycles, the internal flag and counter are reset.

The protection circuitry attempts to recover from the overcurrent condition after waiting 4 soft-start cycles. The internal overcurrent flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the overcurrent fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

LDO Current Limit

The ISL8510 monitors and controls the pass transistor's gate voltage to limit output current. The current limit for LDO is 700mA typical. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Undervoltage Protection

If the voltage detected on the buck regulator FB pin falls 15% below the internal reference voltage, the undervoltage fault condition flag is set. The fault protection circuitry checks the overcurrent flag. If the overcurrent flag is set, the fault monitor latches off the internal power MOSFET. The regulator will not restart until either a POR restart or the EN_PWM pin is cycled.

If the overcurrent flag is not set, an internal undervoltage counter is set to 1. The fault controller continues to monitor the FB pin for 4 clock cycles. If the fault condition persists, the regulator is shutdown. The controller enters a recovery mode similar to the overcurrent hiccup mode. No action is taken for 4 soft-start cycles and the internal undervoltage counter and fault condition flag are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the undervoltage counter overflows during soft-start, the converter is shut down and this hiccup mode operation repeats.

Undervoltage protection only applies to the buck regulator output; the LDO output does not have undervoltage protection.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL8510. There are three sensors on the chip to monitor the junction temperature of the internal LDO, PWM switching power N-Channel MOSFET, and LDO pass transistors. When the junction temperature (T_J) of any of the three sensors exceeds +150°C, the thermal sensor sends a signal to the fault monitor.

The fault monitor commands the buck regulator to shut down and the LDO to turn off the pass transistor. The buck regulator soft-starts and the LDO pass transistor turn on again after the IC's junction temperature cools by +20°C. The buck regulator experiences hiccup mode operation and the LDO a pulsed output during continuous thermal overload conditions. For continuous operation, do not exceed the +125°C junction temperature rating.

Low Dropout Regulator

The regulator consists of a 0.6V reference, error amplifier, MOSFET driver, P-Channel pass transistor, and dual-mode comparator. The voltage is set by means of an external resistor divider on the FB_LDO pin. The 0.6V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower than the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output.

Internal P-Channel Pass Transistor

The LDO regulator in the ISL8510 feature a typical 0.33Ω $r_{DS(ON)}$ P-Channel MOSFET pass transistor. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL8510 does not have these drawbacks.

Integrator Circuitry

The ISL8510 uses external compensation capacitors for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown. Place a 33nF capacitor to GND from CC1 and CC2.

Application Guidelines

Operating Frequency

The ISL8510 operates at a fixed switching frequency of 500kHz.

LDO Regulator Capacitor Selection

Capacitors are required at the ISL8510 LDO Regulators' input and output for stable operation over the entire load range and the full temperature range. Use a >1µF capacitor at the input of LDO Regulator, VIN_LDO pin. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provide better PSRR and line transient response. The input capacitor must be located at a distance of not more then 0.5 inches from the VIN_LDO pin of the IC and returned to a clean analog ground. Any good quality ceramic capacitor can be used as an input capacitor.

The output capacitors used in LDO regulator are used to provide dynamic load current. The amount of capacitance and type of capacitor should be chosen with this criteria in mind. The output capacitor selected must meet the requirements of minimum amount of capacitance and ESR for LDO. The ISL8510 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor

with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 10µF, is recommended for LDO output. There is no upper limit to the output capacitor value. Larger capacitor values can reduce noise and improve load transient response, stability and PSRR. The output capacitor should be located very close to the VOUT pins to minimize impact of PC board inductances. The other end of the capacitor should be returned to a clean analog ground.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Embedded processor systems are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated using Equation 3:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 3)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient. The recommended ΔI is 30% of the maximum output current.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL8510 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equations 4 and 5 give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad \text{(EQ. 4)}$$

$$t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 5)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Rectifier Selection

Current circulates from ground to the junction of the MOSFET and the inductor when the high-side switch is off. As a consequence, the polarity of the switching node is negative with respect to ground. This voltage is approximately -0.5V (a Schottky diode drop) during the off-time. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor. The power dissipation is as shown in Equation 6:

$$P_D[W] = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{(EQ. 6)}$$

where V_D is the voltage of the Schottky diode = 0.5V to 0.7V

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors

to supply the current needed each time the switching MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFET VIN pins (switching MOSFET drain) and the Schottky diode anode.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through Equation 7:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT_{MAX}}{}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}}\right)^2\right)} \quad \text{(EQ. 7)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Feedback Compensation

Figure 30 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at f_{LC} and a zero at f_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

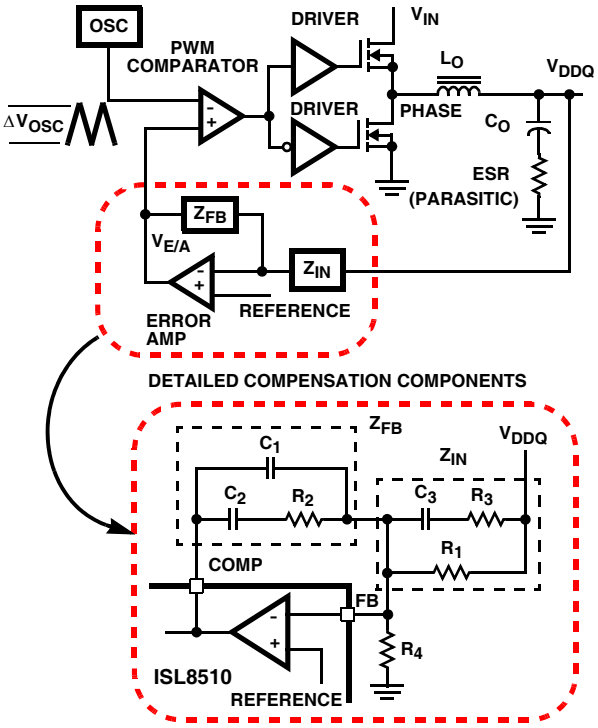
Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad \text{(EQ. 8)}$$

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(EQ. 9)}$$

The compensation network consists of the error amplifier (internal to the ISL6537) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. Equations 10 through 13 relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 31. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1st Zero Below Filter's Double Pole (~75% f_{LC}).
3. Place 2nd Zero at Filter's Double Pole.
4. Place 1st Pole at the ESR Zero.
5. Place 2nd Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.



$$V_{DDQ} = 0.8 \times \left(1 + \frac{R_1}{R_4}\right)$$

FIGURE 30. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

Compensation Break Frequency Equations

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \quad \text{(EQ. 10)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \quad \text{(EQ. 11)}$$

$$f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)} \quad \text{(EQ. 12)}$$

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \quad \text{(EQ. 13)}$$

Figure 31 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 31. Using the guidelines from "Modulator Break Frequency Equations" on page 18 should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 31 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

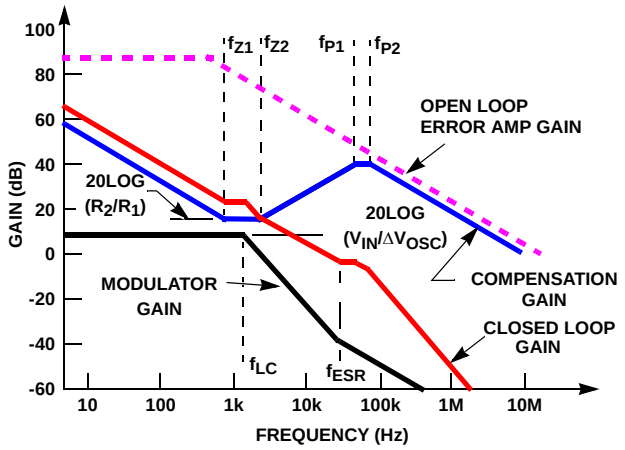


FIGURE 31. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A more detailed explanation of voltage mode control of a buck regulator can be found in Tech Brief TB417, entitled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators."
http://www.intersil.com/data/tb/tb417.pdf

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 500kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the control MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL8510 switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 32 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer (usually a middle layer of the PC board) for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

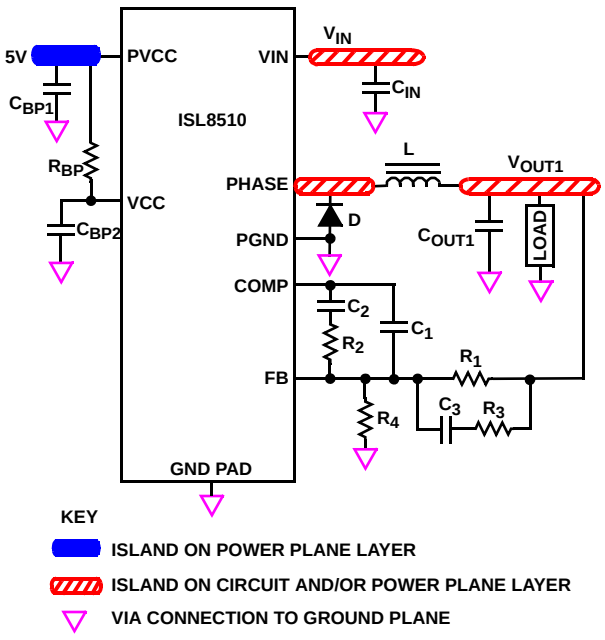


FIGURE 32. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

In order to dissipate heat generated by the internal V_{TT} LDO, the ground pad, pin 29, should be connected to the internal ground plane through at least four vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the ISL6537 first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and lower MOSFETs and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

Package Outline Drawing

L24.4x4D

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
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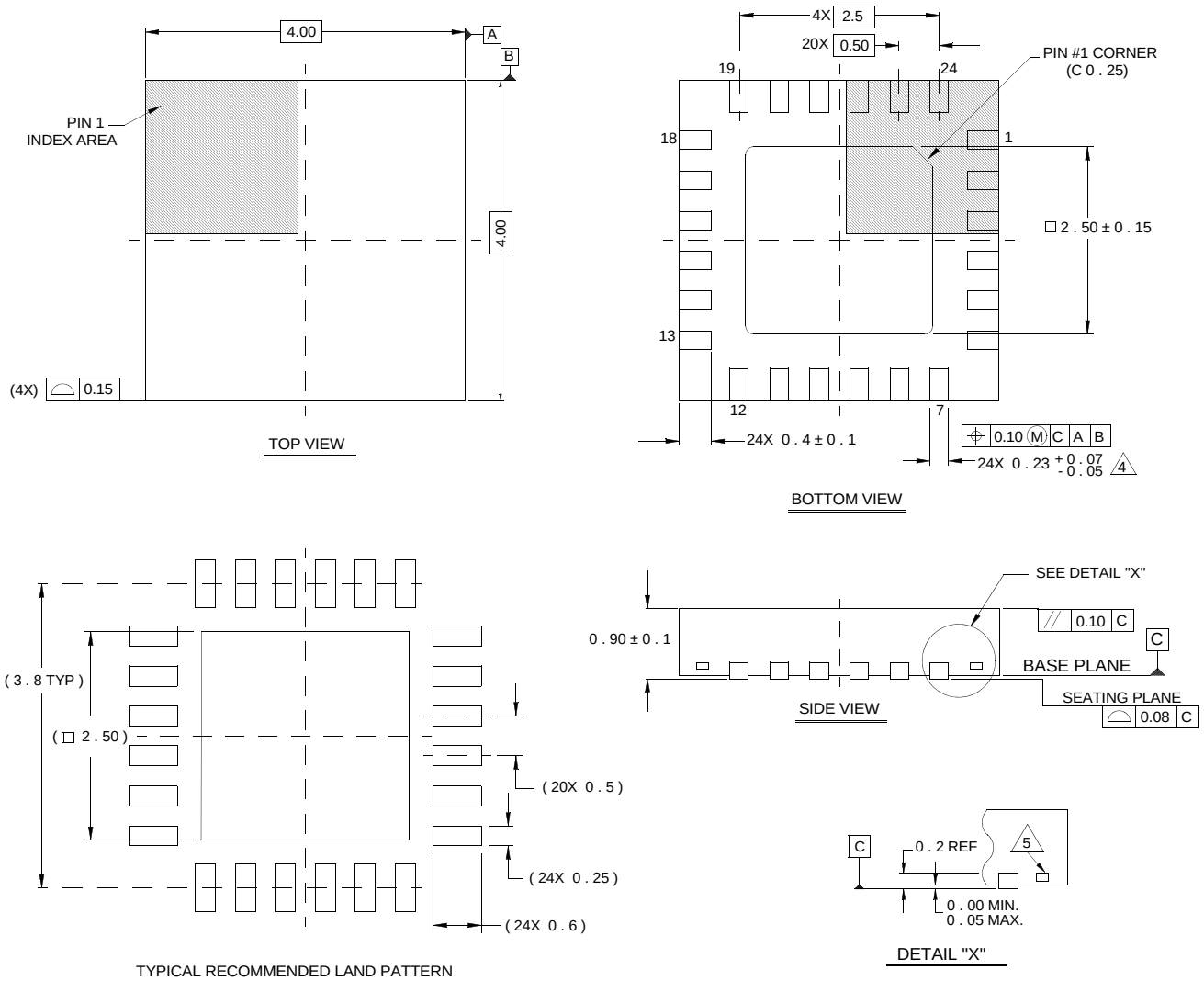

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.