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[Texas Instruments](#)  
[SN74AS253ADRG4](#)

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**SN54ALS253, SN74ALS253, SN74AS253A  
DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS  
WITH 3-STATE OUTPUTS**

SDAS216A – APRIL 1982 – REVISED DECEMBER 1994

- 3-State Versions of the 'ALS153 and SN74AS153
- Permits Multiplexing From n Lines to One Line
- Performs Parallel-to-Serial Conversion
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

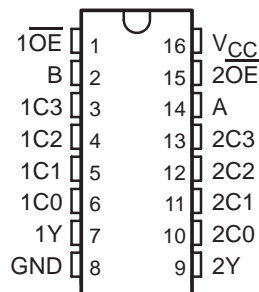
**description**

These data selectors/multiplexers contain inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two 4-line sections.

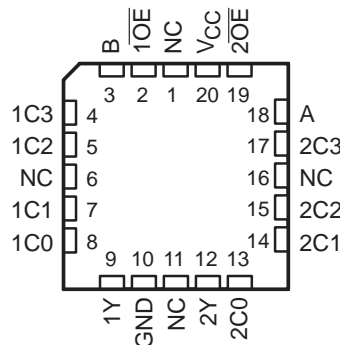
The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable ( $\overline{OE}$ ) input. The output is disabled when  $\overline{OE}$  is high.

The SN54ALS253 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS253 and SN74AS253A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN54ALS253 . . . J PACKAGE  
SN74ALS253, SN74AS253A . . . D OR N PACKAGE  
(TOP VIEW)**



**SN54ALS253 . . . FK PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE**

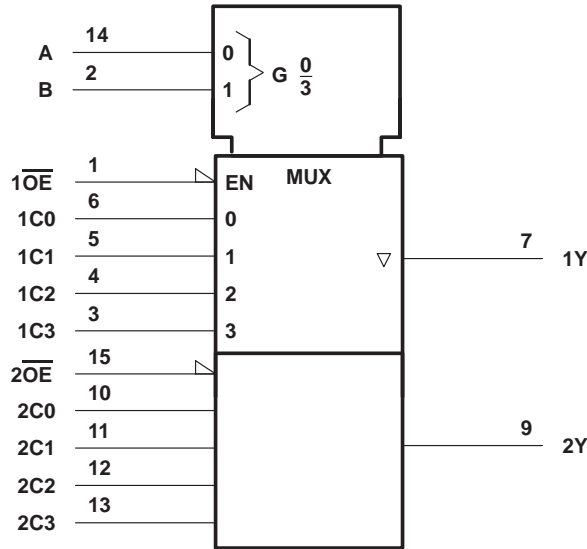
SELECT†		DATA				$\overline{OE}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

† Select inputs A and B are common to both sections.

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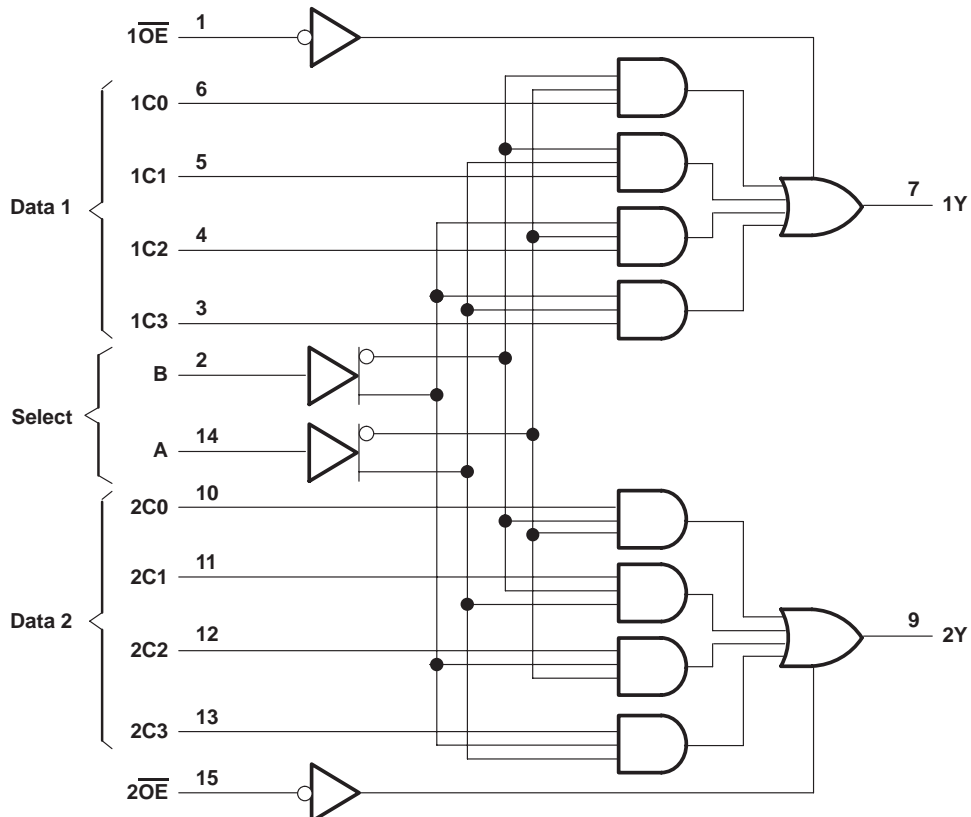
SDAS216A - APRIL 1982 - REVISED DECEMBER 1994

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the D, J, and N packages.

**logic diagram (positive logic)**



Pin numbers shown are for the D, J, and N packages.

**SN54ALS253, SN74ALS253, SN74AS253A**  
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**WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS253 .....	-55°C to 125°C
SN74ALS253 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54ALS253			SN74ALS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-1			-2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS253			SN74ALS253			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -0.4 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V$	$I_{OH} = -1 mA$	2.4	3.3				
		$I_{OH} = -2.6 mA$			2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 12 mA$	0.25	0.4	0.25	0.4	V	
		$I_{OL} = 24 mA$			0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5 V$ , $V_O = 2.7 V$			20			20	μA
$I_{OZL}$	$V_{CC} = 5.5 V$ , $V_O = 0.4 V$			-20			-20	μA
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$			-0.1			-0.1	mA
$I_{O§}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-20		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$	Outputs high	6.5	12	6.5	12	mA	
		Outputs disabled	7.5	14	7.5	14		

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25°C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



**SN54ALS253, SN74ALS253, SN74AS253A**  
**DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS253		SN74ALS253		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Any Y	5	30	5	21	ns
t <sub>PHL</sub>			5	27	5	21	
t <sub>PLH</sub>	Data (any C)	Any Y	2	15	2	10	ns
t <sub>PHL</sub>			3	18	3	14	
t <sub>PZH</sub>	$\overline{OE}$	Any Y	3	20	3	14	ns
t <sub>PZL</sub>			2	19	4	16	
t <sub>PHZ</sub>	$\overline{OE}$	Any Y	2	12	2	10	ns
t <sub>PLZ</sub>			2	18	2	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage, V<sub>CC</sub> ..... 7 V  
 Input voltage, V<sub>I</sub> ..... 7 V  
 Operating free-air temperature range, T<sub>A</sub>: SN74AS253A ..... 0°C to 70°C  
 Storage temperature range ..... -65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN74AS253A			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			48	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

**SN54ALS253, SN74ALS253, SN74AS253A**  
**DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS**  
**WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS253A			UNIT	
		MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V	
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$	2.4	3.2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$		0.35	0.5	V	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			50	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$			-50	$\mu\text{A}$	
$I_I$	A, B	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$	0.2	mA	
	All others			0.1		
$I_{IH}$	A, B	$V_{CC} = 5.5\text{ V}$	$V_I = 2.7\text{ V}$	40	$\mu\text{A}$	
	All others			20		
$I_{IL}$	A, B	$V_{CC} = 5.5\text{ V}$	$V_I = 0.4\text{ V}$	-1	mA	
	All others			-0.5		
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$			-30	-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high		18	29	mA
		Outputs low		20	32	
		Outputs disabled		21	33	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

switching characteristics (see Figure 1)

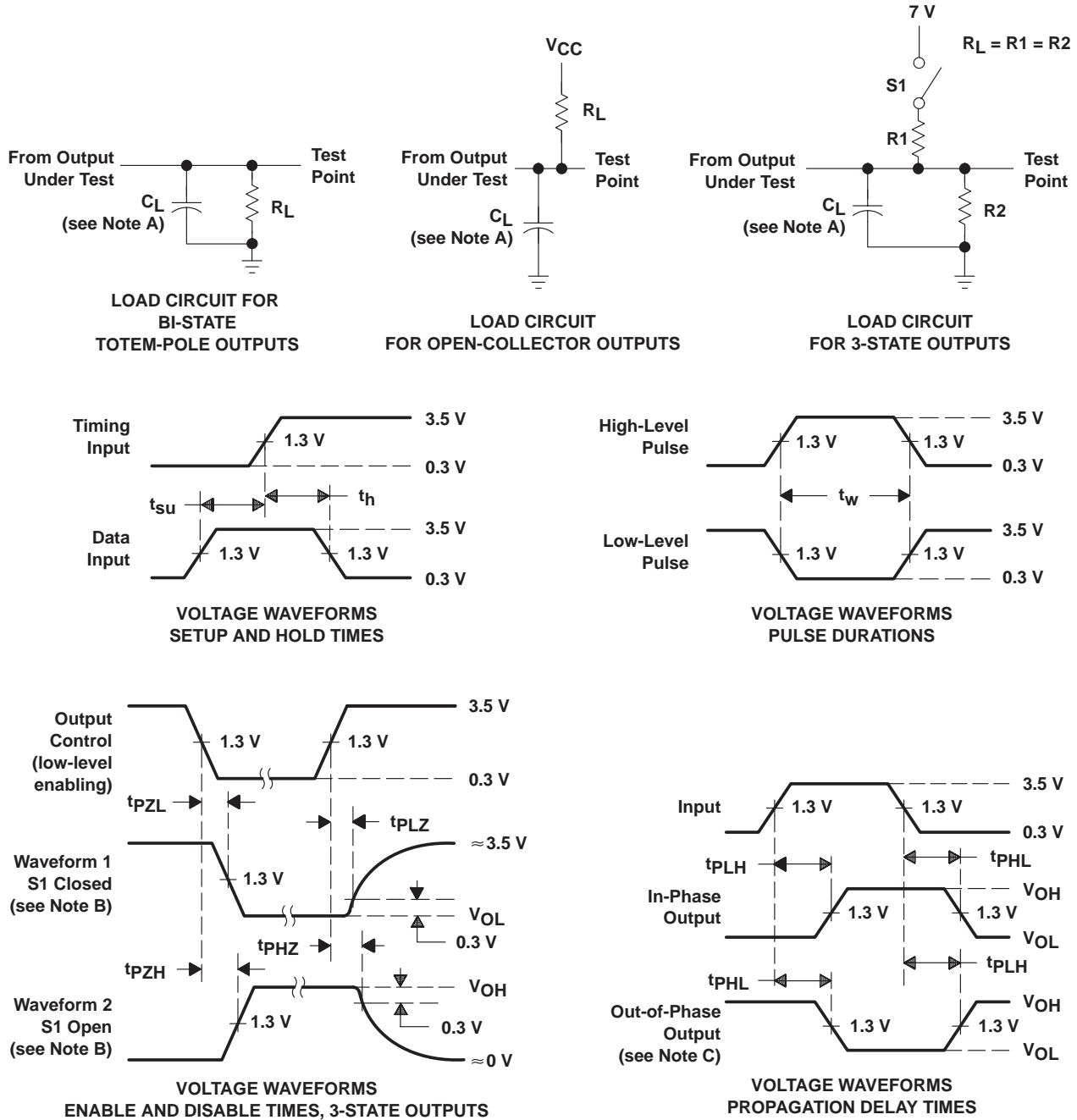
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$		UNIT
			SN74AS253A		
			MIN	MAX	
$t_{PLH}$	A or B	Y	3	13.5	ns
$t_{PHL}$			3	11.5	
$t_{PLH}$	Data (any C)	Y	2.5	7.5	ns
$t_{PHL}$			2.5	8	
$t_{PZH}$	$\overline{OE}$	Any Y	2	12.5	ns
$t_{PZL}$			2.5	11.5	
$t_{PHZ}$	$\overline{OE}$	Any Y	1	6	ns
$t_{PLZ}$			1	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85096012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85096012A SNJ54ALS 253FK	<a href="#">Samples</a>
8509601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8509601EA SNJ54ALS253J	<a href="#">Samples</a>
SN74ALS253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS253	<a href="#">Samples</a>
SN74ALS253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS253	<a href="#">Samples</a>
SN74ALS253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS253	<a href="#">Samples</a>
SN74ALS253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS253	<a href="#">Samples</a>
SN74ALS253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS253N	<a href="#">Samples</a>
SN74ALS253NSR	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN74ALS253NSRE4	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN74ALS253NSRG4	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN74AS253AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS253A	<a href="#">Samples</a>
SN74AS253ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS253A	<a href="#">Samples</a>
SN74AS253AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74AS253ANE4	ACTIVE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		<a href="#">Samples</a>
SNJ54ALS253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85096012A SNJ54ALS 253FK	<a href="#">Samples</a>
SNJ54ALS253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8509601EA SNJ54ALS253J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.





**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS253, SN74ALS253 :**

● Catalog: [SN74ALS253](#)

● Military: [SN54ALS253](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product



**Distributor of Texas Instruments: Excellent Integrated System Limited**

Datasheet of SN74AS253ADRG4 - IC DATA SELECTOR/MUX SGL 16SOIC

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**PACKAGE OPTION ADDENDUM**

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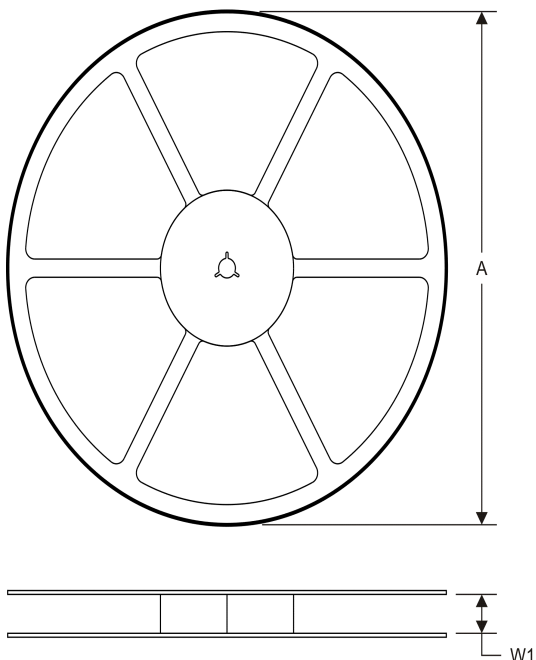
[www.ti.com](http://www.ti.com)

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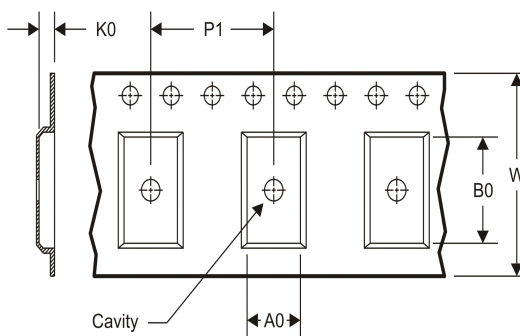
- 
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



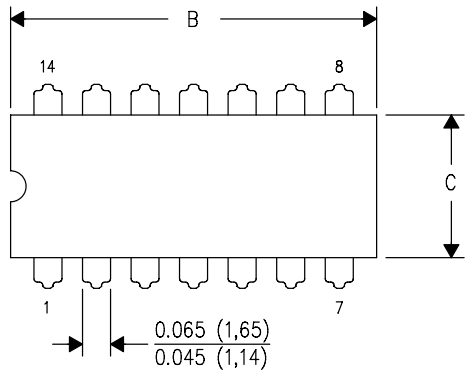
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS253DR	SOIC	D	16	2500	333.2	345.9	28.6

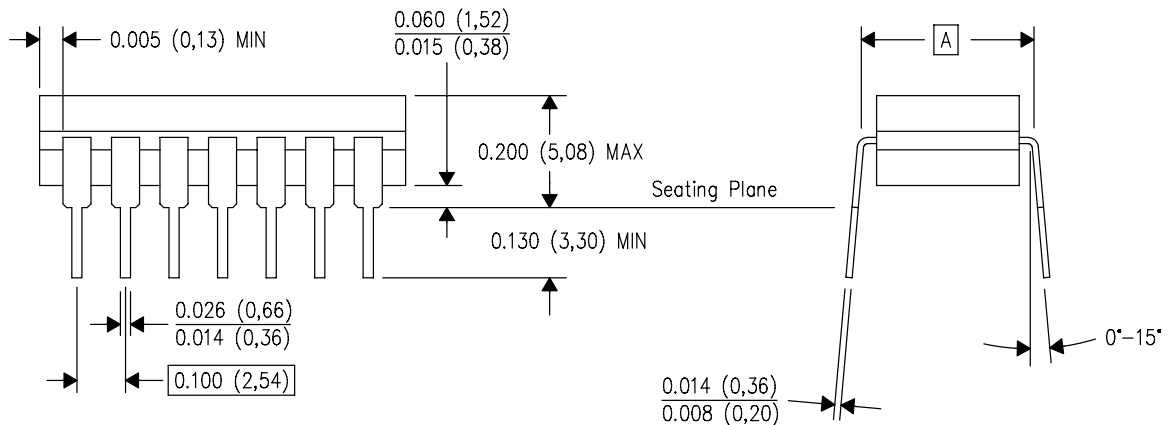
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



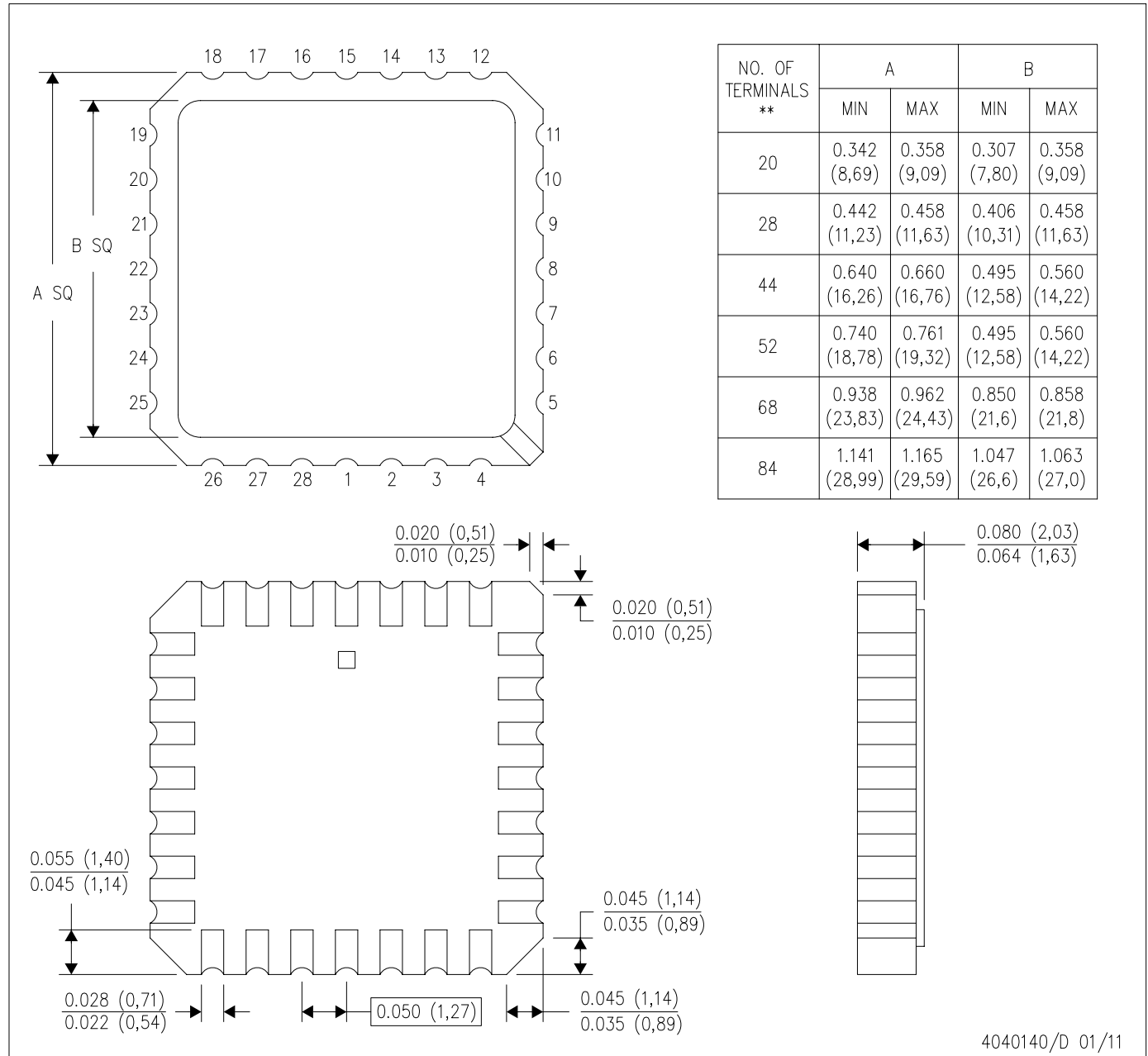
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 01/11

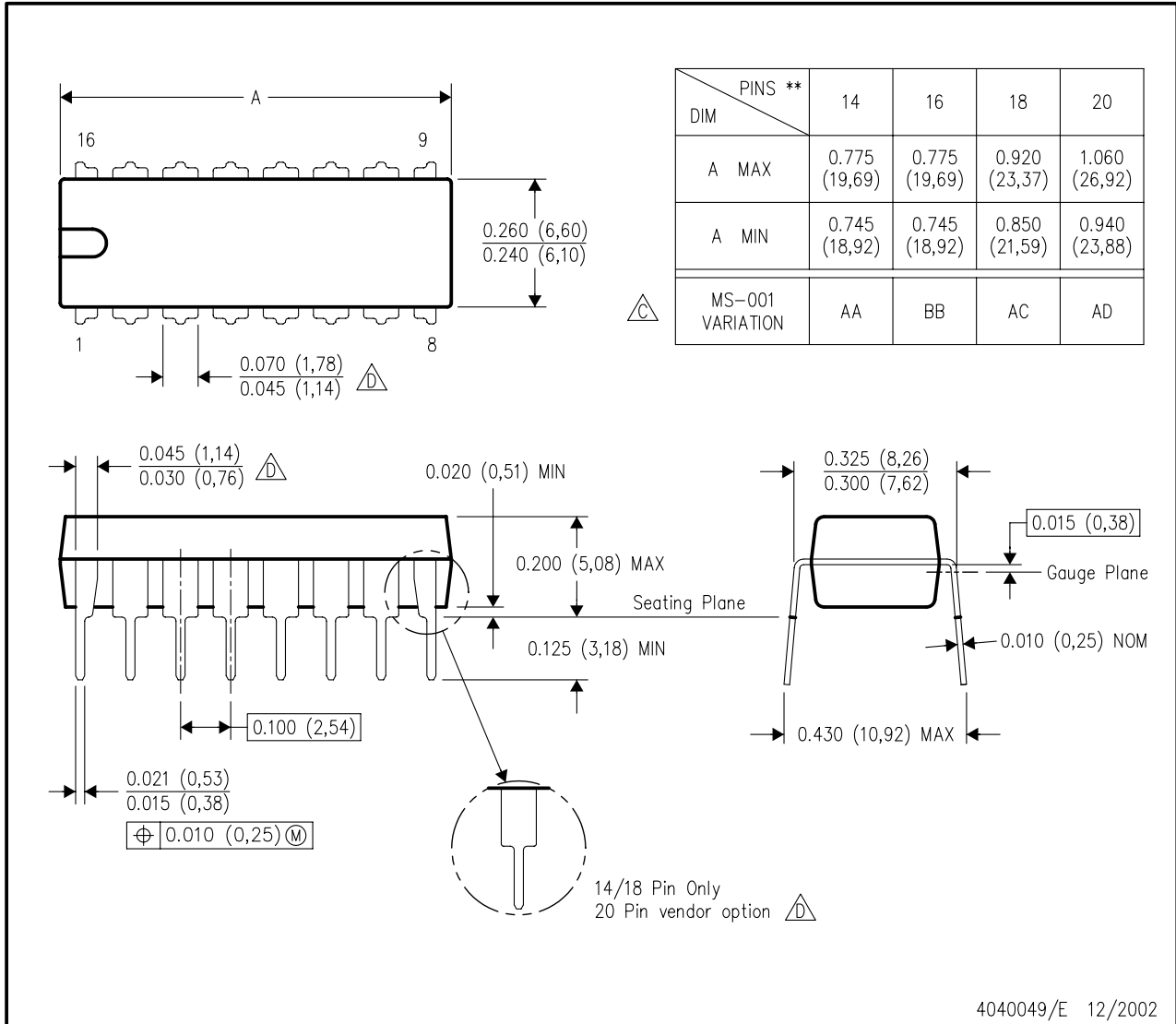
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

**MECHANICAL DATA**

**N (R-PDIP-T\*\*)**

16 PINS SHOWN

**PLASTIC DUAL-IN-LINE PACKAGE**

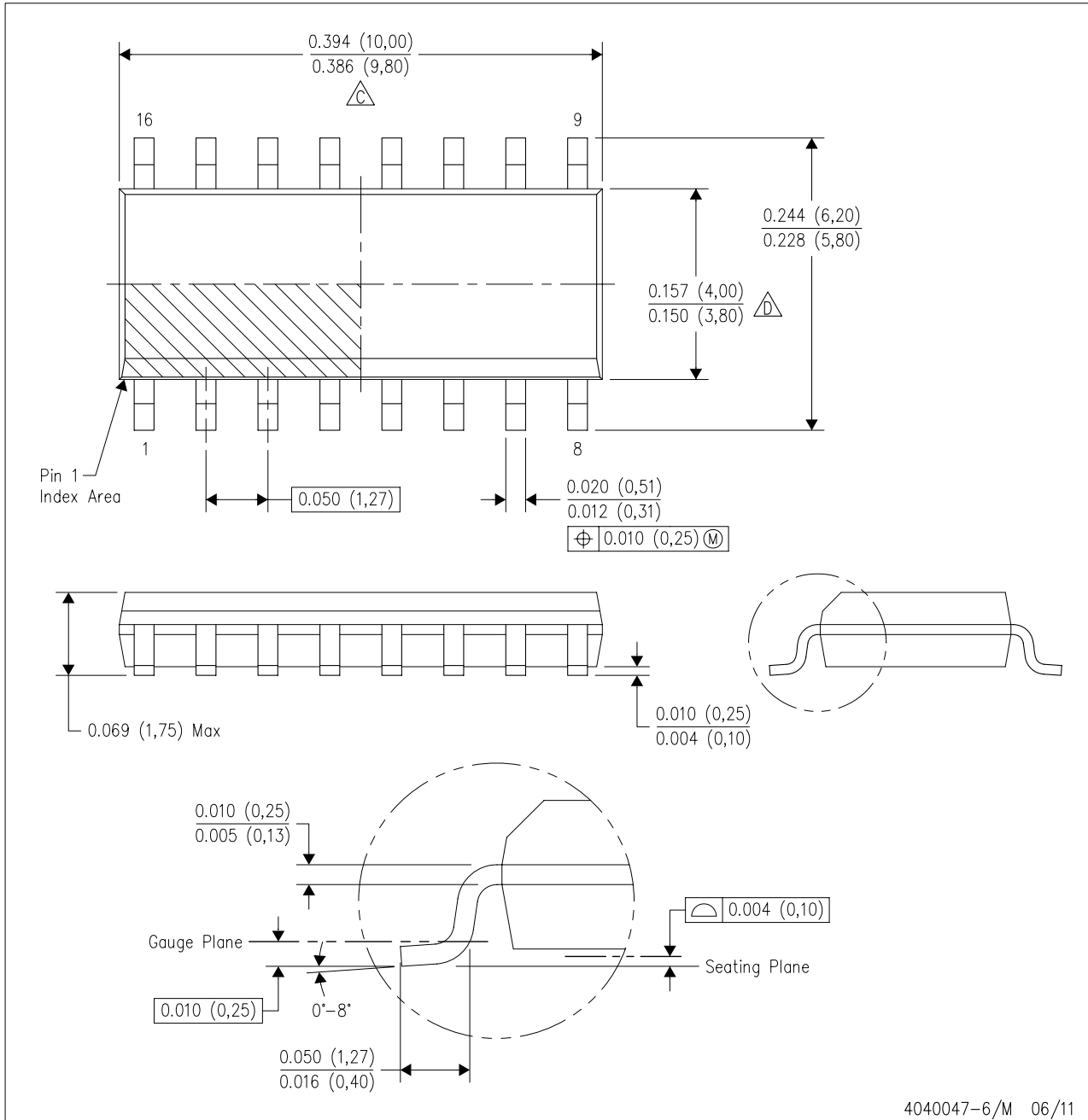


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**MECHANICAL DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



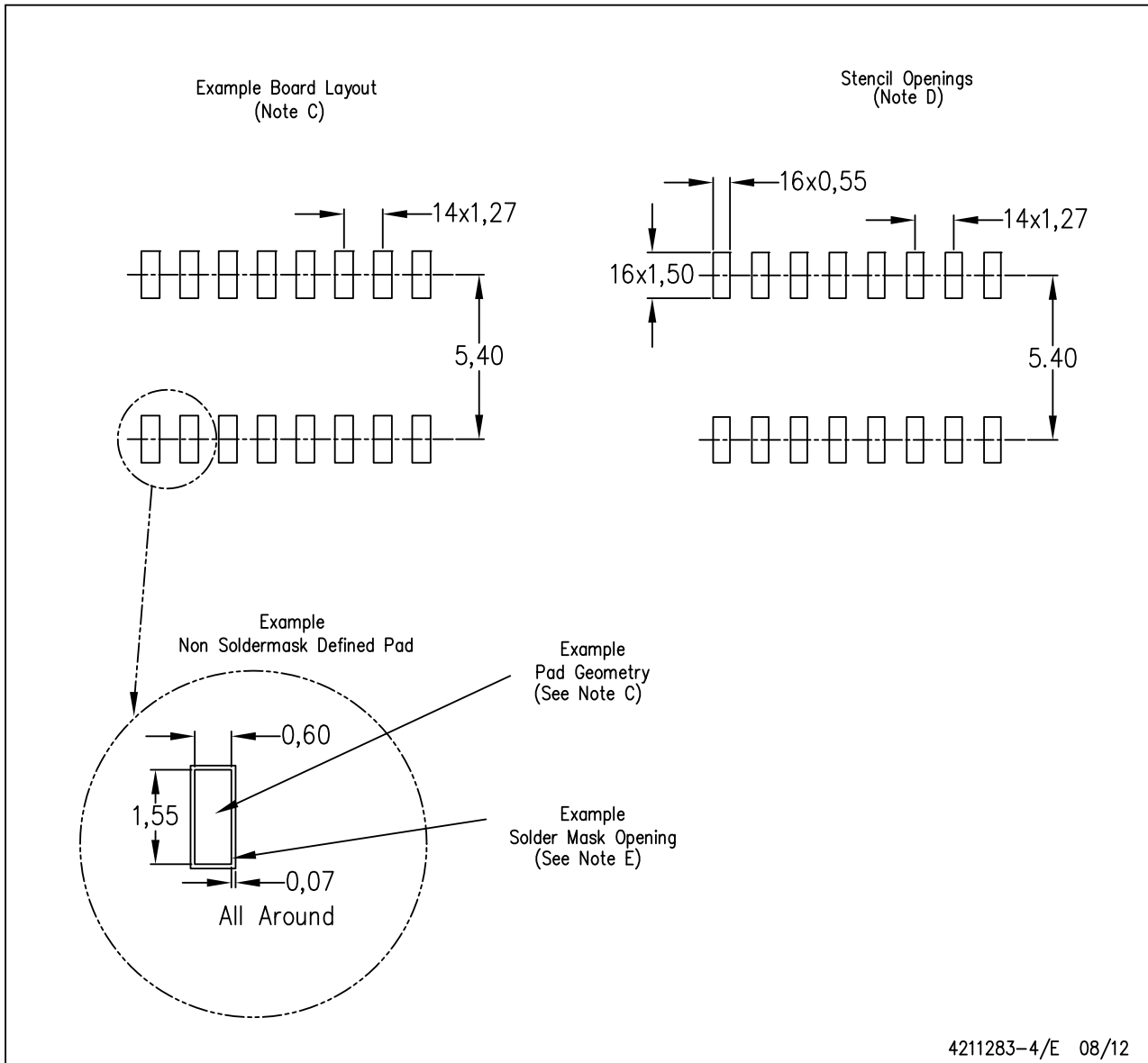
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



**LAND PATTERN DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



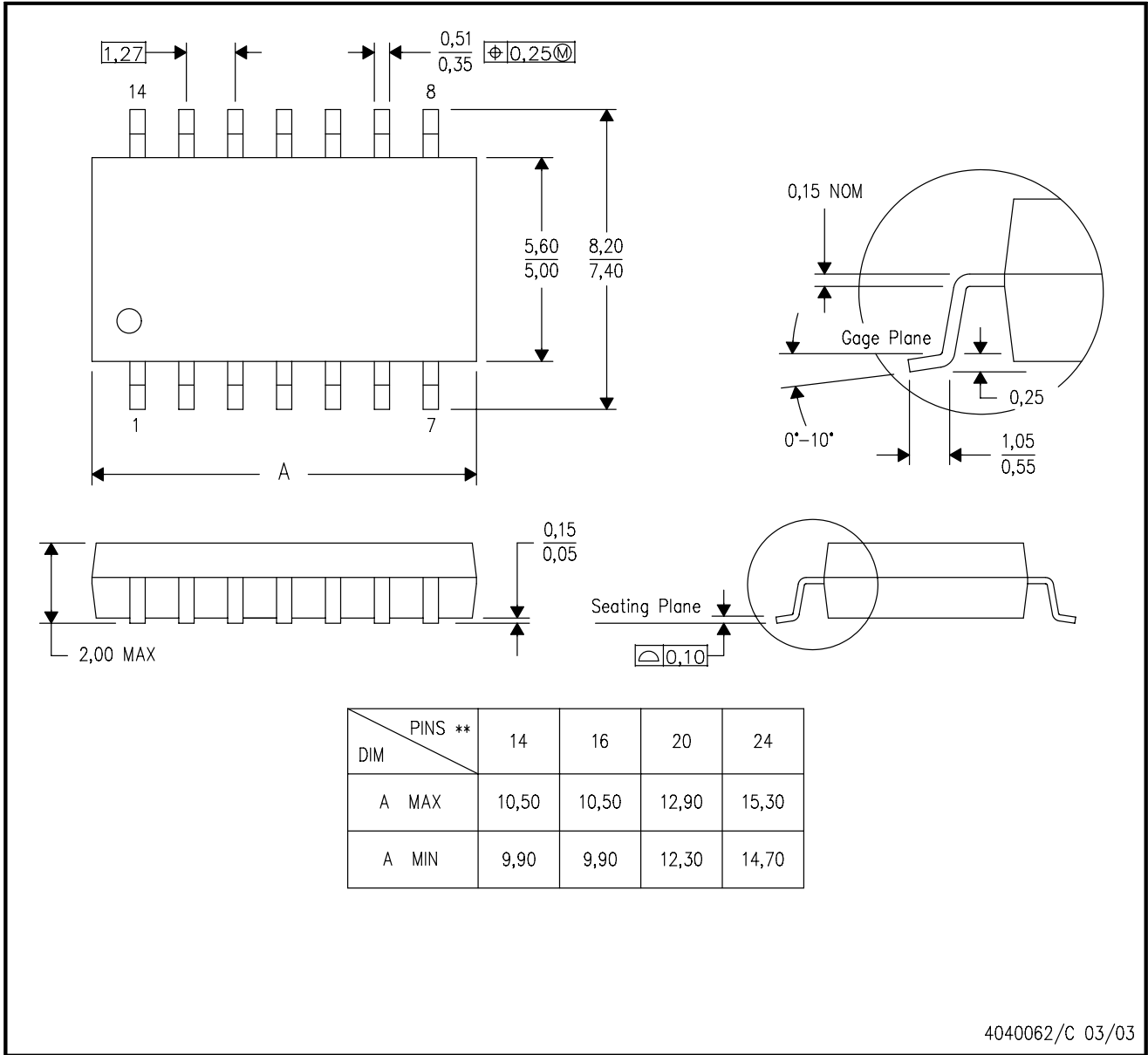
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**MECHANICAL DATA**

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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