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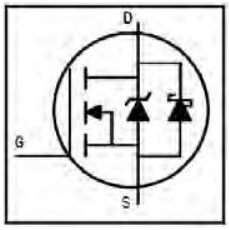
IRL3103D1SPbF

FETKY™ MOSFET & SCHOTTKY RECTIFIER

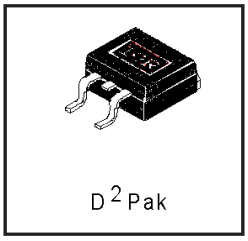
- Co-packaged HEXFET® Power MOSFET and Schottky Diode
- Generation 5 Technology
- Logic Level Gate Drive
- Minimize Circuit Inductance
- Ideal For Synchronous Regulator Application
- Lead-Free



V_{DSS} = 30V

$R_{DS(on)}$ = 0.014Ω

I_D = 64A



D 2 Pak

Description

The FETKY family of co-packaged HEXFET power MOSFETs and Schottky Diodes offer the designer an innovative board space saving solution for switching regulator applications. A low on resistance Gen 5 MOSFET with a low forward voltage drop Schottky diode and minimized component interconnect inductance and resistance result in maximized converter efficiencies.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V③	64	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V③	45	
I_{DM}	Pulsed Drain Current ①③	220	
P_D @T_A = 25°C	Power Dissipation	3.1	W
P_D @T_C = 25°C	Power Dissipation	89	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—–	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	—–	40	

MOSFET Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.037	—	V/°C	Reference to 25°C, I_D = 1mA③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.014	Ω	V_{GS} = 10V, I_D = 34A ②
		—	—	0.019		V_{GS} = 4.5V, I_D = 28A ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	23	—	—	S	V_{DS} = 25V, I_D = 34A③
I_{DSS}	Drain-to-Source Leakage Current	—	—	0.10	mA	V_{DS} = 30V, V_{GS} = 0V
		—	—	22		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	43	nC	I_D = 32A
Q_{gs}	Gate-to-Source Charge	—	—	14		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		V_{GS} = 4.5V, See Fig. 6 ②
$t_{d(on)}$	Turn-On Delay Time	—	9.0	—	ns	V_{DD} = 15V
t_r	Rise Time	—	210	—		I_D = 32A
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		R_G = 3.4Ω, V_{GS} =4.5V
t_f	Fall Time	—	54	—		R_D = 0.43 Ω, ②③
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1900	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	810	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5
C_{iss}	Input Capacitance	—	3500	—		V_{GS} = 0V, V_{DS} = 0V

Body Diode & Schottky Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_F (AV)	(Schottky)	—	—	2.0	A	MOSFET symbol showing the integral reverse p-n junction and Schottky diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD1}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 32A, V_{GS} = 0V ②
V_{SD2}	Diode Forward Voltage	—	—	0.50	V	T_J = 25°C, I_S = 1.0A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	51	77	ns	T_J = 25°C, I_F = 32A
Q_{rr}	Reverse Recovery Charge	—	49	73	nC	di/dt = 100A/µs ②
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 10)

② Pulse width ≤ 300µs; duty cycle ≤ 2%.

③Uses IRL3103D1 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

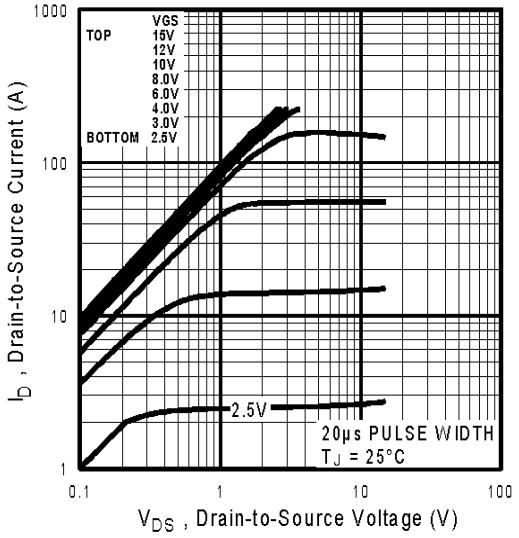


Fig 1. Typical Output Characteristics

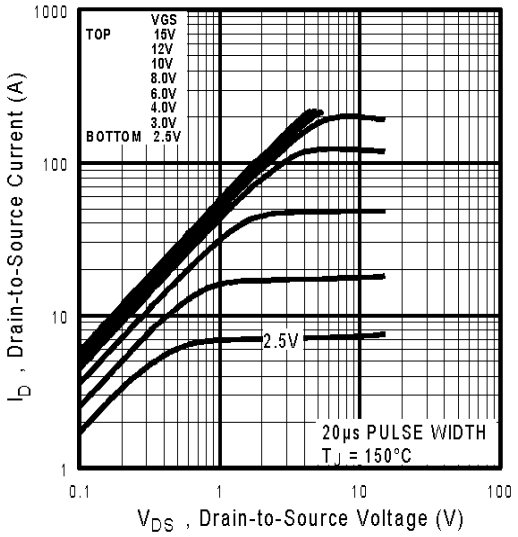


Fig 2. Typical Output Characteristics

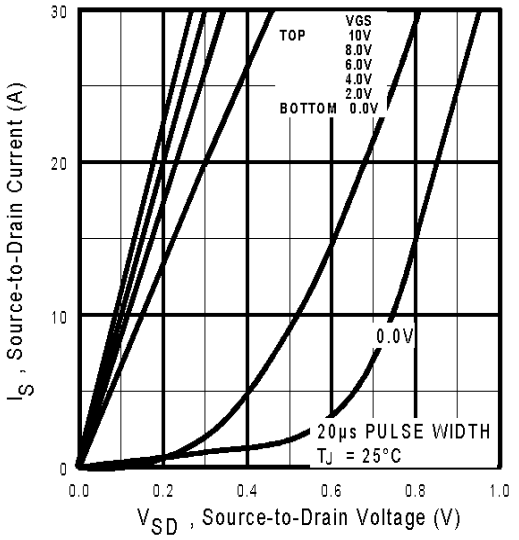


Fig 3. Typical Reverse Output Characteristics

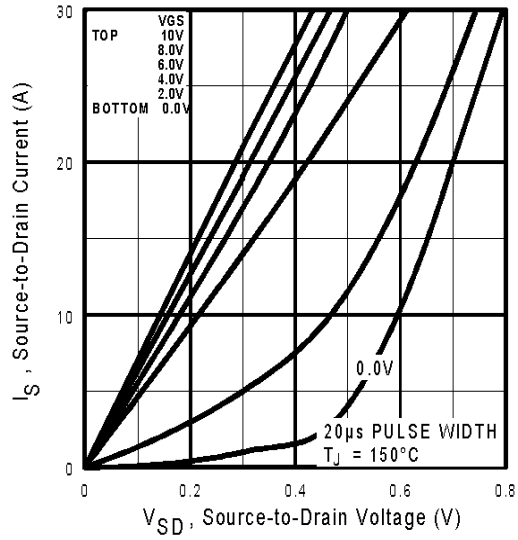


Fig 4. Typical Reverse Output Characteristics

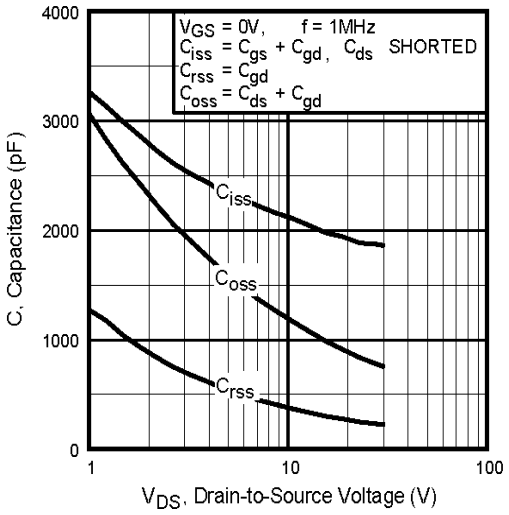


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

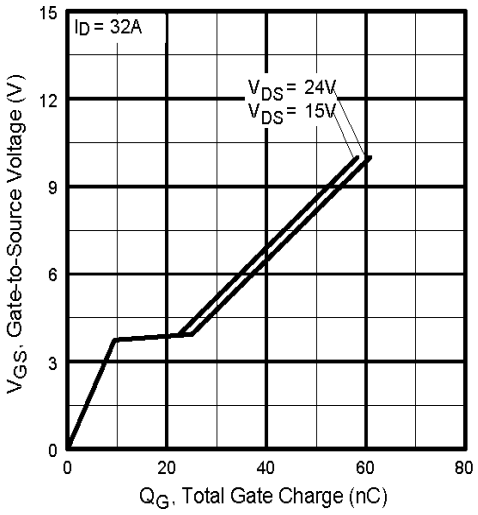


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

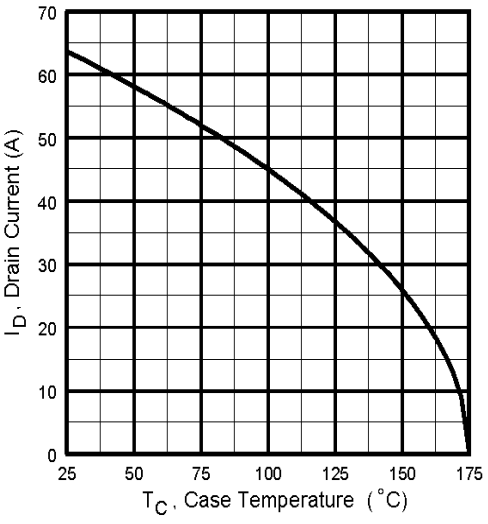


Fig 7. Maximum Drain Current Vs. Case Temperature

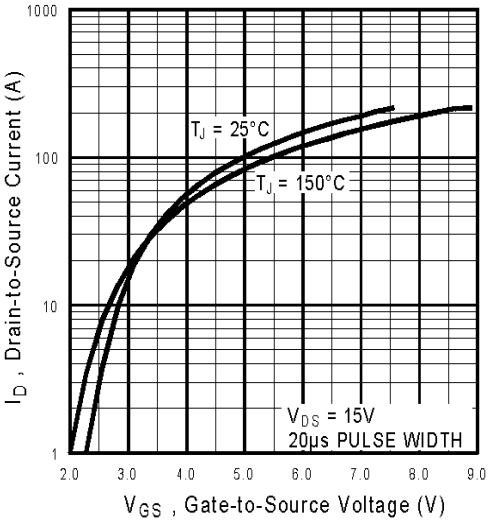


Fig 8. Typical Transfer Characteristics

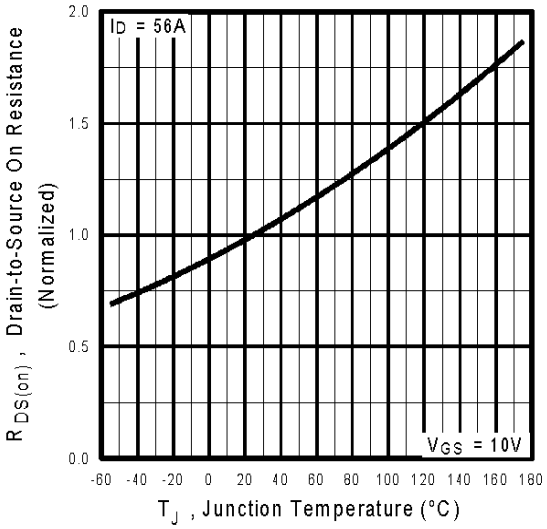


Fig 9. Normalized On-Resistance Vs. Temperature

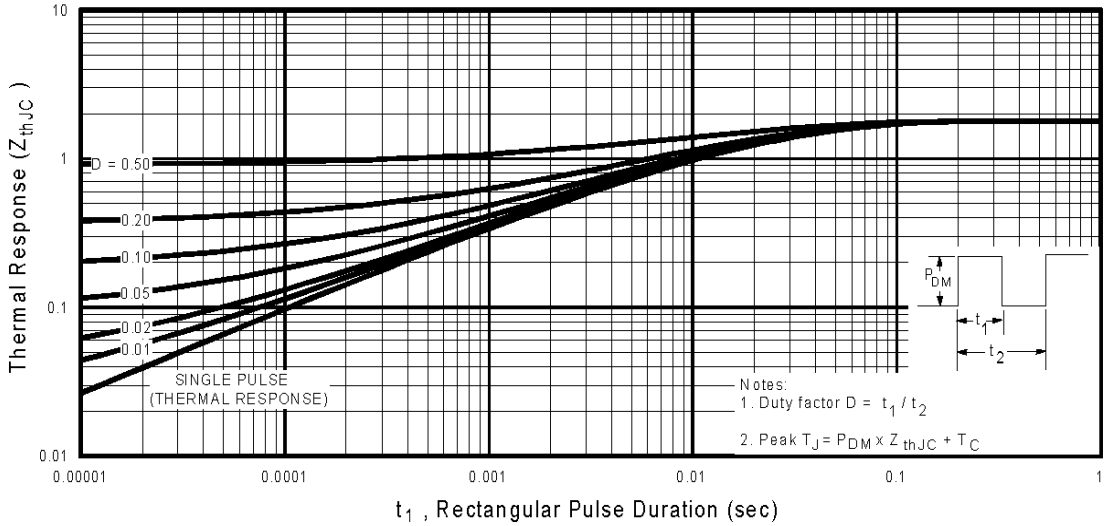


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRL3103D1SPbF

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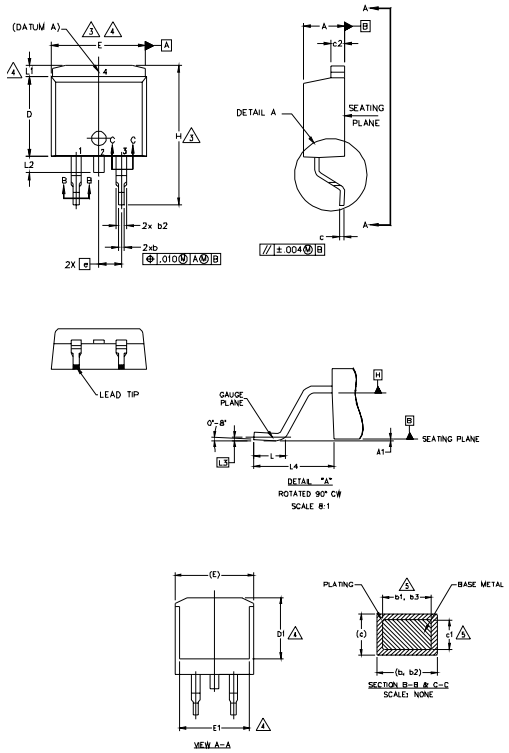
D²Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

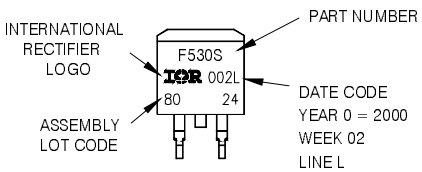
1.– ANODE *
2, 4.– CATHODE
3.– ANODE

* PART DEPENDENT.

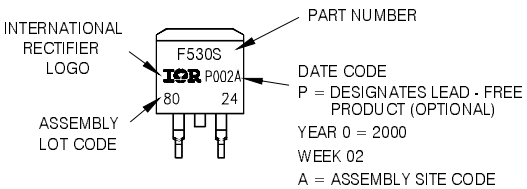
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: "P" in assembly line position
indicates "Lead – Free"

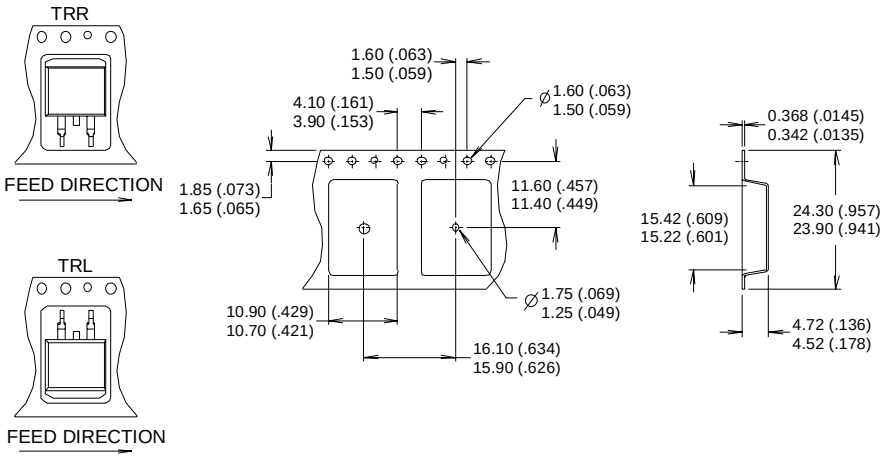


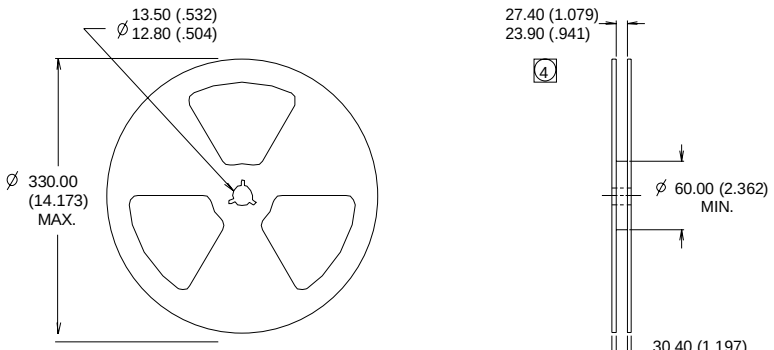
OR



D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.

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