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Si5519DU
 Vishay Siliconix

N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	20	0.036 at V _{GS} = 4.5 V	6.0	5.4 nC
		0.063 at V _{GS} = 2.5 V	6.0	
P-Channel	- 20	0.064 at V _{GS} = - 4.5 V	- 6.0	6.0 nC
		0.095 at V _{GS} = - 2.5 V	- 6.0	

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFETs

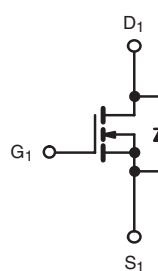
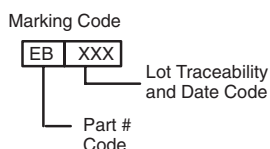
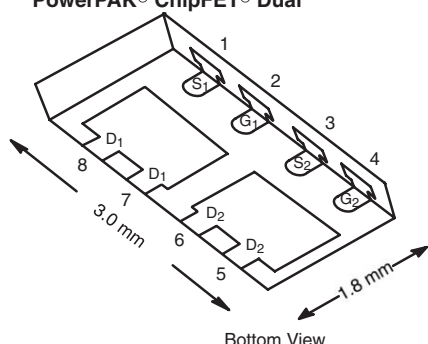


RoHS
 COMPLIANT

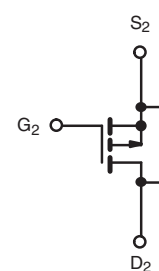
APPLICATIONS

- Portable DC-DC Applications

PowerPAK[®] ChipFET[®] Dual



N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si5519DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	- 20	V
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6.0 ^a	- 6.0 ^a
		T _C = 70 °C	6.0 ^a	- 6.0 ^a
		T _A = 25 °C	6.0 ^{a, b, c}	- 4.8 ^{b, c}
		T _A = 70 °C	4.9 ^{b, c}	- 3.8 ^{b, c}
Pulsed Drain Current	I _{DM}	25	- 20	A
Source Drain Current Diode Current	I _S	T _C = 25 °C	6.0 ^a	
		T _A = 25 °C	1.9 ^{b, c}	- 1.9 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	10.4	10.4
		T _C = 70 °C	6.6	6.6
		T _A = 25 °C	2.27 ^{b, c}	2.27 ^{b, c}
		T _A = 70 °C	1.45 ^{b, c}	1.45 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	43	55	43	55	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	9.5	12	9.5	12	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Reliability Manual for profile. The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 105 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	20		V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		20.74	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-18.2		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		4.0	mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		1.83		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.8	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.8	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch			100	nA
			P-Ch			-100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	25			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 6.1\text{ A}$	N-Ch		0.030	0.036	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -4.8\text{ A}$	P-Ch		0.053	0.064	
		$V_{GS} = 2.5\text{ V}, I_D = 1.6\text{ A}$	N-Ch		0.052	0.063	
		$V_{GS} = -2.5\text{ V}, I_D = -1.05\text{ A}$	P-Ch		0.078	0.095	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 6.7\text{ A}$	N-Ch		15		S
		$V_{DS} = -10\text{ V}, I_D = -4.8\text{ A}$	P-Ch		9.5		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		660		pF
			P-Ch		475		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		108		pF
			P-Ch		135		
Reverse Transfer Capacitance	C_{rss}		N-Ch		65		pF
			P-Ch		100		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.8\text{ A}$	N-Ch		11.65	17.5	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -3.2\text{ A}$	P-Ch		11.7	18	
		N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.8\text{ A}$	N-Ch		5.4	8.1	
			P-Ch		6.0	9.0	
Gate-Source Charge	Q_{gs}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.2\text{ A}$	N-Ch		1.48		nC
			P-Ch		1.05		
Gate-Drain Charge	Q_{gd}		N-Ch		1.4		nC
			P-Ch		2.1		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch		5.2		Ω
			P-Ch		9.8		



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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.04\ \Omega$ $I_D \cong 4.9\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		5.5	8.25	ns
			P-Ch		4.5	6.8	
Rise Time	t_r	P-Channel $V_{DD} = -10\text{ V}$, $R_L = 2.63\ \Omega$ $I_D \cong -3.8\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		15	22.5	
			P-Ch		11	16.5	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		22	33	
			P-Ch		25	37.5	
Fall Time	t_f		N-Ch		6	9	
			P-Ch		8.5	12.8	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			8.6	A
			P-Ch			- 8.6	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			25	V
			P-Ch			- 20	
Body Diode Voltage	V_{SD}	$I_S = 3.1\text{ A}$, $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	ns
		$I_S = -2.2\text{ A}$, $V_{GS} = 0\text{ V}$	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 3.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		14.4	21.6	nC
			P-Ch		20.6	31	
Body Diode Reverse Recovery Charge	Q_{rr}	P-Channel $I_F = -2.2\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		8	12	ns
			P-Ch		7.2	11	
Reverse Recovery Fall Time	t_a		N-Ch		10		
			P-Ch		6.6		
Reverse Recovery Rise Time	t_b		N-Ch		4.4		
			P-Ch		14		

Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

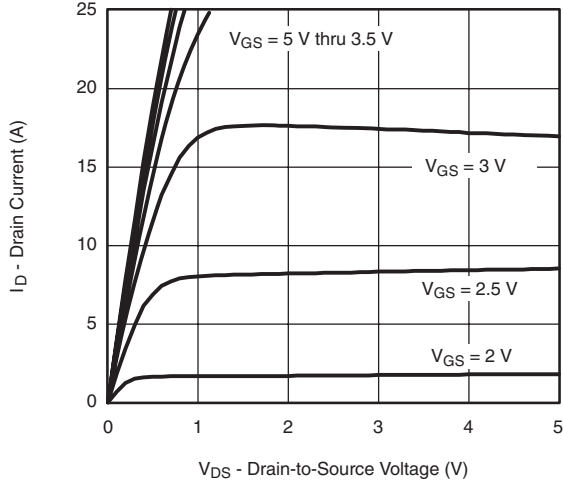
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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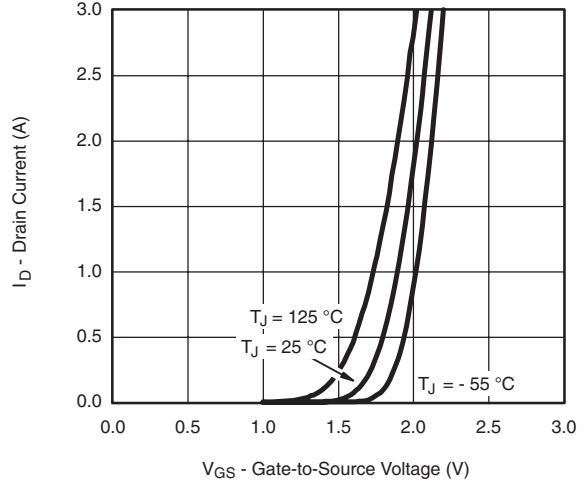
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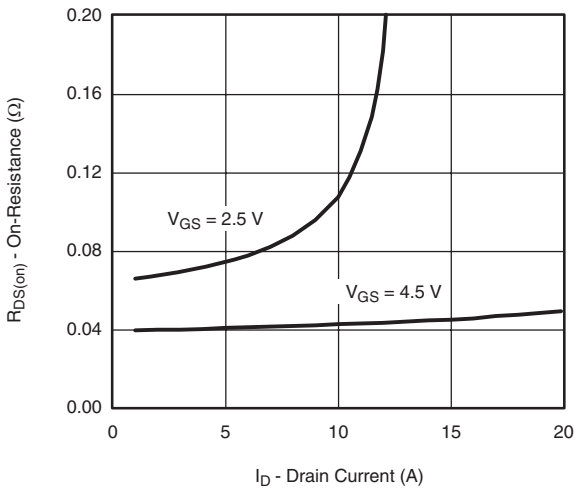
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



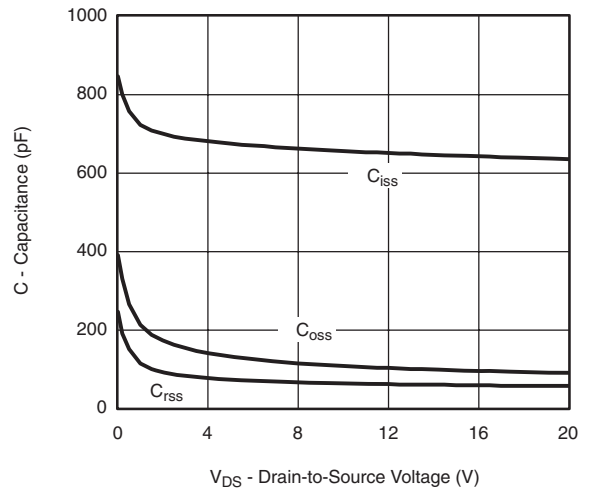
Output Characteristics



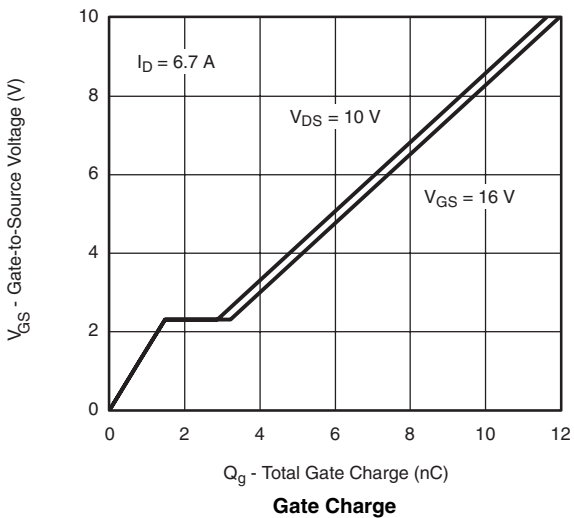
Transfer Characteristics



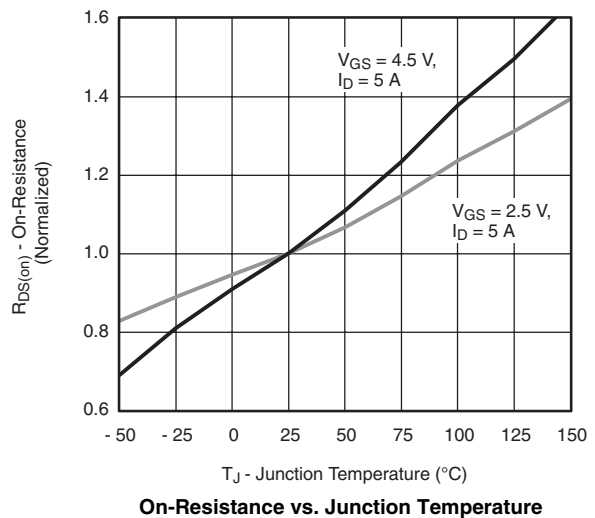
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

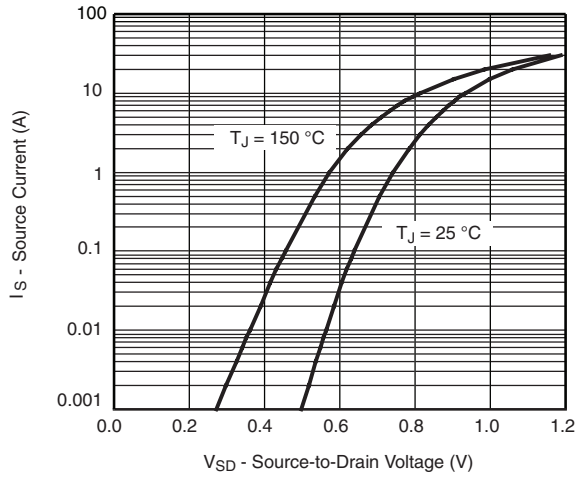


On-Resistance vs. Junction Temperature

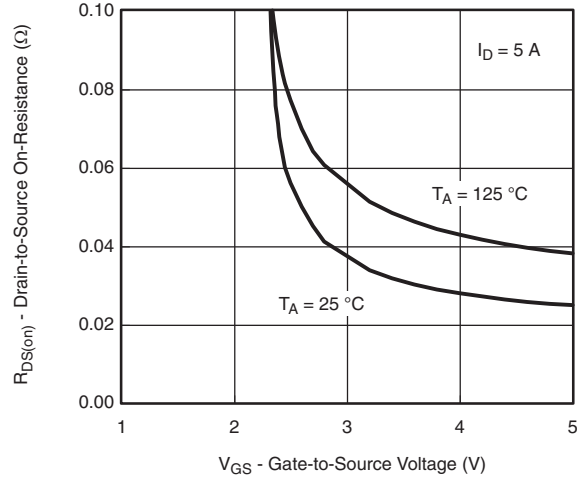


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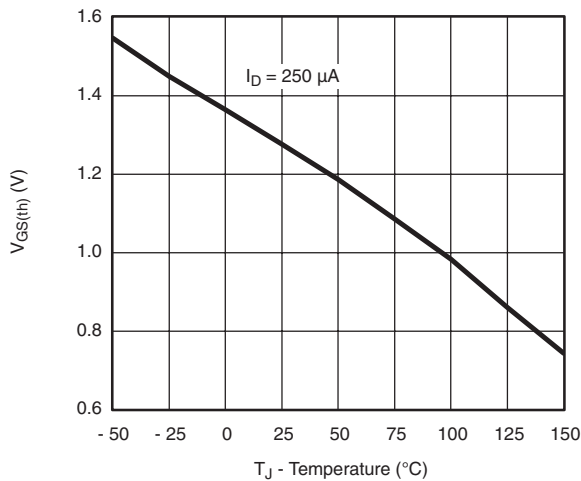
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



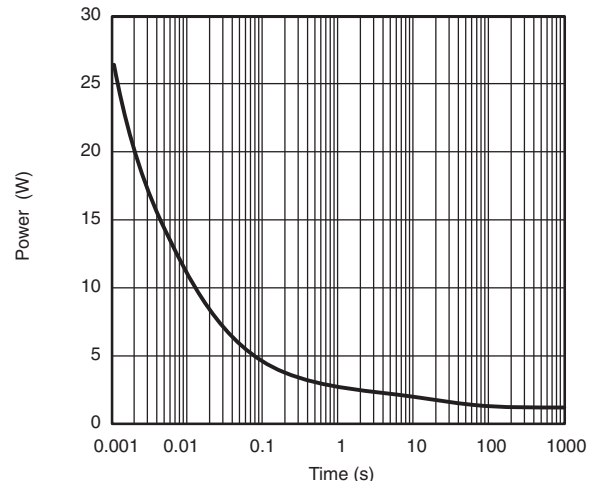
Source-Drain Diode Forward Voltage



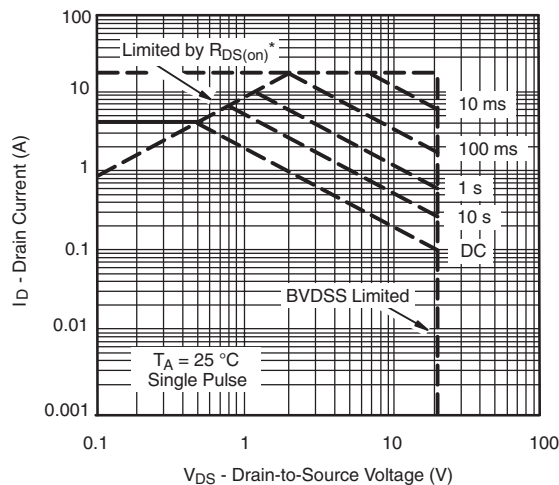
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

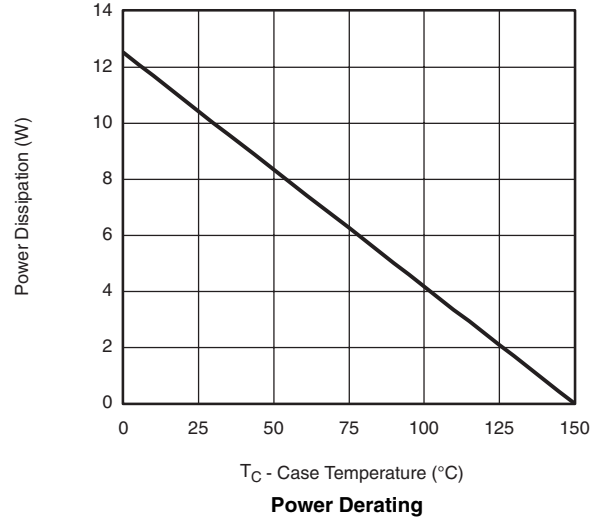
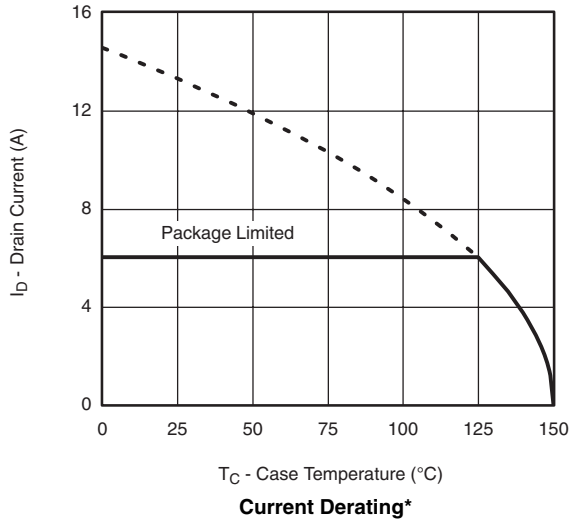
Safe Operating Area, Junction-to-Ambient

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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

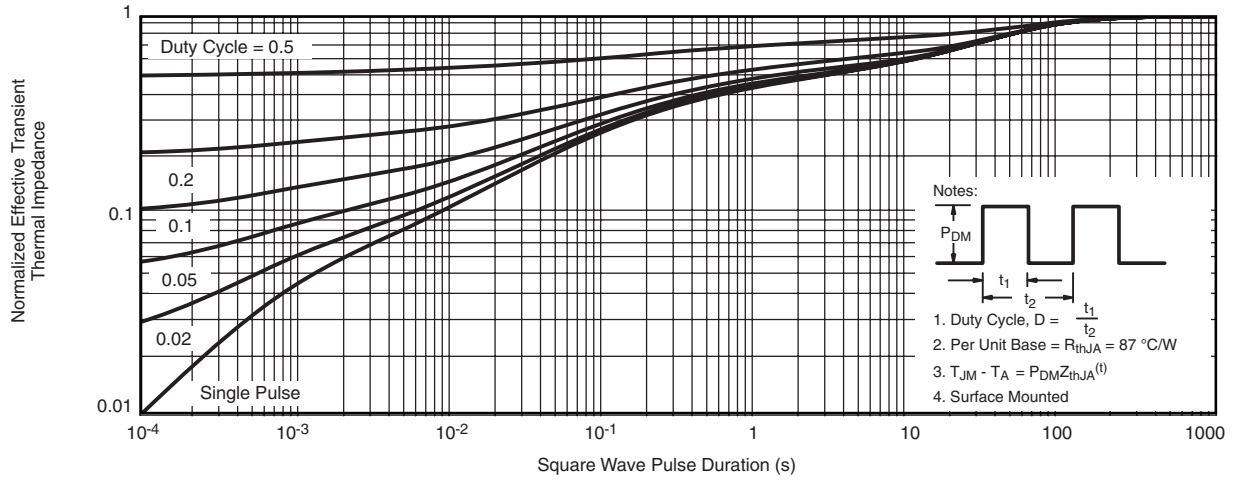


* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

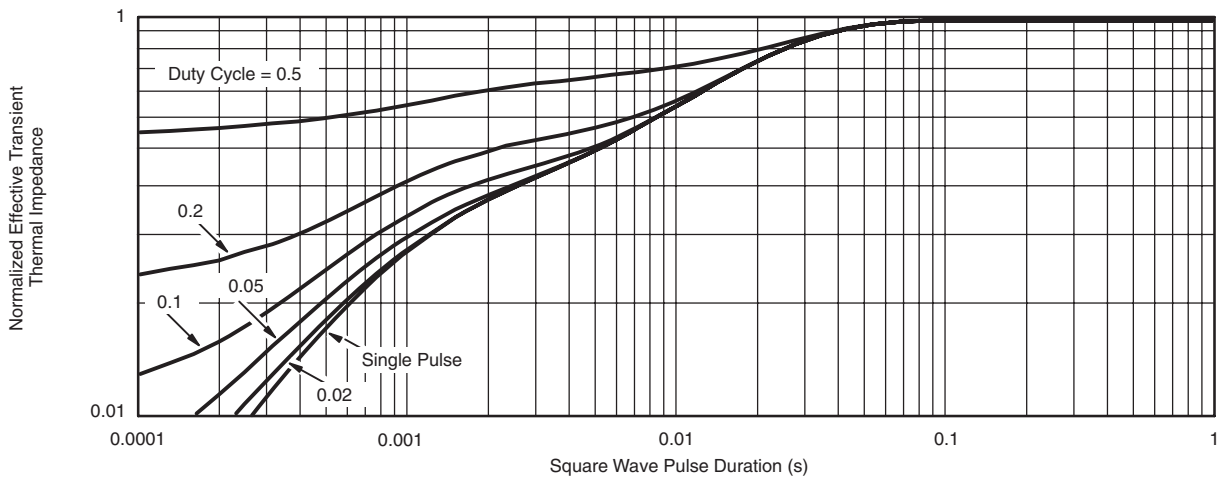


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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



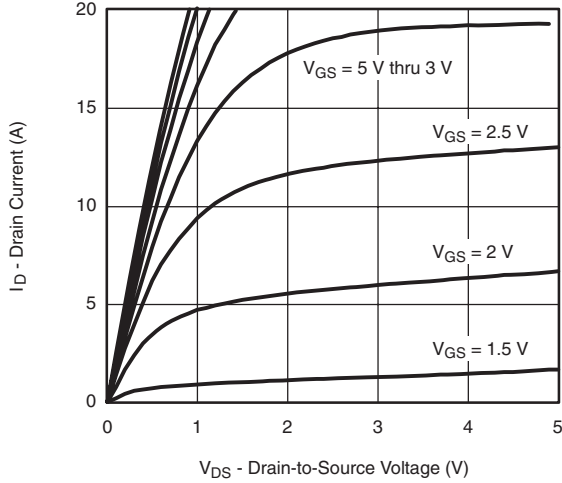
Normalized Thermal Transient Impedance, Junction-to-Case

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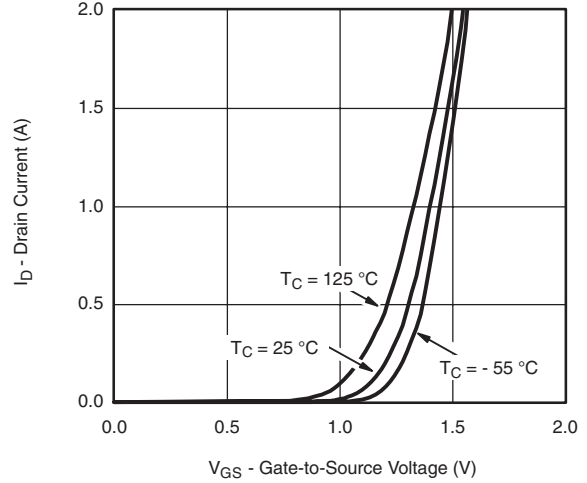
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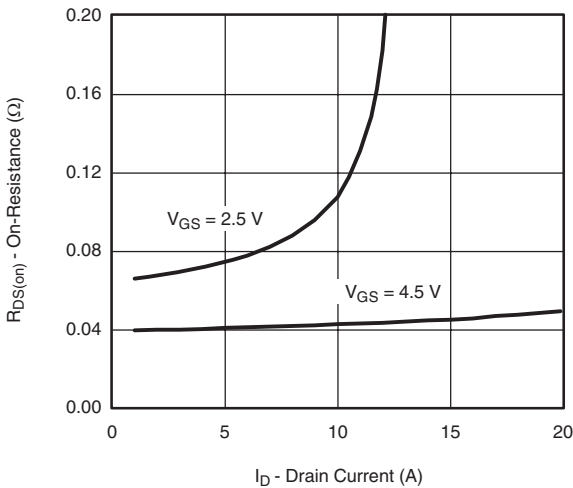
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



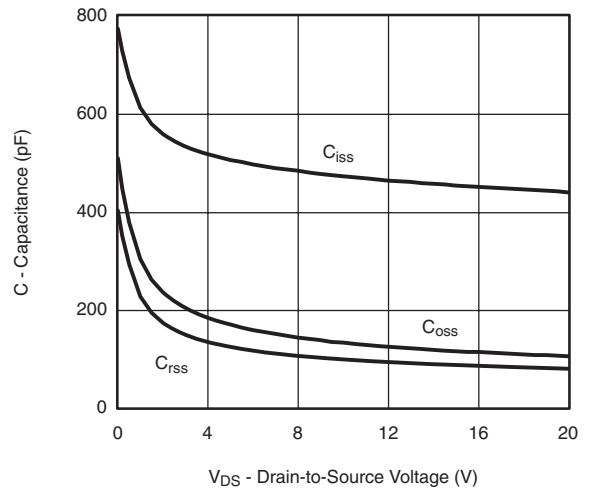
Output Characteristics



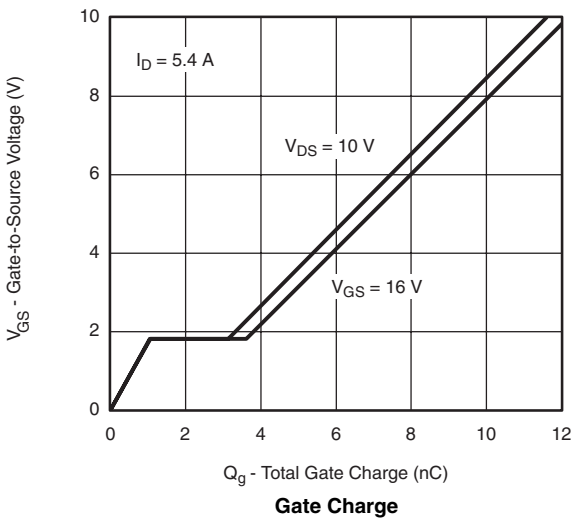
Transfer Characteristics



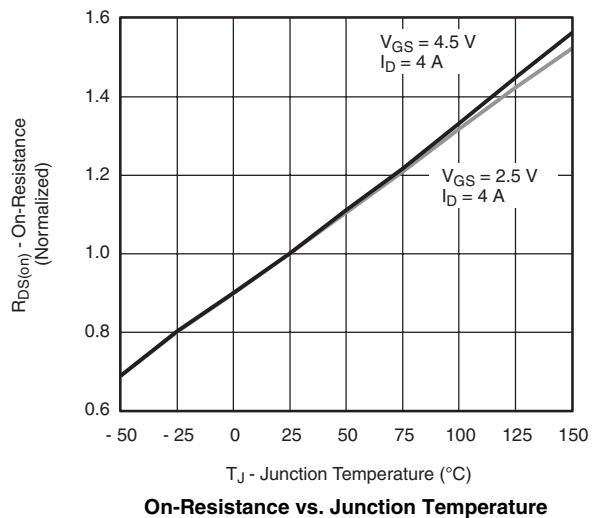
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

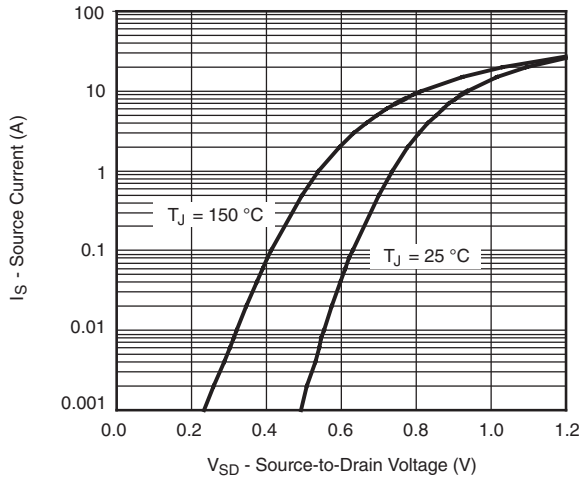


On-Resistance vs. Junction Temperature

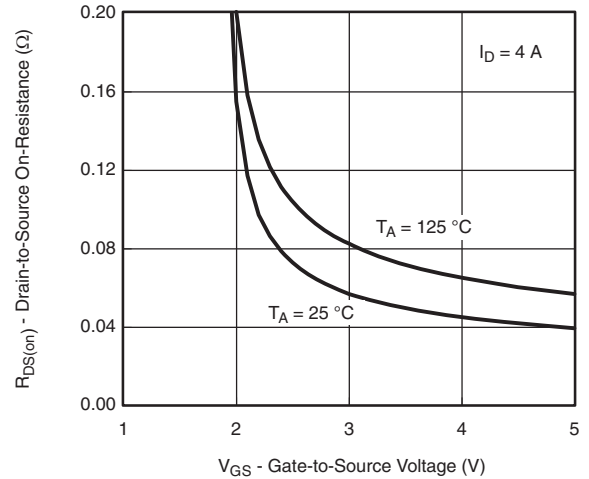


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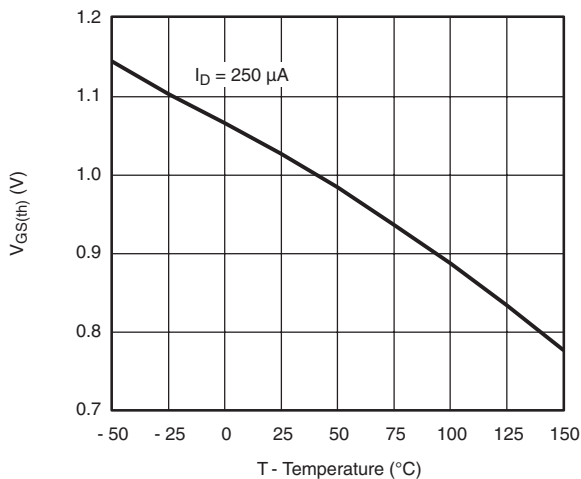
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



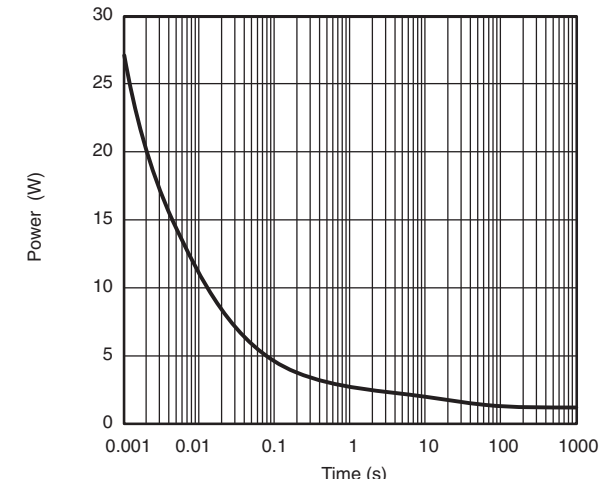
Source-Drain Diode Forward Voltage



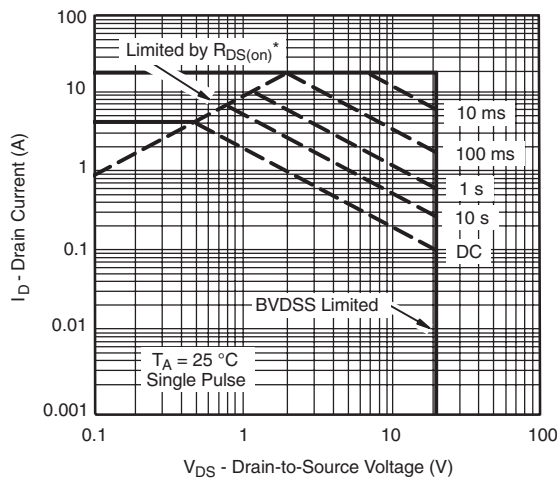
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

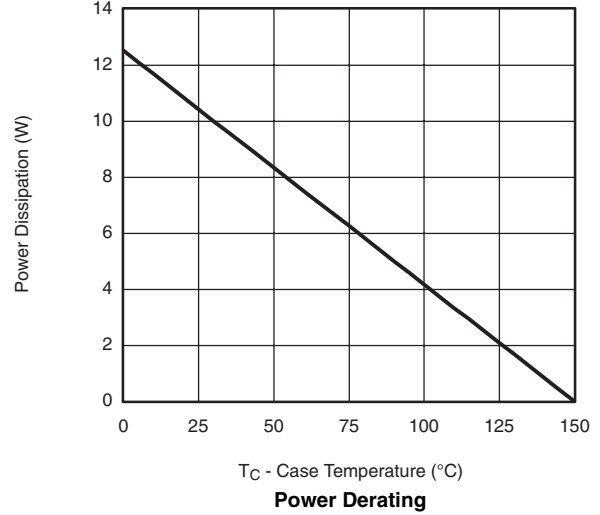
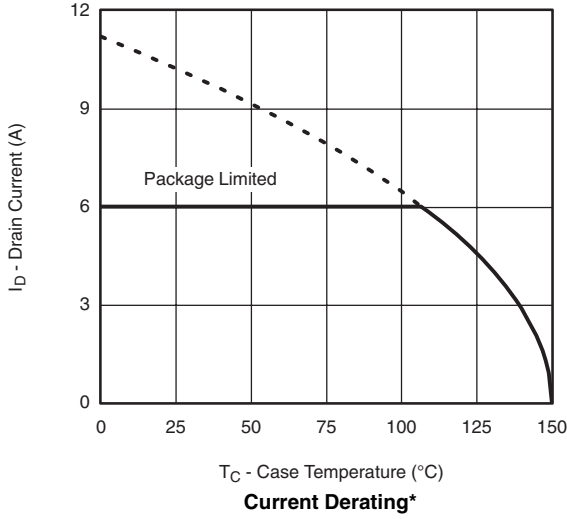
Safe Operating Area, Junction-to-Case

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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

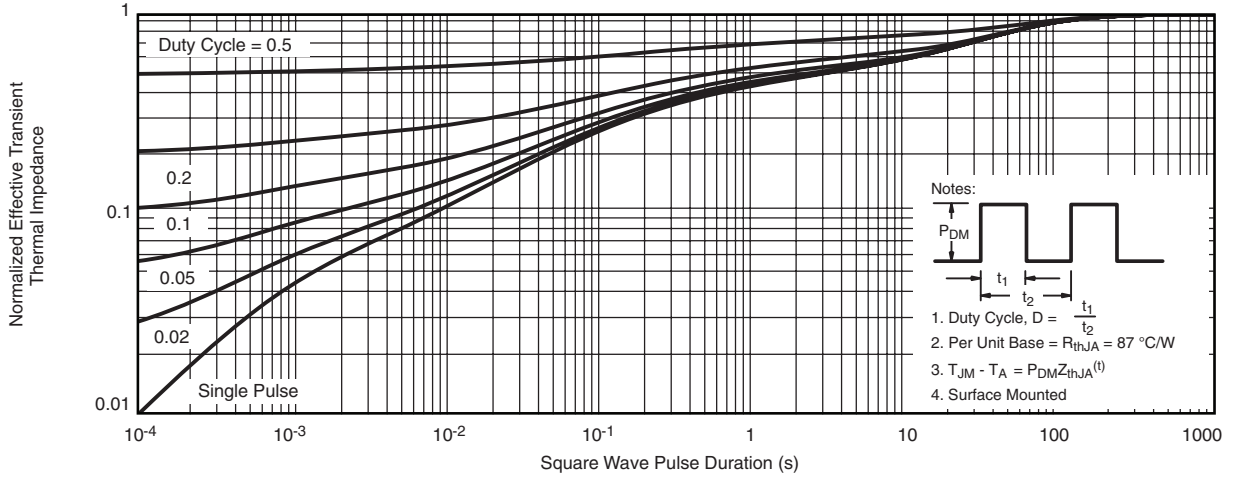


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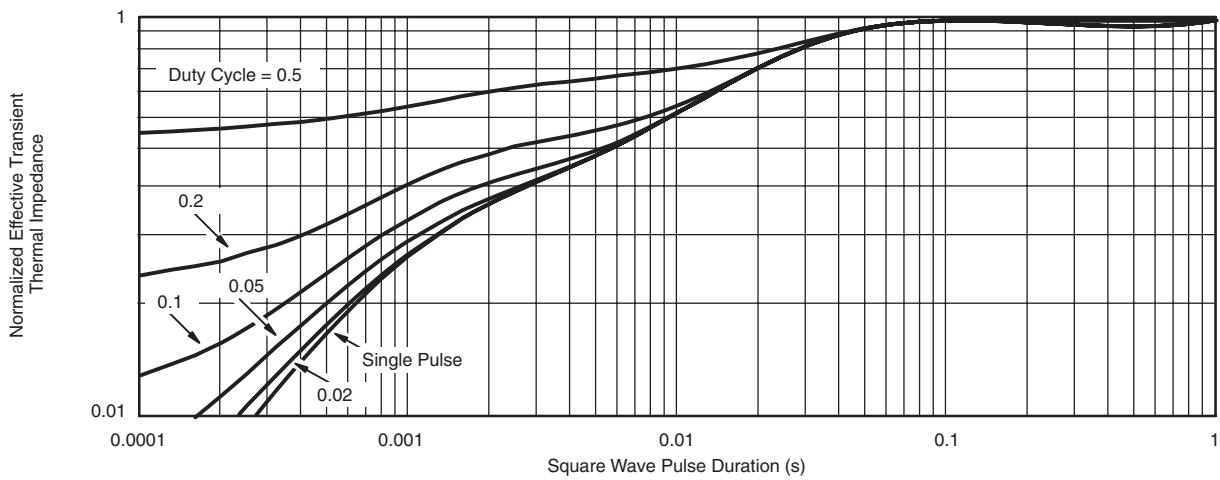


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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74406>.



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