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Stocking Distributor

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[SIA513DJ-T1-GE3](#)

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sales@integrated-circuit.com

New Product



SiA513DJ
 Vishay Siliconix

N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	20	0.060 at V _{GS} = 4.5 V	4.5 ^a	3.5 nC
		0.092 at V _{GS} = 2.5 V	4.5 ^a	
P-Channel	- 20	0.110 at V _{GS} = - 4.5 V	- 4.5 ^a	3 nC
		0.185 at V _{GS} = - 2.5 V	- 4.5 ^a	

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFETs
- New Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance

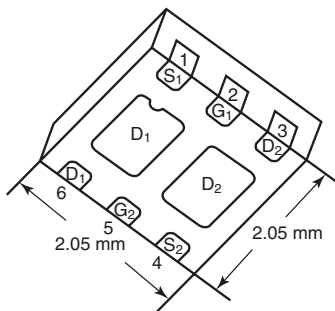


RoHS
 COMPLIANT

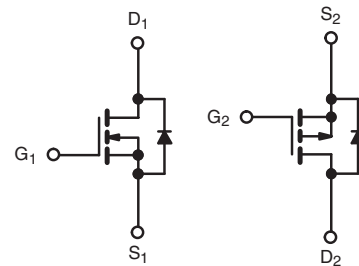
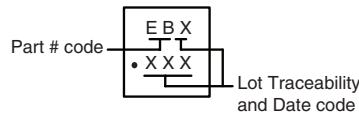
APPLICATIONS

- Portable Devices

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA513DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	- 20	V
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	4.5 ^a	- 4.5 ^a
		T _C = 70 °C	4.5 ^a	- 4.5 ^a
		T _A = 25 °C	4.5 ^{a, b, c}	- 3.3 ^{b, c}
		T _A = 70 °C	3.2 ^{b, c}	- 2.4 ^{b, c}
Pulsed Drain Current	I _{DM}	15	- 10	A
Source Drain Current Diode Current	I _S	T _C = 25 °C	4.5 ^a	
		T _A = 25 °C	1.6 ^{b, c}	- 1.6 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	6.5	6.5
		T _C = 70 °C	5	5
		T _A = 25 °C	1.9 ^{b, c}	1.9 ^{b, c}
		T _A = 70 °C	1.2 ^{b, c}	1.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	52	65	52	65	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	12.5	16	12.5	16		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	20			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		22		mV/°C
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-16		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-3.5		mV/°C
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		2.5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	10			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-5			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.4\text{ A}$	N-Ch		0.050	0.060	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -2.5\text{ A}$	P-Ch		0.091	0.110	
		$V_{GS} = 2.5\text{ V}, I_D = 1.1\text{ A}$	N-Ch		0.076	0.092	
		$V_{GS} = -2.5\text{ V}, I_D = -0.54\text{ A}$	P-Ch		0.152	0.185	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 3.4\text{ A}$	N-Ch		8		S
		$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}$	P-Ch		3.5		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		360		pF
			P-Ch		250		
Output Capacitance	C_{oss}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		70		
			P-Ch		70		
Reverse Transfer Capacitance	C_{rss}		N-Ch		40		
			P-Ch		45		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	N-Ch		7.5	12	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -3.3\text{ A}$	P-Ch		6	9	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.5\text{ A}$	N-Ch		3.5	5.3	
			P-Ch		3	4.5	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.3\text{ A}$	N-Ch		0.9		
			P-Ch		0.7		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch		2.5		Ω
			P-Ch		8		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		10	15	ns
			P-Ch		20	30	
Rise Time	t_r	P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\ \Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		40	60	
			P-Ch		45	70	
Turn-Off Delay Time	$t_{d(off)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		20	30	
			P-Ch		15	25	
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\ \Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		30	45	
			P-Ch		10	15	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		5	10	
			P-Ch		4	8	
Rise Time	t_r	P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\ \Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		15	25	
			P-Ch		12	20	
Turn-Off Delay Time	$t_{d(off)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\ \Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		15	25	
			P-Ch		12	20	
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\ \Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		10	15	
			P-Ch		5	10	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			4.5	A
			P-Ch			-4.5	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			15	
			P-Ch			-10	
Body Diode Voltage	V_{SD}	$I_S = 3.6\text{ A}$, $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -2.6\text{ A}$, $V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 3.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		15	30	ns
			P-Ch		20	40	
Body Diode Reverse Recovery Charge	Q_{rr}	P-Channel $I_F = -2.6\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		10	20	nC
			P-Ch		10	20	
Reverse Recovery Fall Time	t_a		N-Ch		10		ns
			P-Ch		8		
Reverse Recovery Rise Time	t_b		N-Ch		5		
			P-Ch		12		

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

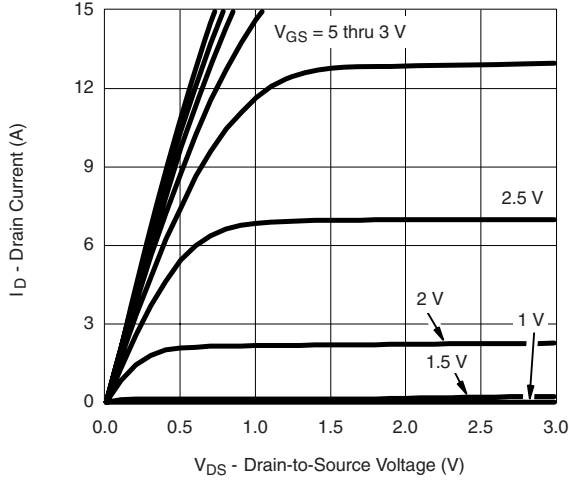
New Product

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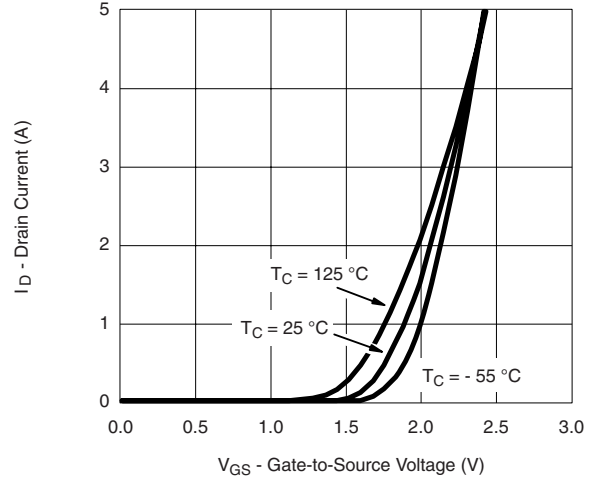
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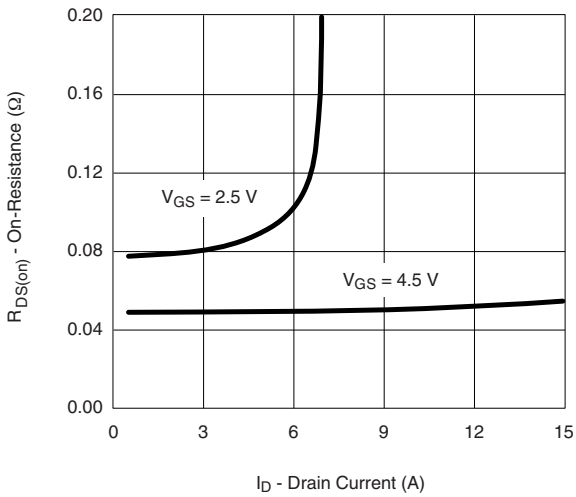
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



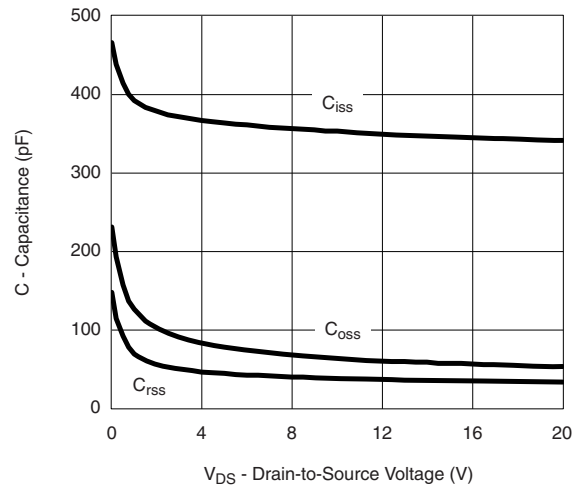
Output Characteristics



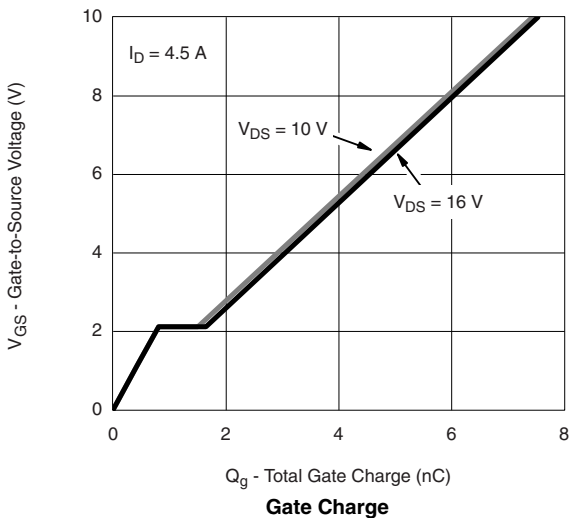
Transfer Characteristics



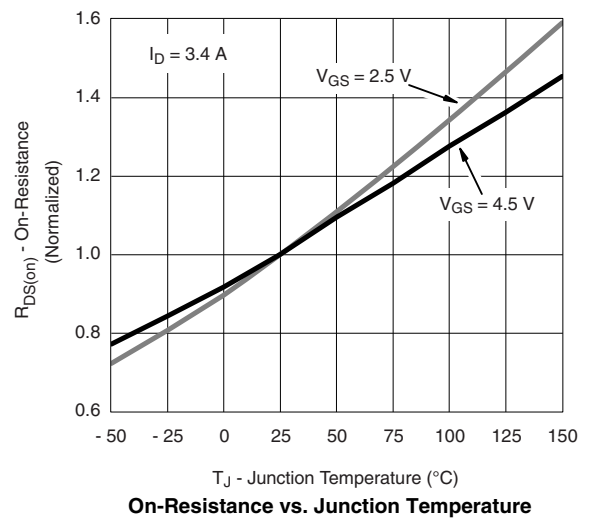
On-Resistance vs. Drain Current



Capacitance



Gate Charge



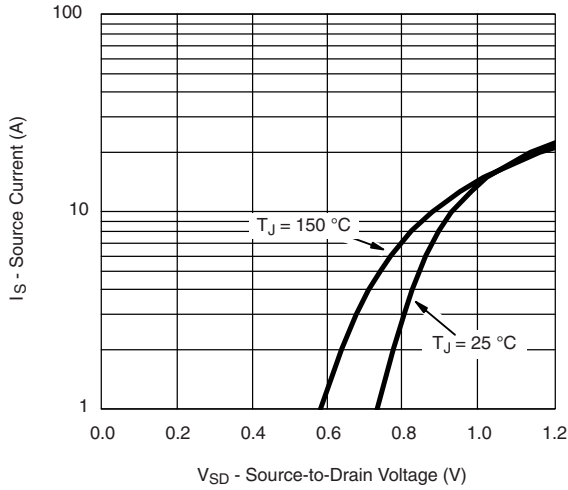
On-Resistance vs. Junction Temperature

New Product

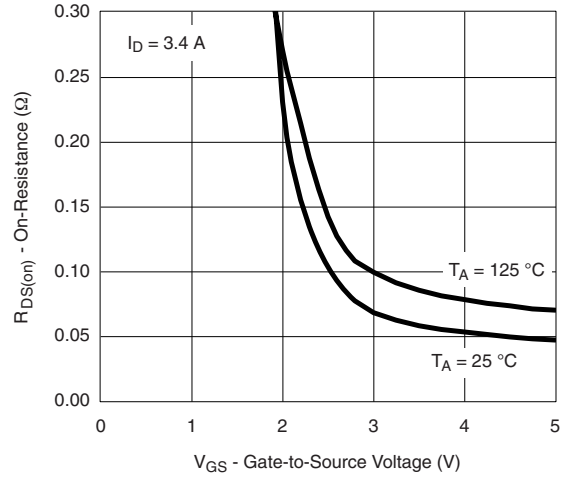


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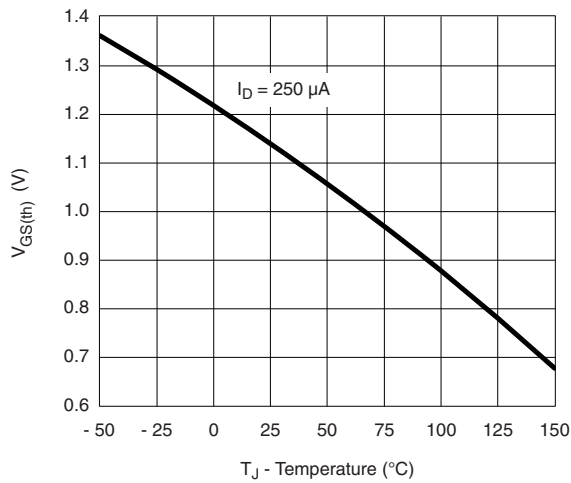
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



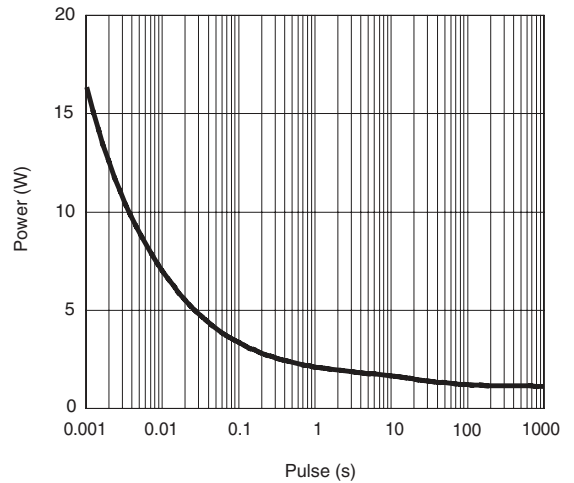
Source-Drain Diode Forward Voltage



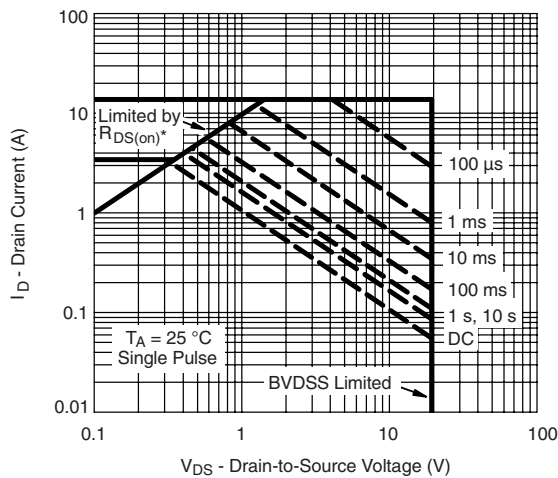
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Safe Operating Area, Junction-to-Ambient
 * $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

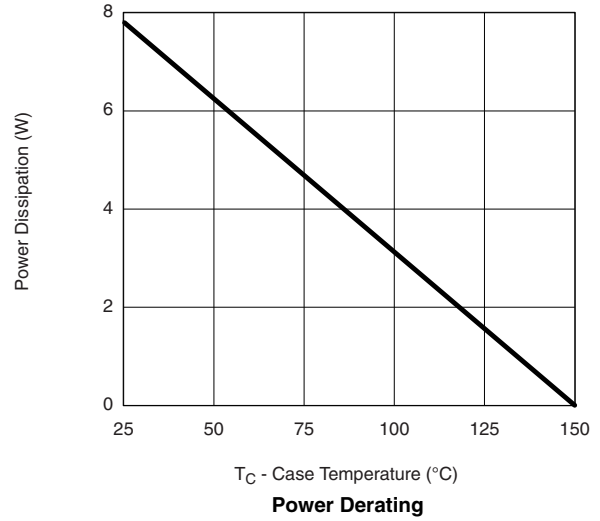
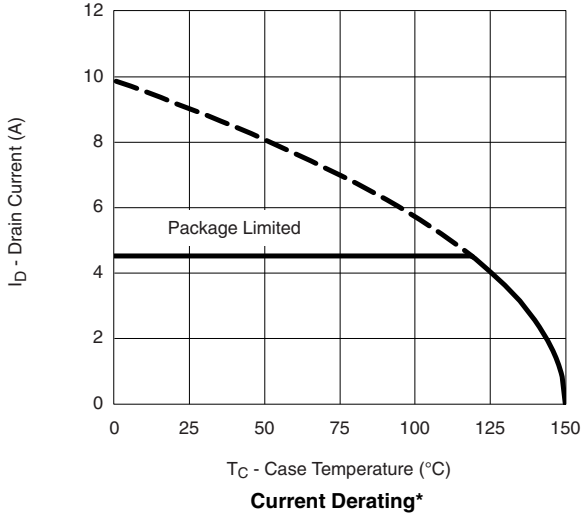
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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



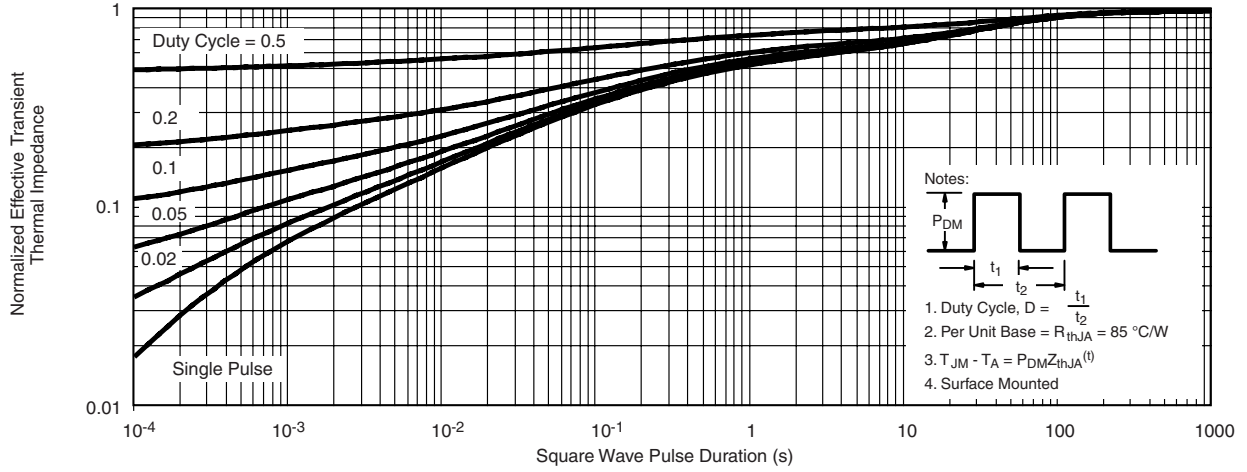
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

New Product

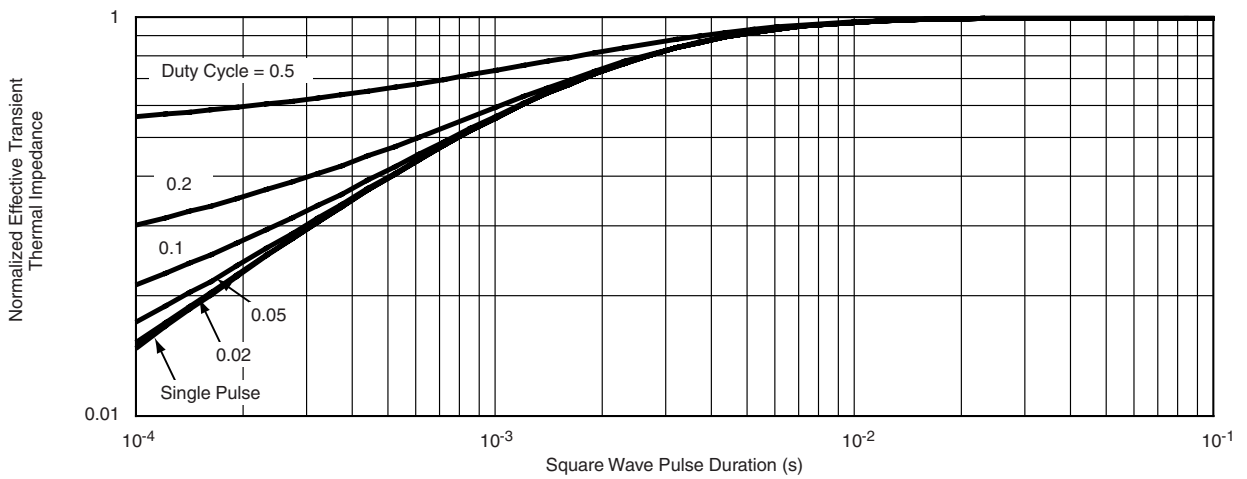


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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

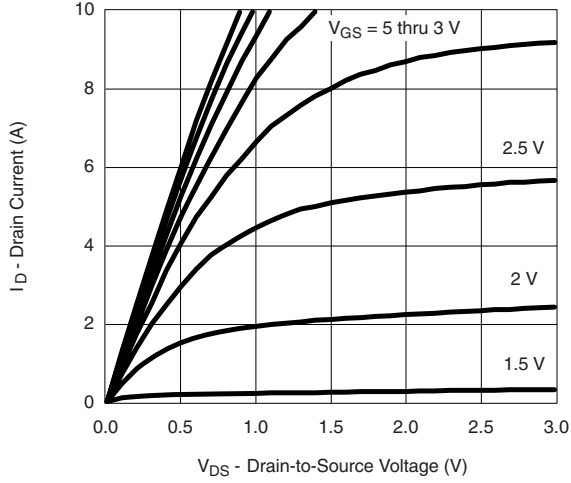
New Product

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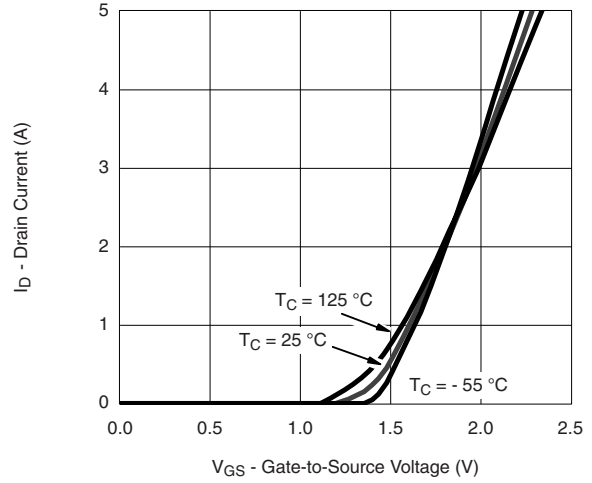
Vishay Siliconix



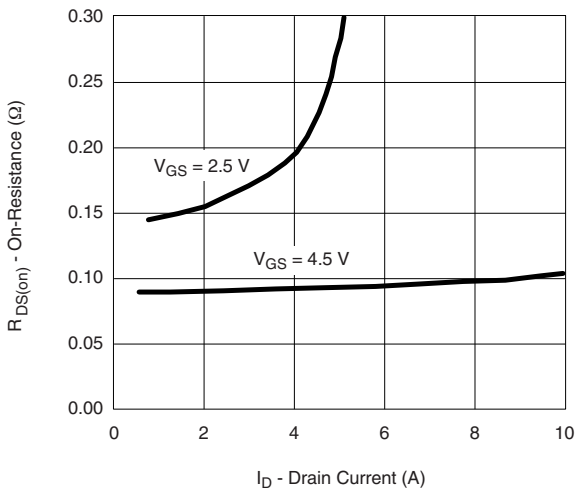
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



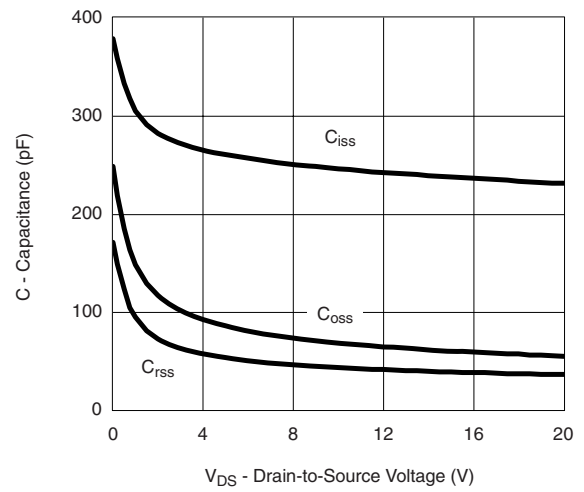
Output Characteristics



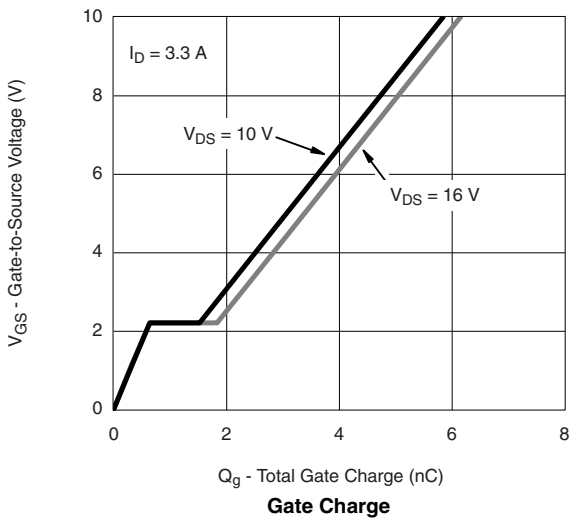
Transfer Characteristics



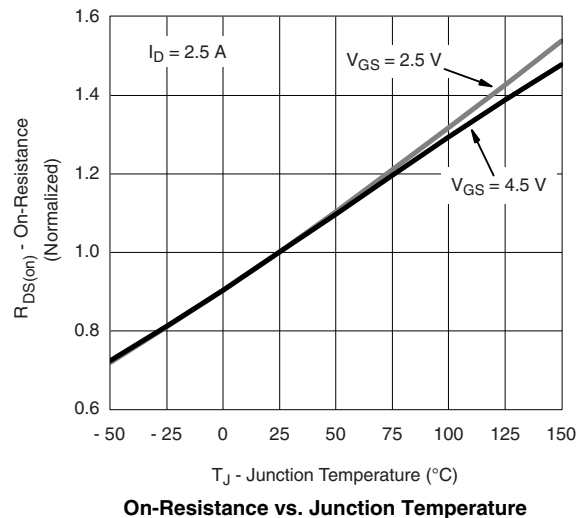
On-Resistance vs. Drain Current



Capacitance



Gate Charge



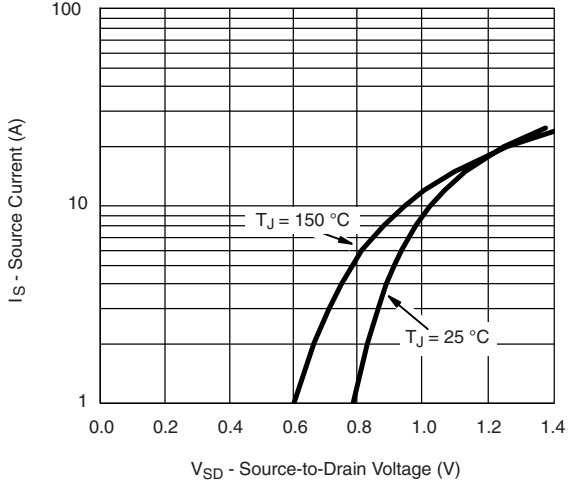
On-Resistance vs. Junction Temperature

New Product

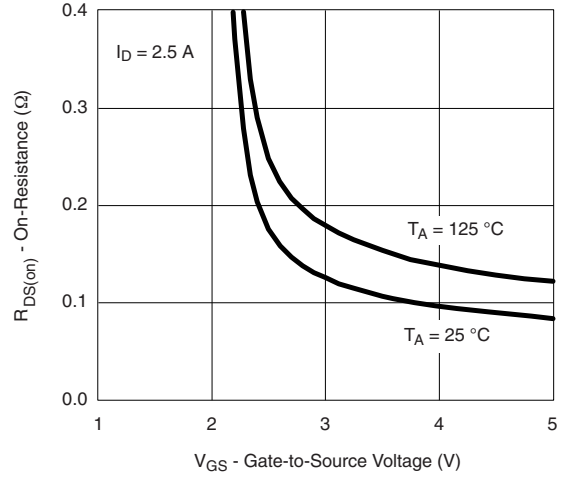


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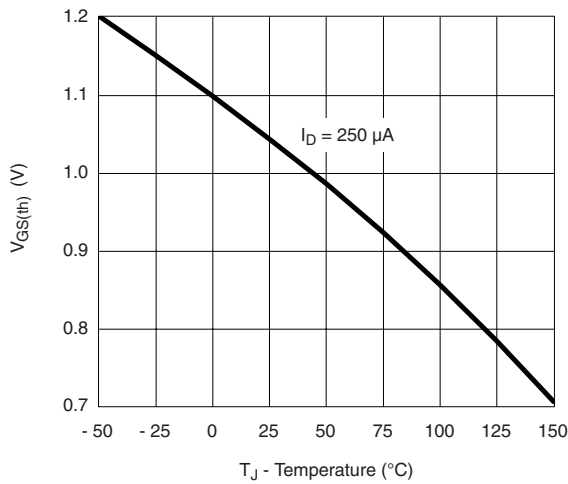
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



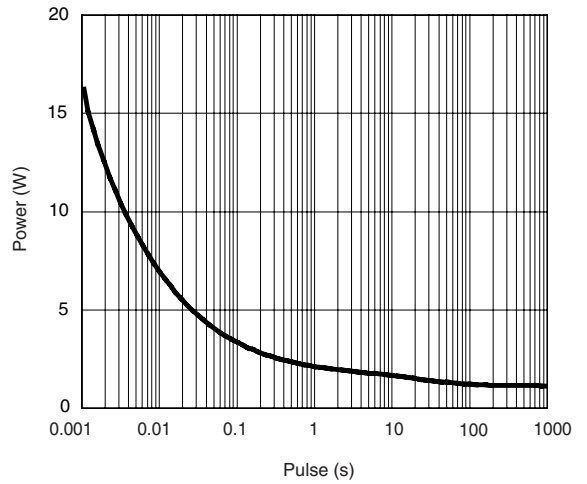
Source-Drain Diode Forward Voltage



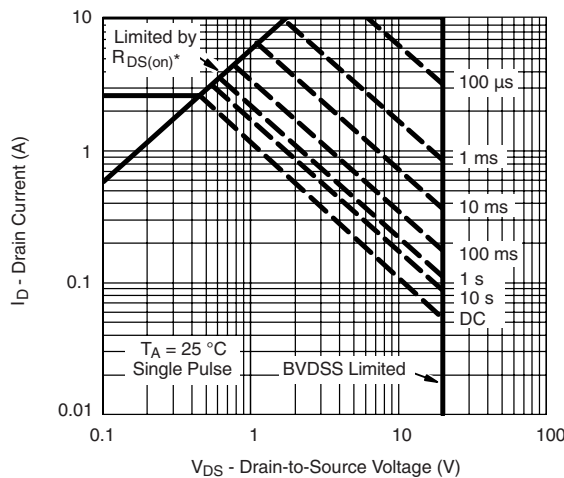
On-Resistance vs. Gate-to-Source



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

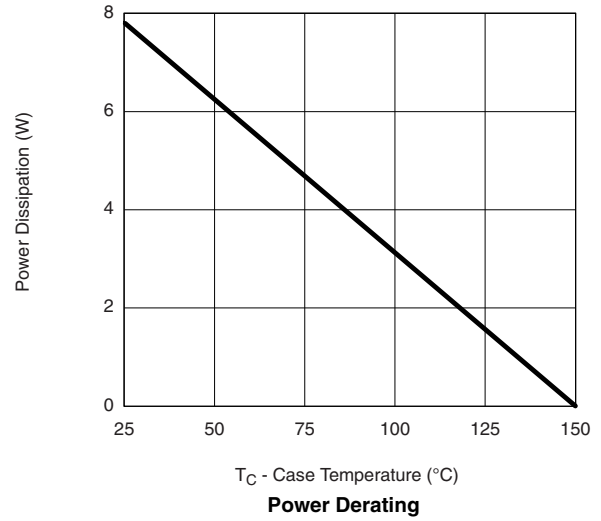
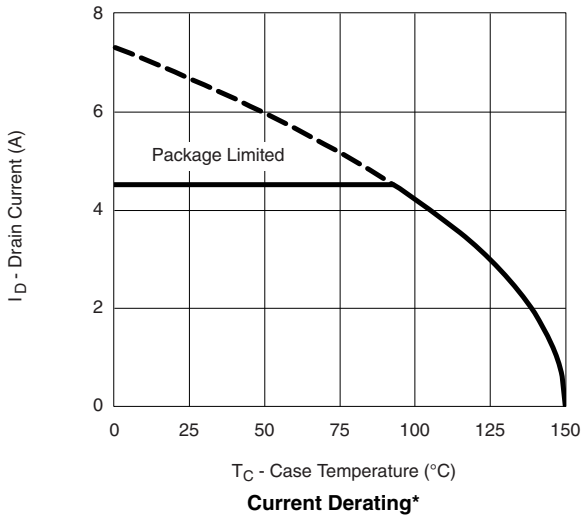
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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



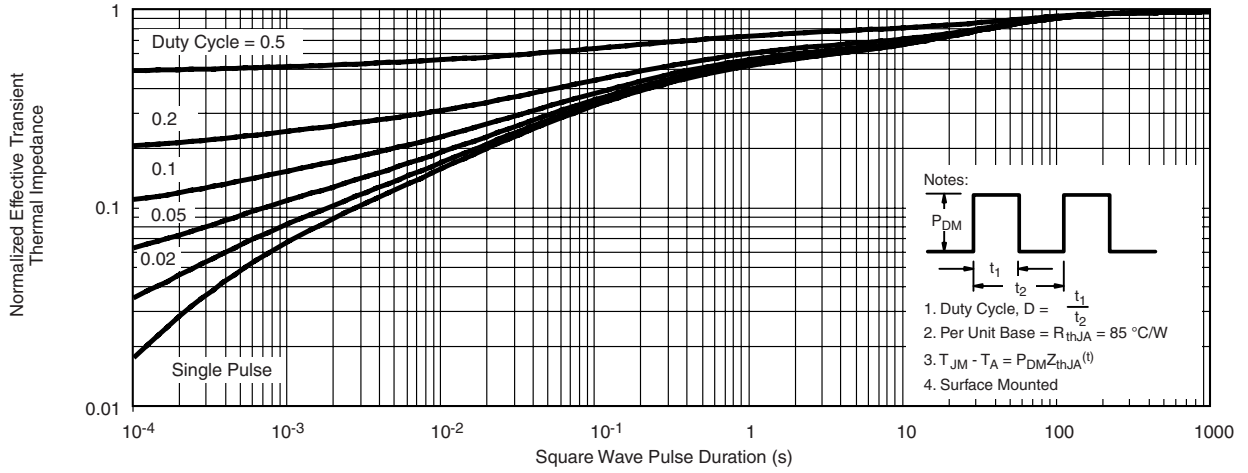
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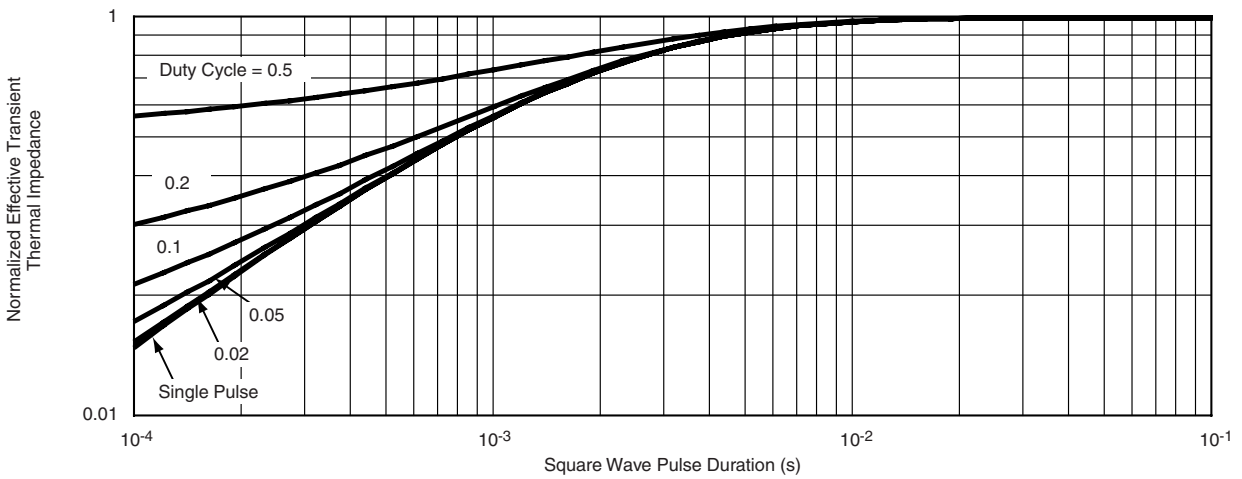


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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

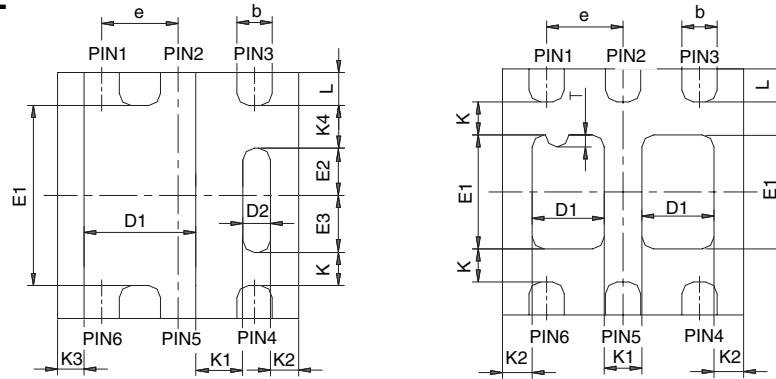
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70443>.



Package Information

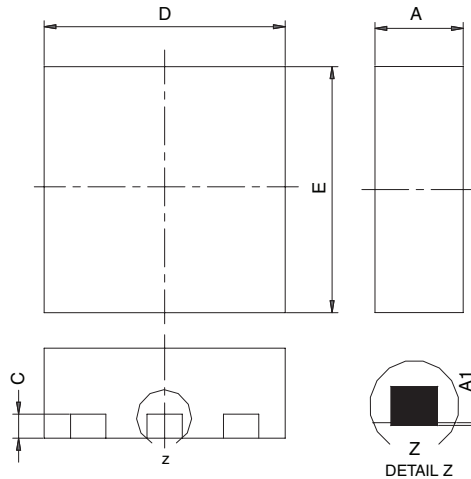
Vishay Siliconix

PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

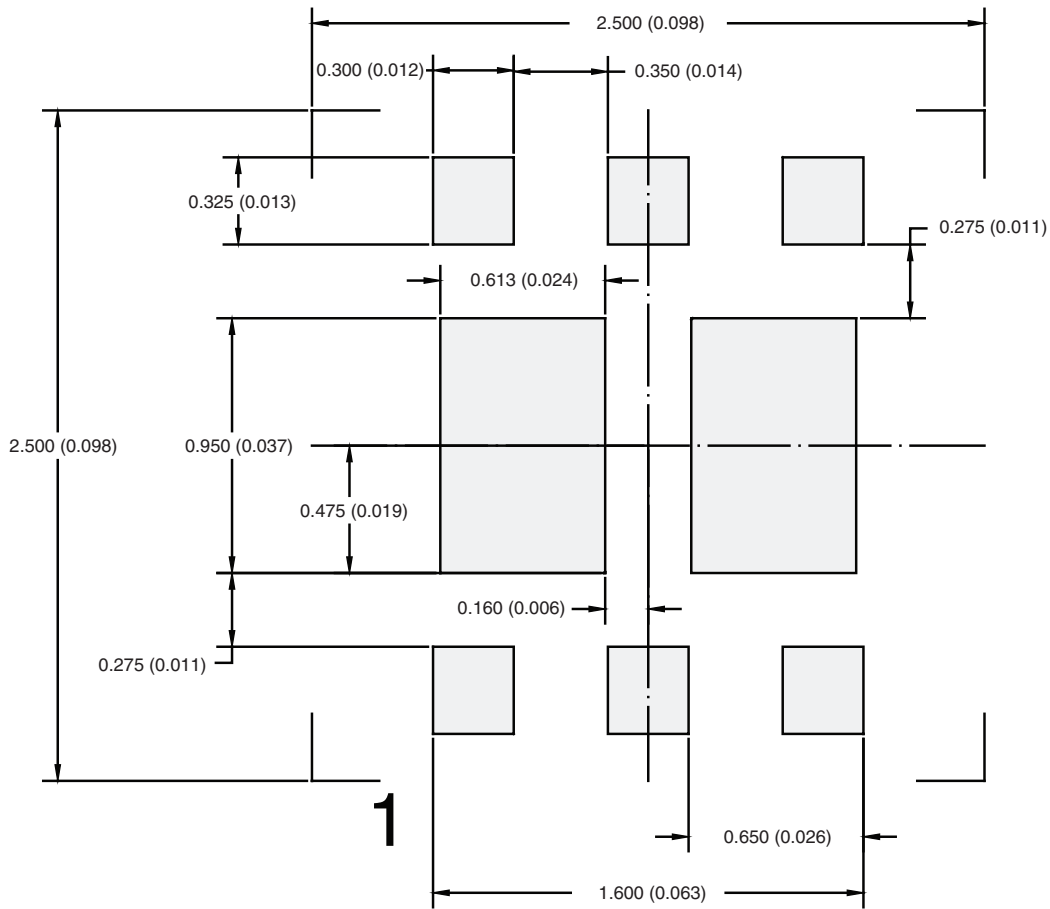
ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

Application Note 826

Vishay Siliconix



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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